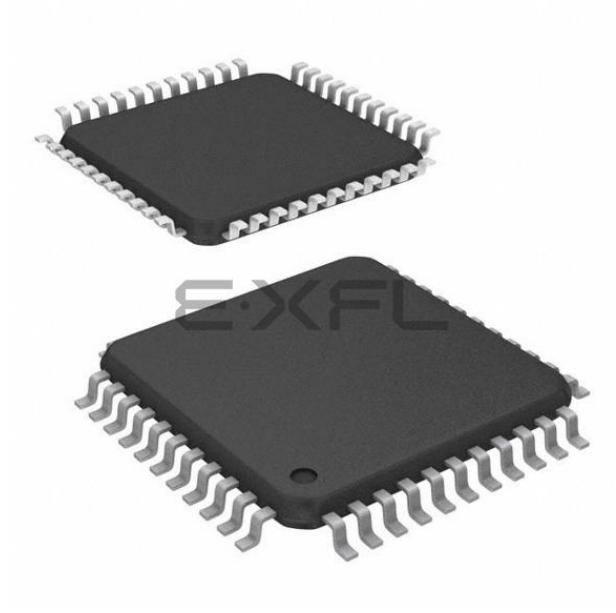

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	25 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1502asl-25au44

Enhanced Features

- Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)
- Output Enable Product Terms
- D Latch Mode
- Combinatorial Output with Registered Feedback within Any Macrocell
- Three Global Clock Pins
- ITD (Input Transition Detection) Circuits on Global Clocks, Inputs and I/O (“L” Versions)
- Fast Registered Input from Product Term
- Programmable “Pin-keeper” Option
- V_{CC} Power-up Reset Option
- Pull-up Option on JTAG Pins TMS and TDI
- Advanced Power Management Features
  - Input Transition Detection
  - Power-down (“L” Versions)
  - Individual Macrocell Power Option
  - Disable ITD on Global Clocks, Inputs, and I/O

Description

The Atmel® ATF1502AS(L) is a high-performance, high-density Complex Programmable Logic Device (CPLD) which utilizes the Atmel proven electrically-erasable technology. With 32 logic macrocells and up to 36 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI, and classic PLDs. The ATF1502AS(L)’s enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1502AS(L) has up to 32 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can serve as a global control signal, register clock, register reset, or output enable. Each of these control signals can be selected for use individually within each macrocell.

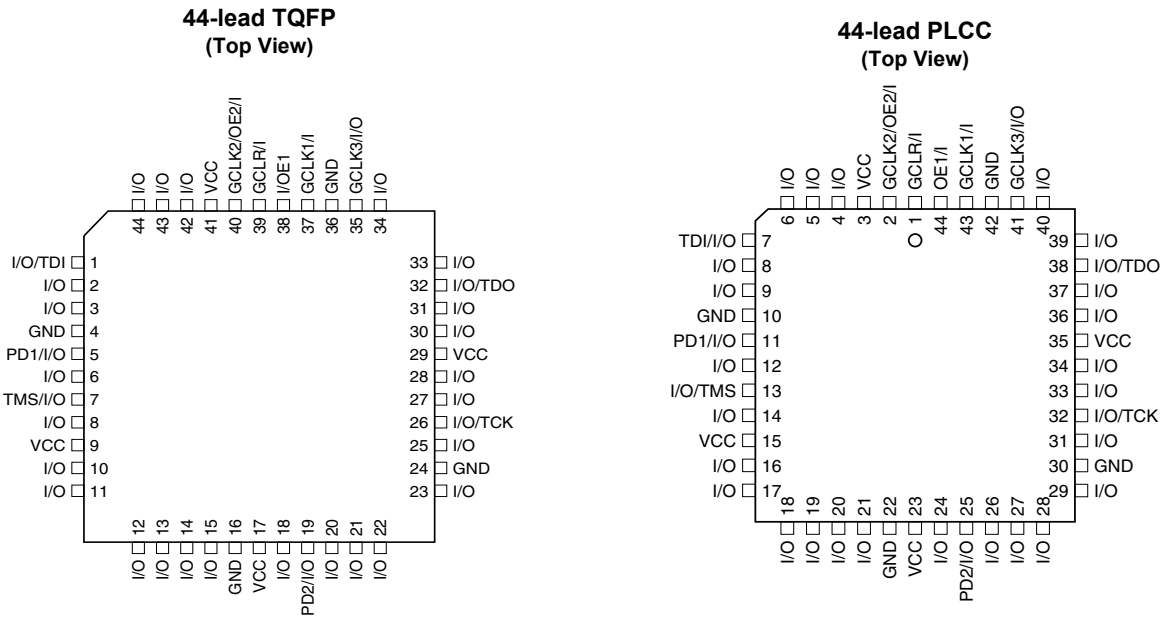
Each of the 32 macrocells generates a buried feedback which goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1502AS(L) allows fast, efficient generation of complex logic functions. The ATF1502AS(L) contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1502AS(L) macrocell, shown in Figure 1, is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of five sections:

- Product Terms and Product Term Select Multiplexer
- OR/XOR/CASCADE Logic
- Flip-flop
- Output Select and Enable
- Logic Array Inputs

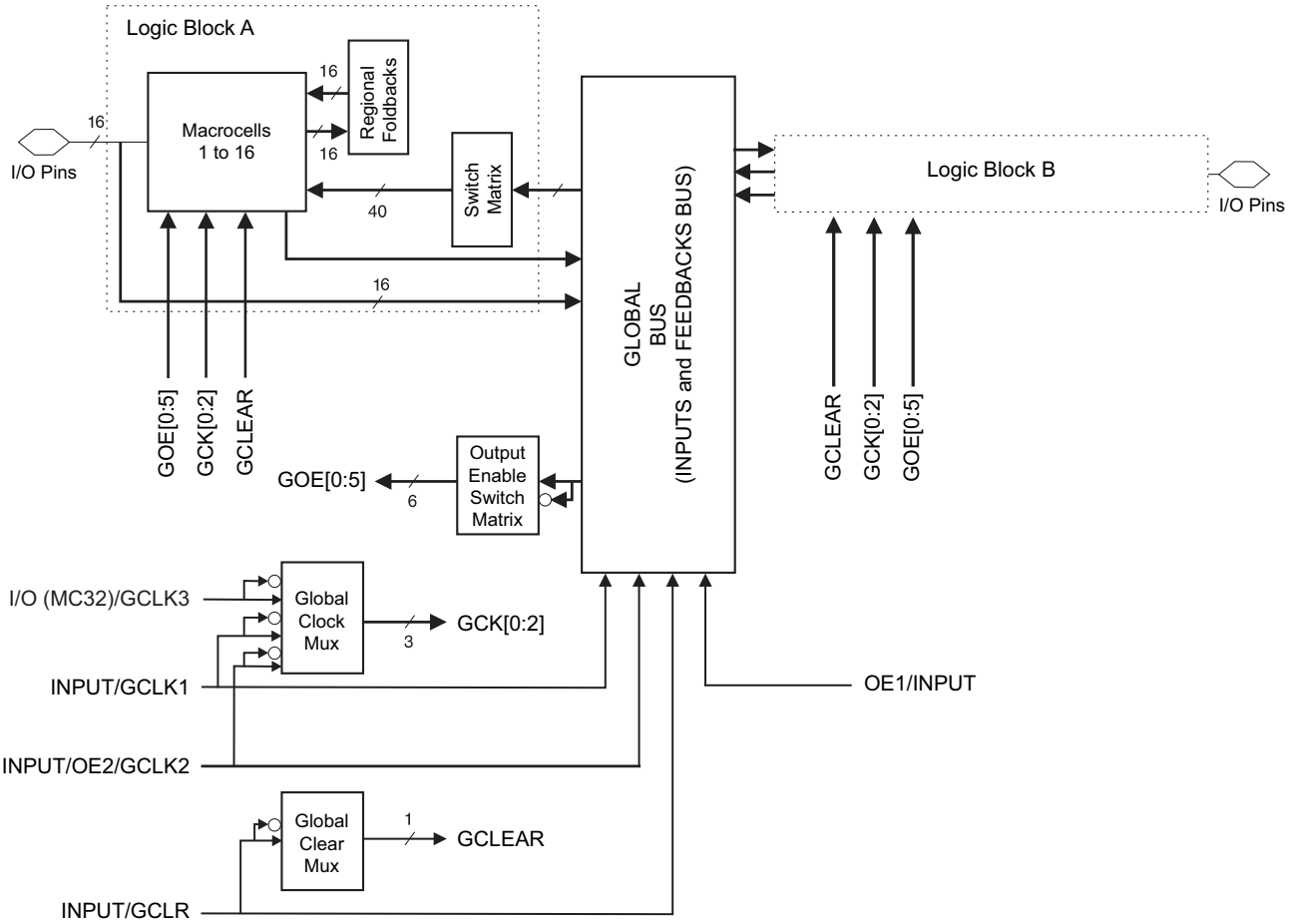
1. Pin Configurations and Pinouts

Figure 1-1. Pinouts



2. Block Diagram

Figure 2-1. Block Diagram



Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1502AS(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1502AS(L) device is an In-System Programmable (ISP) device. It uses the industry standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

4. Programmable Pin-keeper Option for Inputs and I/Os

The ATF1502AS(L) offers the option of programming all input and I/O pins so the pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Figure 4-1. Input Diagram

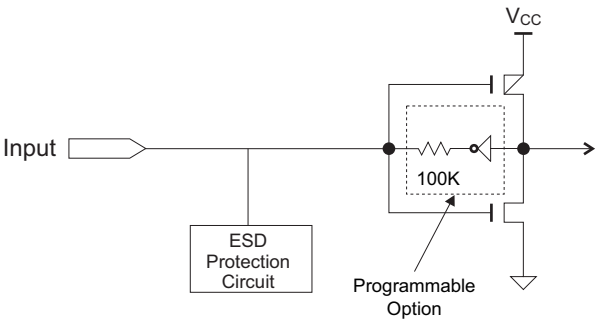
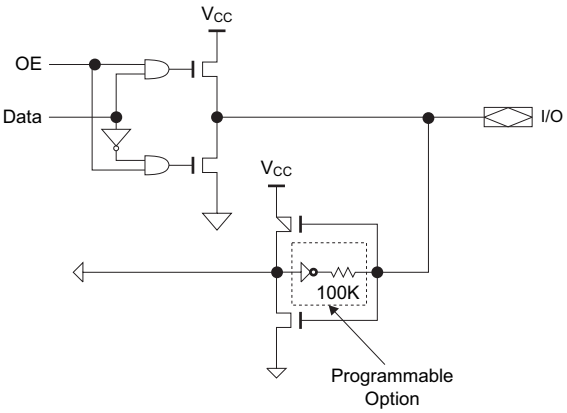


Figure 4-2. I/O Diagram



5. Speed/Power Management

The ATF1502AS(L) has several built-in speed and power management features. The ATF1502AS(L) contains circuitry which automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 50MHz. This feature may be selected as a design option.

To further reduce power, each ATF1502AS(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

The ATF1502AS(L) also has an optional power-down mode. In this mode, current drops to below 10mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output; however, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with reduced-power bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH}, and t_{SEXP}.

The ATF1502AS(L) macrocell also has an option whereby the power can be reduced on a per-macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

6. Design Software Support

ATF1502AS(L) designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages and formats.

7. Power-up Reset

The ATF1502AS(L) is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

- The V_{CC} rise must be monotonic,
- After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
- The clock must remain stable during T_D.

The ATF1502AS(L) has two options for the hysteresis about the reset level, V_{RST}, Small and Large. During the fitting process, users may configure the device with the Power-up Reset hysteresis set to Large or Small. Atmel POF2JED users may select the Large option by including the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

- If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred micro amps as well.

8. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1502AS(L) fuse patterns. Once programmed, fuse verify is inhibited; however, the 16-bit User Signature remains accessible.

9. Programming

ATF1502AS(L) devices are In-System Programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1502AS(L) via the PC. ISP is performed by using either a download cable, a comparable board tester, or a simple microprocessor interface.

When using the ISP hardware or software to program the ATF1502AS(L) devices, four I/O pins must be reserved for the JTAG interface. However, the logic features that the macrocells have associated with these I/O pins are still available to the design for burned logic functions.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by Atmel-provided software utilities.

ATF1502AS(L) devices can also be programmed using standard third-party programmers. With a third-party programmer, the JTAG ISP port can be disabled, thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

10. ISP Programming Protection

The ATF1502AS(L) has a special feature which locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition, the pin-keeper option preserves the previous state of the input and I/O PMS during programming.

All ATF1502AS(L) devices are initially shipped in the erased state, thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

Table 11-4. AC Characteristics[11.9] (Continued)

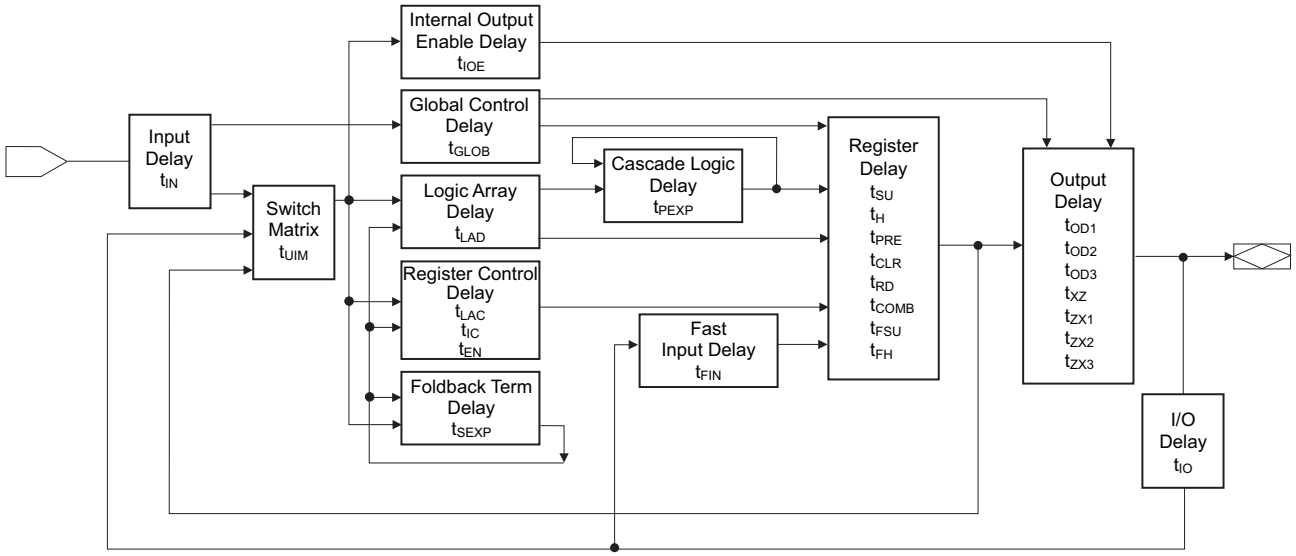
Symbol	Parameter	-7		-10		-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35pF)		4.0		5.0		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35pF)		4.5		5.5		10	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35pF)		9		9		12	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5pF)		4		5		8	ns
t_{SU}	Register Setup Time	3		3		6		ns
t_H	Register Hold Time	2		3		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		5		ns
t_{RD}	Register Delay		1		2		2	ns
t_{COMB}	Combinatorial Delay		1		2		2	ns
t_{IC}	Array Clock Delay		3		5		8	ns
t_{EN}	Register Enable Time		3		5		8	ns
t_{GLOB}	Global Control Delay		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		6	ns
t_{CLR}	Register Clear Time		2		3		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2	ns
t_{RPA}	Reduced-power Adder[2]		10		11		15	ns

Notes: 1. See ordering information for valid part numbers.

2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

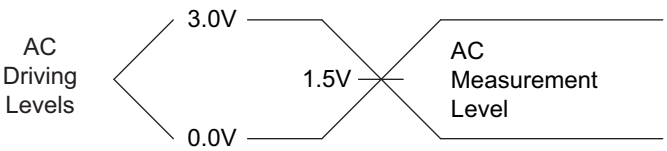
11.6 Timing Model

Figure 11-1. Timing Model



11.7 Input Test Waveforms and Measurement Levels

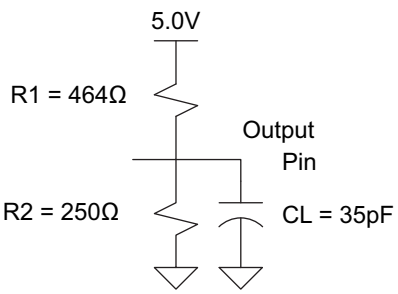
Figure 11-2. Input Test Waveforms and Measurement Levels



Note: t_R, t_F = 1.5ns typical

11.8 Output AC Test Loads

Figure 11-3. Output AC Test Loads



11.9 Power-down Mode

The ATF1502AS(L) includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 5mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure the pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using the power-down pin may not use the PD pin logic array input; however, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

11.9.1 Power-down AC Characteristics

Table 11-5. Power-down AC Characteristics[1][2]

Symbol	Parameter	-7		-10		-25		Units
		Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O before PD High	7		10		25		ns
t_{GVDH}	Valid OE[2] before PD High	7		10		25		ns
t_{CVDH}	Valid Clock[2] before PD High	7		10		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		35	ns
t_{DHGX}	OE[2] Don't Care after PD High		12		15		35	ns
t_{DHCX}	Clock[2] Don't Care after PD High		12		15		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

12. JTAG-BST/ISP Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1502AS(L). The boundary-scan technique involves the inclusion of a shift-register stage (contained in a Boundary-Scan Cell) adjacent to each component so signals at component boundaries can be controlled and observed using scan testing methods. Each input pin and I/O pin has its own Boundary-Scan Cell (BSC) to support Boundary-Scan Testing (BST). The ATF1502AS(L) does not include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include:

- SAMPLE/PRELOAD
- EXTEST
- BYPASS
- IDCODE
- HIGHZ

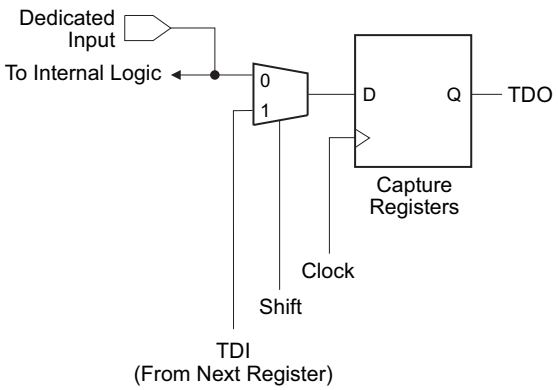
The ATF1502AS(L) ISP can fully be described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1502AS(L) programming to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1502AS(L) has the option of using four JTAG-standard I/O pins for BST and ISP purposes. The ATF1502AS(L) is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

13. JTAG Boundary-scan Cell (BSC) Testing

The ATF1502AS(L) contains up to 32 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own BSC in order to support BST as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device, and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells is shown below.

Figure 13-1. BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



Note: 1. The ATF1502AS(L) has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

14. PCI Compliance

The ATF1502AS(L) supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1502AS(L) allows this without contributing to system noise while delivering low output to output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance.

Figure 14-1. PCI Voltage-to-current Curves for +5.0V Signaling in Pull-up Mode

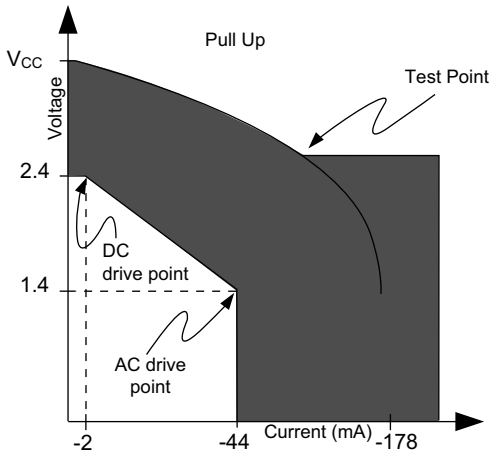


Figure 14-2. PCI Voltage-to-current Curves for +5.0V Signaling in Pull-down Mode

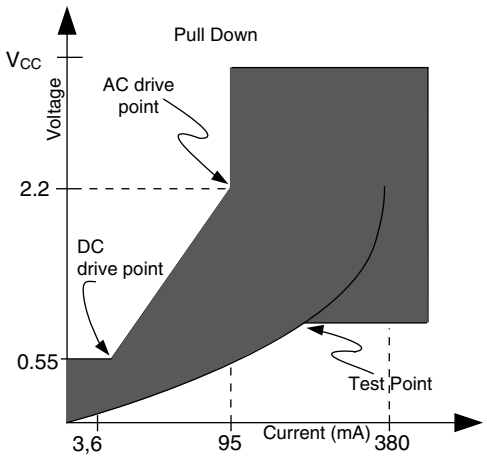


Table 14-1. PCI DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current(1)	V_{IN} = 2.7V		70	µA
I_{IL}	Input Low Leakage Current(1)	V_{IN} = 0.5V		-70	µA
V_{OH}	Output High Voltage	I_{OUT} = -2mA	2.4		V
V_{OL}	Output Low Voltage	I_{OUT} = 3mA, 6mA		0.55	V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance			12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

Note: 1. Leakage current is with pin-keeper off.

Table 14-2. PCI AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching Current High (Test High)	$0 < V_{OUT} \leq 1.4$	-44		mA
		$1.4 < V_{OUT} < 2.4$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A	mA
		$V_{OUT} = 3.1V$		-142	µA
$I_{OL(AC)}$	Switching Current Low (Test Point)	$V_{OUT} > 2.2V$	95		mA
		$2.2 > V_{OUT} > 0$	$V_{OUT}/0.023$		mA
		$0.1 > V_{OUT} > 0$		Equation B	mA
		$V_{OUT} = 0.71$		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$SLEW_R$	Output Rise Slew Rate	0.4V to 2.4V Load	1	5	V/ns
$SLEW_F$	Output Fall Slew Rate	2.4V to 0.4V Load	1	5	V/ns

Notes: 1. Equation A: $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1V$.
2. Equation B: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$.

15. Pinouts

15.1 ATF1502AS(L) Dedicated Pinouts

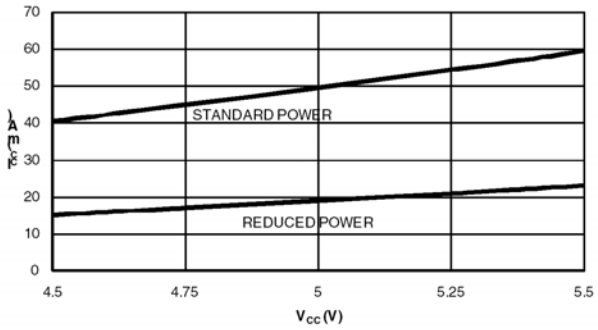
Dedicated Pin	44-lead TQFP	44-lead J-lead
INPUT/OE2/GCLK2	40	2
INPUT/GCLR	39	1
INPUT/OE1	38	44
INPUT/GCLK1	37	43
I/O / GCLK3	35	41
I/O / PD (1,2)	5, 19	11, 25
I/O / TDI (JTAG)	1	7
I/O / TMS (JTAG)	7	13
I/O / TCK (JTAG)	26	32
I/O / TDO (JTAG)	32	38
GND	4, 16, 24, 36	10, 22, 30, 42
V_{CC}	9, 17, 29, 41	3, 15, 23, 35
# of Signal Pins	36	36
# User I/O Pins	32	32

Note:
OE (1, 2) . . . . . Global OE pins
GCLR . . . . . Global Clear pin
GCLK (1, 2, 3) . . . . . Global Clock pins
PD (1, 2) . . . . . Power-down pins
TDI, TMS, TCK, TDO . . . JTAG pins used for boundary-scan testing or in-system programming
GND . . . . . Ground pins
V_{CC} . . . . . V_{CC} pins for the device (+5V)

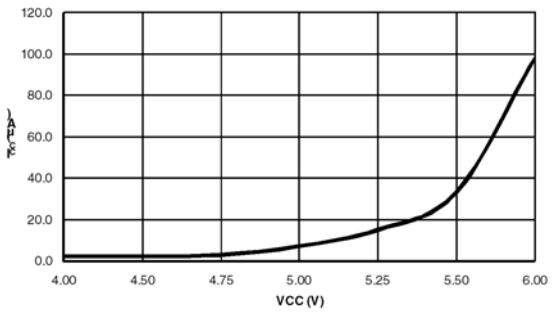
15.2 ATF1502AS(L) I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP
1	A	4	42
2	A	5	43
3	A/**PD1**	6	44
4/**TDI**	A	7	1
5	A	8	2
6	A	9	3
7	A	11	5
8	A	12	6
9/**TMS**	A	13	7
10	A	14	8
11	A	16	10
12	A	17	11
13	A	18	12
14	A	19	13
15	A	20	14
16	A	21	15
17	B	41	35
18	B	40	34
19	B	39	33
20/**TDO**	B	38	32
21	B	37	31
22	B	36	30
23	B	34	28
24	B	33	27
25/**TCK**	B	32	26
26	B	31	25
27	B	29	23
28	B	28	22
29	B	27	21
30	B	26	20
31	B	25	19
32	B	24	18

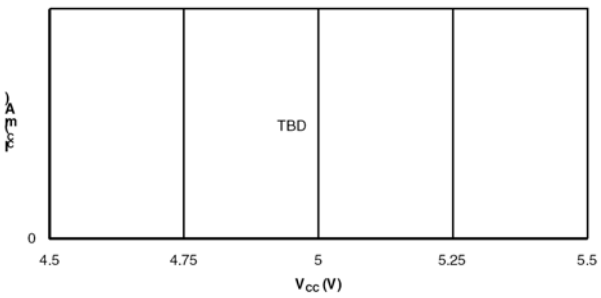
SUPPLY CURRENT VS. SUPPLY VOLTAGE
AS VERSION (T_A = 25°C, F = 0)



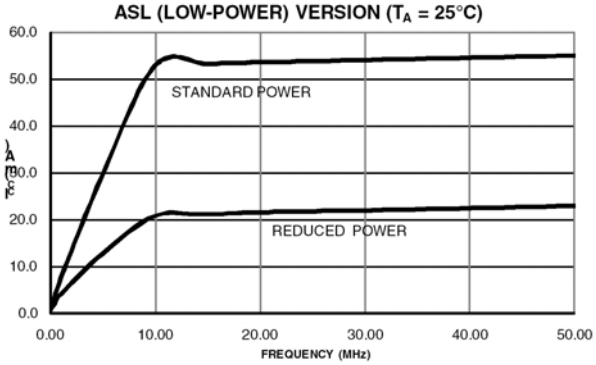
SUPPLY CURRENT VS. SUPPLY VOLTAGE
(T = 25°C, NON-TURBO, BIT6 = 0, BIT 30 = 0)



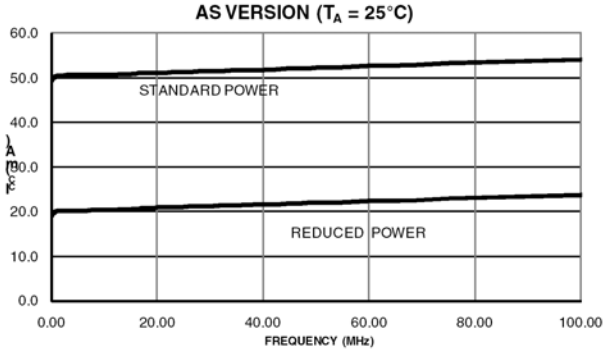
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE (T_A = 25°C, F = 0)



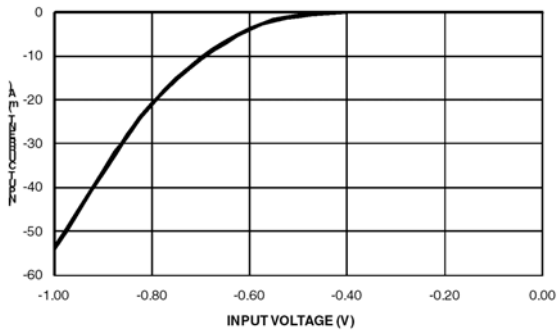
SUPPLY CURRENT VS. FREQUENCY
ASL (LOW-POWER) VERSION (T_A = 25°C)



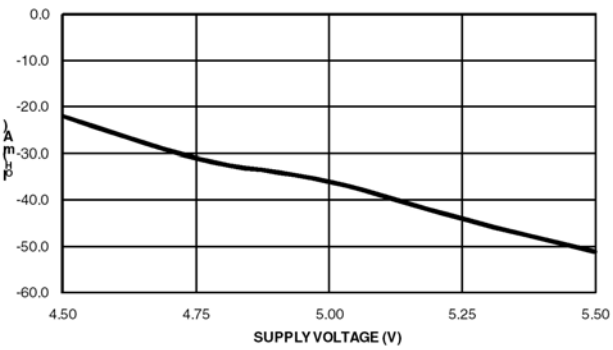
SUPPLY CURRENT VS. FREQUENCY
AS VERSION (T_A = 25°C)



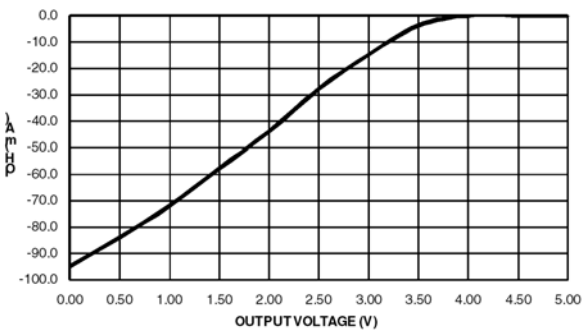
INPUT CLAMP CURRENT VS. INPUT VOLTAGE
(V_{CC} = 5V, T_A = 25°C)



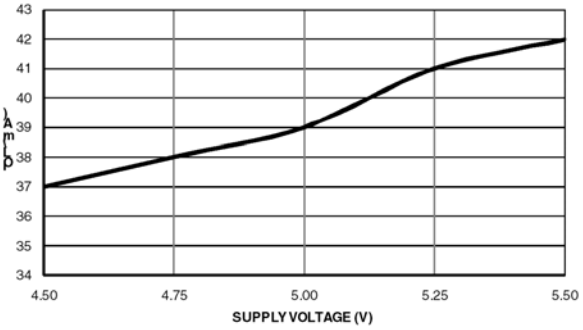
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE
(V_{OH} = 2.4V, T_A = 25°C)



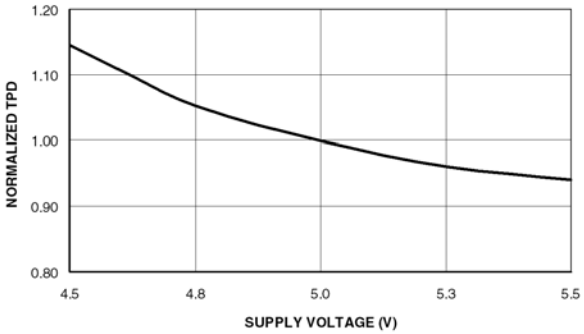
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE
(V_{CC} = 5V, T_A = 25°C)



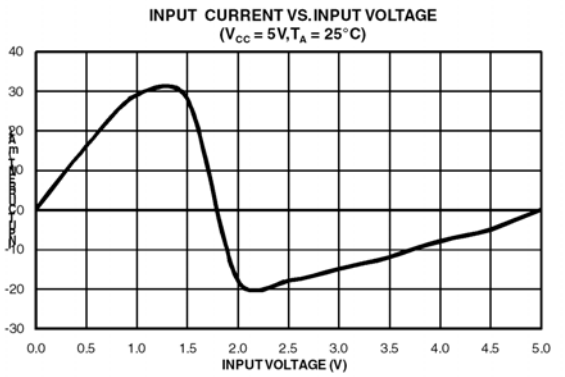
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE
(VOL = 0.5V, T_A = 25°C)



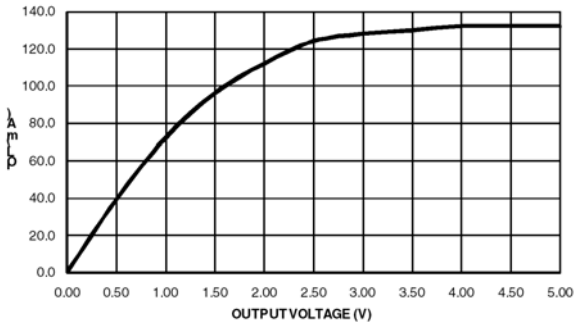
NORMALIZED TPD
VS. SUPPLY VOLTAGE (T_A = 25°C)



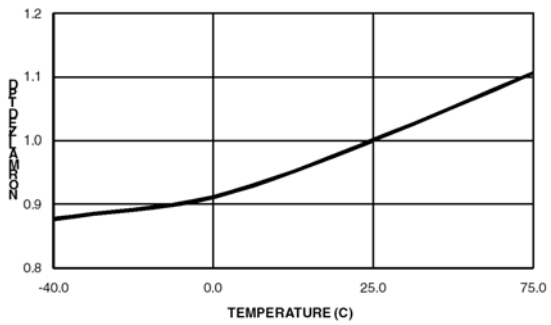
INPUT CURRENT VS. INPUT VOLTAGE
(V_{CC} = 5V, T_A = 25°C)



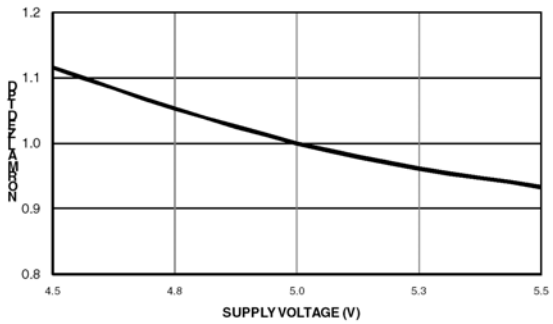
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
(V_{CC} = 5V, T_A = 25°C)



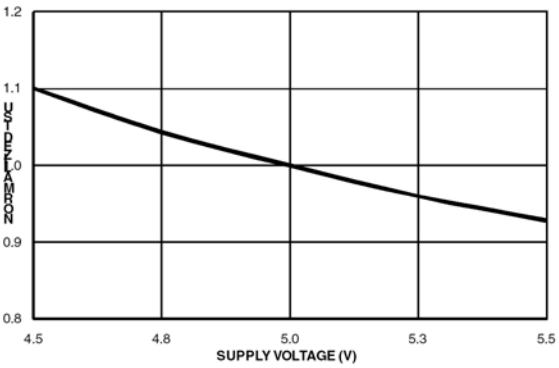
NORMALIZED TPD
VS. TEMPERATURE (V_{CC} = 5.0V)



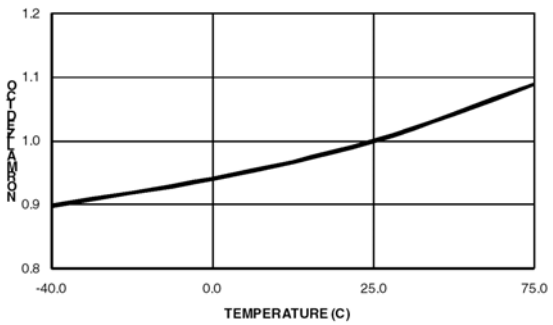
NORMALIZED TCO
VS. SUPPLY VOLTAGE (T_A = 25°C)



NORMALIZED TSU VS. SUPPLY VOLTAGE (T_A = 25°C)



NORMALIZED TCO
VS. TEMPERATURE (V_{CC} = 5.0V)



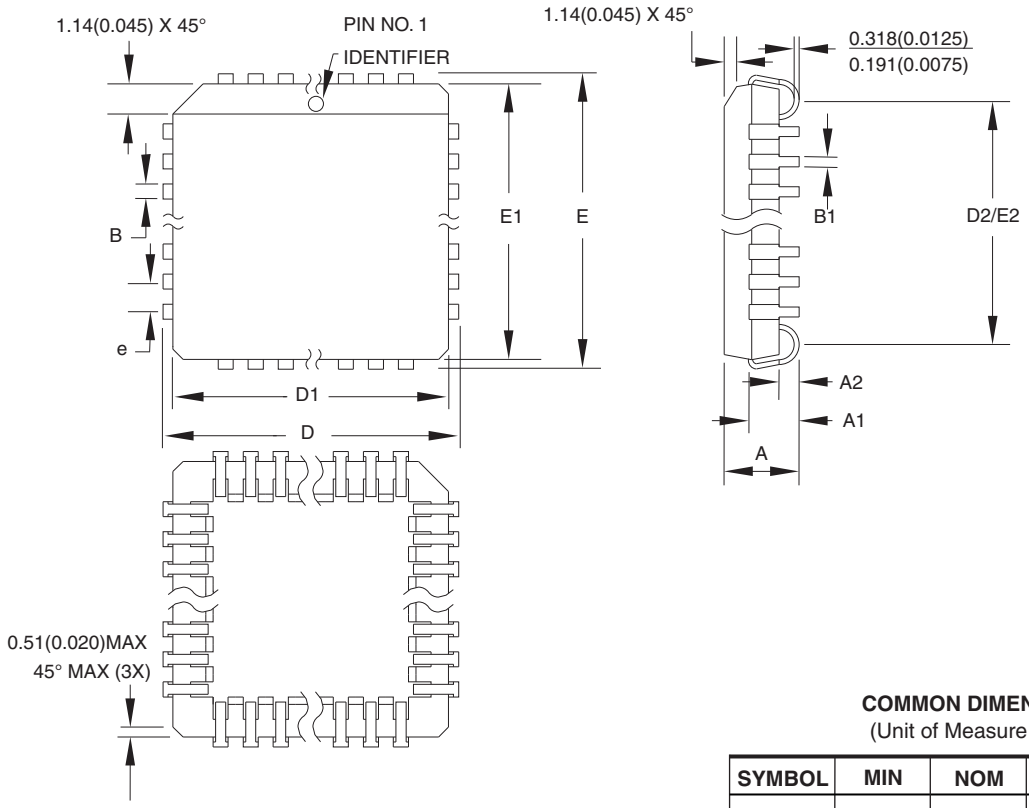
16. Ordering Information

16.1 Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1502AS-7AX44	44A	Commercial (0°C to 70°C)
			ATF1502AS-7JX44	44J	
10	5	125	ATF1502AS-10AU44	44A	Industrial (-40°C to +85°C)
			ATF1502AS-10JU44	44J	
25	13	60	ATF1502ASL-25AU44	44A	Industrial (-40°C to +85°C)
			ATF1502ASL-25JU44	44J	

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack Package (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)

17.2 44J — 44-lead PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

Atmel	TITLE	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

18. Revision History

Revision	Date	Comments
0995L	03/2014	Remove lead based package offering and 15ns speed grade. Update template, logos, and disclaimer page.
0995K	06/2005	Green package options added.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**