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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf8390-i-pt

PIC18F6390/6490/8390/8490

TABLE 1-3: PIC18F8X90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RJ0/SEG32 RJ0 SEG32	62	I/O O	ST Analog	PORTJ is a bidirectional I/O port. Digital I/O. SEG32 output for LCD.
RJ1/SEG33 RJ1 SEG33	61	I/O O	ST Analog	Digital I/O. SEG33 output for LCD.
RJ2/SEG34 RJ2 SEG34	60	I/O O	ST Analog	Digital I/O. SEG34 output for LCD.
RJ3/SEG35 RJ3 SEG35	59	I/O O	ST Analog	Digital I/O. SEG35 output for LCD.
RJ4/SEG39 RJ4 SEG39	39	I/O O	ST Analog	Digital I/O. SEG39 output for LCD.
RJ5/SEG38 RJ5 SEG38	40	I/O O	ST Analog	Digital I/O. SEG38 output for LCD.
RJ6/SEG37 RJ6 SEG37	41	I/O O	ST Analog	Digital I/O. SEG37 output for LCD.
RJ7/SEG36 RJ7 SEG36	42	I/O O	ST Analog	Digital I/O. SEG36 output for LCD.
Vss	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVss	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

2.7.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 2-2) controls several aspects of the device clock's operation, both in full-power operation and in power-managed modes.

The System Clock Select bits, SCS1:SCS0, select the clock source. The available clock sources are the primary clock (defined by the FOSC:FOSC0 Configuration bits), the secondary clock (Timer1 oscillator) and the internal oscillator block. The clock source changes immediately after one or more of the bits is written to, following a brief clock transition interval. The SCS bits are cleared on all forms of Reset.

The Internal Oscillator Frequency Select bits, IRCF2:IRCF0, select the frequency output of the internal oscillator block to drive the device clock. The choices are the INTRC source, the INTOSC source (8 MHz) or one of the frequencies derived from the INTOSC postscaler (31.25 kHz to 4 MHz). If the internal oscillator block is supplying the device clock, changing the states of these bits will have an immediate change on the internal oscillator's output.

When an output frequency of 31 kHz is selected (IRCF2:IRCF0 = 000), users may choose which internal oscillator acts as the source. This is done with the INTSRC bit in the OSCTUNE register (OSCTUNE<7>). Setting this bit selects INTOSC as a 31.25 kHz clock source by enabling the divide-by-256 output of the INTOSC postscaler. Clearing INTSRC selects INTRC (nominally 31 kHz) as the clock source.

This option allows users to select the tunable and more precise INTOSC as a clock source, while maintaining power savings with a very low clock speed. Regardless of the setting of INTSRC, INTRC always remains the clock source for features such as the Watchdog Timer and the Fail-Safe Clock Monitor.

The OSTS, IOFS and T1RUN bits indicate which clock source is currently providing the device clock. The OSTS bit indicates that the Oscillator Start-up Timer has timed out and the primary clock is providing the device clock in primary clock modes. The IOFS bit indicates when the internal oscillator block has stabilized and is providing the device clock in RC Clock modes. The T1RUN bit (T1CON<6>) indicates when the Timer1 oscillator is providing the device clock in secondary clock modes. In power-managed modes, only one of these three bits will be set at any time. If none of these bits are set, the INTRC is providing the clock, or the internal oscillator block has just started and is not yet stable.

The IDLEN bit determines if the device goes into Sleep mode or one of the Idle modes when the SLEEP instruction is executed.

The use of the flag and control bits in the OSCCON register is discussed in more detail in **Section 3.0 "Power-Managed Modes"**.

Note 1: The Timer1 oscillator must be enabled to select the secondary clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 Control register (T1CON<3>). If the Timer1 oscillator is not enabled, then any attempt to select a secondary clock source when executing a SLEEP instruction will be ignored.

2: It is recommended that the Timer1 oscillator be operating and stable before executing the SLEEP instruction, or a very long delay may occur while the Timer1 oscillator starts.

2.7.2 OSCILLATOR TRANSITIONS

PIC18F6390/6490/8390/8490 devices contain circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in **Section 3.1.2 "Entering Power-Managed Modes"**.

2.8 Effects of Power-Managed Modes on the Various Clock Sources

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin, if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the Timer1 oscillator is operating and providing the device clock. The Timer1 oscillator may also run in all power-managed modes if required to clock Timer1 or Timer3.

In internal oscillator modes (RC_RUN and RC_IDLE), the internal oscillator block provides the device clock source. The 31 kHz INTRC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the power-managed mode (see **Section 23.2 “Watchdog Timer (WDT)”** through **Section 23.4 “Fail-Safe Clock Monitor”** for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up). The INTOSC output at 8 MHz may be used directly to clock the device, or may be divided down by the postscaler. The INTOSC output is disabled if the clock is provided directly from the INTRC output.

If the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTRC is required to support WDT operation. The Timer1 oscillator may be operating to support a Real-Time Clock. Other features may be operating that do not require a device clock source (i.e., MSSP slave, INTx pins and others). Peripherals that may add significant current consumption are listed in **Section 26.2 “DC Characteristics: Power-Down and Supply Current”**.

2.9 Power-up Delays

Power-up delays are controlled by two timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 4.5 “Device Reset Timers”**.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up (parameter 33, Table 26-10). It is enabled by clearing (= 0) the PWRTEN Configuration bit.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the HSPLL Oscillator mode is selected, the device is kept in Reset for an additional 2 ms, following the HS mode OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of interval T_{CSD} (parameter 38, Table 26-10) following POR while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTIO modes are used as the primary clock source.

TABLE 2-3: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

Oscillator Mode	OSC1 Pin	OSC2 Pin
RC, INTIO1	Floating, external resistor should pull high	At logic low (clock/4 output)
RCIO, INTIO2	Floating, external resistor should pull high	Configured as PORTA, bit 6
ECIO	Floating, pulled by external clock	Configured as PORTA, bit 6
EC	Floating, pulled by external clock	At logic low (clock/4 output)
LP, XT and HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

Note: See Table 4-2 in **Section 4.0 “Reset”** for time-outs due to Sleep and MCLR Reset.

3.4.2 SEC_IDLE MODE

In SEC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the Timer1 oscillator. This mode is entered from SEC_RUN by setting the IDLEN bit and executing a `SLEEP` instruction. If the device is in another Run mode, set IDLEN first, then set SCS1:SCS0 to '01' and execute `SLEEP`. When the clock source is switched to the Timer1 oscillator, the primary oscillator is shut down, the OSTS bit is cleared and the T1RUN bit is set.

When a wake event occurs, the peripherals continue to be clocked from the Timer1 oscillator. After an interval of TcSD following the wake event, the CPU begins executing code being clocked by the Timer1 oscillator. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run (see Figure 3-8).

Note: The Timer1 oscillator should already be running prior to entering SEC_IDLE mode. If the T1OSCEN bit is not set when the `SLEEP` instruction is executed, the `SLEEP` instruction will be ignored and entry to SEC_IDLE mode will not occur. If the Timer1 oscillator is enabled, but not yet running, peripheral clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.

3.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a `SLEEP` instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute `SLEEP`. Although its value is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. The INTOSC multiplexer may be used to select a higher clock frequency by modifying the IRCF bits before executing the `SLEEP` instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value, or the INTSRC bit is set, the INTOSC output is enabled. The IOFS bit becomes set after the INTOSC output becomes stable after an interval of TIOBST (parameter 39, Table 26-10). Clocks to the peripherals continue while the INTOSC source stabilizes. If the IRCF bits were previously at a non-zero value, or INTSRC was set before the `SLEEP` instruction was executed and the INTOSC source was already stable, the IOFS bit will remain set. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled; the IOFS bit will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TcSD following the wake event, the CPU begins executing code being clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

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EXAMPLE 6-1: READING A FLASH PROGRAM MEMORY WORD

	MOVLW	CODE_ADDR_UPPER	; Load TBLPTR with the base
	MOVWF	TBLPTRU	; address of the word
	MOVLW	CODE_ADDR_HIGH	
	MOVWF	TBLPTRH	
	MOVLW	CODE_ADDR_LOW	
	MOVWF	TBLPTRL	
READ_WORD			
	TBLRD**		; read into TABLAT and increment
	MOVF	TABLAT, W	; get data
	MOVWF	WORD_EVEN	
	TBLRD**		; read into TABLAT and increment
	MOVF	TABLAT, W	; get data
	MOVWF	WORD_ODD	

TABLE 6-2: REGISTERS ASSOCIATED WITH READING PROGRAM FLASH MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
TBLPTRU	—	—	bit 21	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)					59
TBLPTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)								59
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								59
TABLAT	Program Memory Table Latch								59

Legend: — = unimplemented, read as '0'. Shaded cells are not used during Flash access.

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REGISTER 8-3: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **INT2IP:** INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 6 **INT1IP:** INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 5 **INT3IE:** INT3 External Interrupt Enable bit
1 = Enables the INT3 external interrupt
0 = Disables the INT3 external interrupt
- bit 4 **INT2IE:** INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt
- bit 3 **INT1IE:** INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt
- bit 2 **INT3IF:** INT3 External Interrupt Flag bit
1 = The INT3 external interrupt occurred (must be cleared in software)
0 = The INT3 external interrupt did not occur
- bit 1 **INT2IF:** INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur
- bit 0 **INT1IF:** INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global interrupt enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

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REGISTER 8-8: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIE	CMIE	—	—	BCLIE	HLVDIE	TMR3IE	CCP2IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **OSCFIE:** Oscillator Fail Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 6 **CMIE:** Comparator Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **BCL1IE:** Bus Collision Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 2 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 1 **TMR3IE:** TMR3 Overflow Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit

1 = Enabled

0 = Disabled

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TABLE 9-12: PORTF FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	Buffer	Description
RF0/AN5/SEG18	RF0	0	O	DIG	LATF<0> data output. Output is unaffected by analog input; disabled when LCD segment is enabled.
		1	I	ST	PORTF<0> data input. Reads '0' on POR.
	AN5	1	I	ANA	A/D input channel 5. Default configuration on POR.
	SEG18	x	O	ANA	Segment 18 analog output for LCD.
RF1/AN6/C2OUT/SEG19	RF1	0	O	DIG	LATF<1> data output. Output is unaffected by analog input; disabled when LCD segment is enabled.
		1	I	ST	PORTF<1> data input. Reads '0' on POR.
	AN6	1	I	ANA	A/D input channel 6. Default configuration on POR.
	C2OUT	0	O	DIG	Comparator 2 output; takes priority over port data.
	SEG19	x	O	ANA	Segment 19 analog output for LCD.
RF2/AN7/C1OUT/SEG20	RF2	0	O	DIG	LATF<2> data output. Output is unaffected by analog input; disabled when LCD segment is enabled.
		1	I	ST	PORTF<2> data input. Reads '0' on POR.
	AN7	1	I	ANA	A/D input channel 7. Default configuration on POR.
	C1OUT	0	O	TTL	Comparator 1 output; takes priority over port data.
	SEG20	x	O	ANA	Segment 20 analog output for LCD.
RF3/AN8/SEG21	RF3	0	O	DIG	LATF<3> data output. Output is unaffected by analog input; disabled when LCD segment is enabled.
		1	I	ST	PORTF<3> data input. Reads '0' on POR.
	AN8	1	I	ANA	A/D input channel 8 and Comparator C2+ input. Default input configuration on POR; not affected by analog output.
	SEG21	x	O	ANA	Segment 21 analog output for LCD.
RF4/AN9/SEG22	RF4	0	O	DIG	LATF<4> data output. Output is unaffected by analog input; disabled when LCD segment is enabled.
		1	I	ST	PORTF<4> data input. Reads '0' on POR.
	AN9	1	I	ANA	A/D input channel 9 and Comparator C2- input. Default input configuration on POR; does not affect digital output.
	SEG22	x	O	ANA	Segment 22 analog output for LCD.
RF5/AN10/CVREF/SEG23	RF5	0	O	DIG	LATF<5> data output. Output unaffected by analog input; disabled when either LCD segment or CVREF is enabled.
		1	I	ST	PORTF<5> data input. Reads '0' on POR.
	AN10	1	I	ANA	A/D input channel 10 and Comparator C1+ input. Default input configuration on POR.
	CVREF	0	O	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
	SEG23	x	O	ANA	Segment 23 analog output for LCD.
RF6/AN11/SEG24	RF6	0	O	DIG	LATF<6> data output. Output is unaffected by analog input; disabled when LCD segment is enabled.
		1	I	ST	PORTF<6> data input. Reads '0' on POR.
	AN11	1	I	ANA	A/D input channel 11 and Comparator C1- input. Default input configuration on POR; does not affect digital output.
	SEG24	x	O	ANA	Segment 24 analog output for LCD.
RF7/ \overline{SS} /SEG25	RF7	0	O	DIG	LATF<7> data output; disabled when LCD segment is enabled.
		1	I	ST	PORTF<7> data input.
	\overline{SS}	1	I	TTL	Slave select input for MSSP module.
	SEG25	x	O	ANA	Segment 25 analog output for LCD.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

9.7 PORTG, TRISG and LATG Registers

PORTG is a 6-bit wide, bidirectional port. The corresponding Data Direction register is TRISG. Setting a TRISG bit (= 1) will make the corresponding PORTG pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISG bit (= 0) will make the corresponding PORTG pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATG) is also memory mapped. Read-modify-write operations on the LATG register read and write the latched output value for PORTG.

PORTG is multiplexed with both USART and LCD functions (Table 9-14). PORTG pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTG pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings. The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register without concern due to peripheral overrides.

PORTG<4:0> are also multiplexed with LCD segment drives controlled by bits in the LCDSE3 register. I/O port functions are only available when the segments are disabled.

The sixth pin of PORTG ($\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$) is an input only pin. Its operation is controlled by the MCLRE Configuration bit. When selected as a port pin (MCLRE = 0), it functions as a digital input only pin; as such, it does not have TRIS or LAT bits associated with its operation. Otherwise, it functions as the device's Master Clear input. In either configuration, RG5 also functions as the programming voltage input during programming.

Note: On a Power-on Reset, RG5 is enabled as a digital input only if Master Clear functionality is disabled. All other 5 pins are configured as digital inputs.

EXAMPLE 9-7: INITIALIZING PORTG

```
CLRF    PORTG    ; Initialize PORTG by
                  ; clearing output
                  ; data latches
CLRF    LATG     ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW   0x04     ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISG    ; Set RG1:RG0 as outputs
                  ; RG2 as input
                  ; RG4:RG3 as inputs
```

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TABLE 9-18: PORTJ FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	Buffer	Description
RJ0/SEG32	RJ0	0	O	DIG	LATJ<0> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<0> data input.
	SEG32	x	O	ANA	Segment 32 analog output for LCD.
RJ1/SEG33	RJ1	0	O	DIG	LATJ<1> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<1> data input.
	SEG33	x	O	ANA	Segment 33 analog output for LCD.
RJ2/SEG34	RJ2	0	O	DIG	LATJ<2> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<2> data input.
	SEG34	x	O	ANA	Segment 34 analog output for LCD.
RJ3/SEG35	RJ3	0	O	DIG	LATJ<3> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<3> data input.
	SEG35	x	O	ANA	Segment 35 analog output for LCD.
RJ4/SEG39	RJ4	0	O	DIG	LATJ<4> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<4> data input.
	SEG39	x	O	ANA	Segment 39 analog output for LCD.
RJ5/SEG38	RJ5	0	O	DIG	LATJ<5> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<5> data input.
	SEG38	x	O	ANA	Segment 38 analog output for LCD.
RJ6/SEG37	RJ6	0	O	DIG	LATJ<6> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<6> data input.
	SEG37	x	O	ANA	Segment 37 analog output for LCD.
RJ7/SEG36	RJ7	0	O	DIG	LATJ<7> data output; disabled when LCD segment enabled.
		1	I	ST	PORTJ<7> data input.
	SEG36	x	O	ANA	Segment 36 analog output for LCD.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 9-19: SUMMARY OF REGISTERS ASSOCIATED WITH PORTJ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
PORTJ	Read PORTJ pin/Write PORTJ Data Latch								62
LATJ	LATJ Data Output Register								62
TRISJ	PORTJ Data Direction Register								62
LCDSE4	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	64

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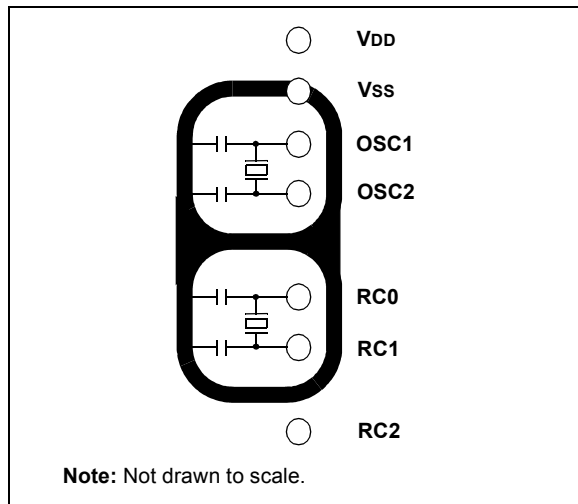
11.3.3 TIMER1 OSCILLATOR LAYOUT CONSIDERATIONS

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 11-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than VSS or VDD.

If a high-speed circuit must be located near the oscillator (such as the CCP1 pin in Output Compare or PWM mode, or the primary oscillator using the OSC2 pin), a grounded guard ring around the oscillator circuit, as shown in Figure 11-4, may be helpful when used on a single sided PCB or in addition to a ground plane.

FIGURE 11-4: OSCILLATOR CIRCUIT WITH GROUNDED GUARD RING



11.4 Timer1 Interrupt

The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The Timer1 interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled or disabled by setting or clearing the Timer1 Interrupt Enable bit, TMR1IE (PIE1<0>).

11.5 Resetting Timer1 Using the CCP Special Event Trigger

If either of the CCP modules is configured in Compare mode to generate a Special Event Trigger (CCP1M3:CCP1M0 or CCP2M3:CCP2M0 = 1011), this signal will reset Timer1. The trigger from CCP2 will also start an A/D conversion if the A/D module is enabled (see Section 14.3.4 “Special Event Trigger” for more information.).

The module must be configured as either a timer or a synchronous counter to take advantage of this feature. When used this way, the CCPRH:CCPRL register pair effectively becomes a period register for Timer1.

If Timer1 is running in Asynchronous Counter mode, this Reset operation may not work.

In the event that a write to Timer1 coincides with a Special Event Trigger, the write operation will take precedence.

Note: The Special Event Triggers from the CCP2 module will not set the TMR1IF interrupt flag bit (PIR1<0>).

11.6 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in Section 11.3 “Timer1 Oscillator”, above) gives users the option to include RTC functionality to their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

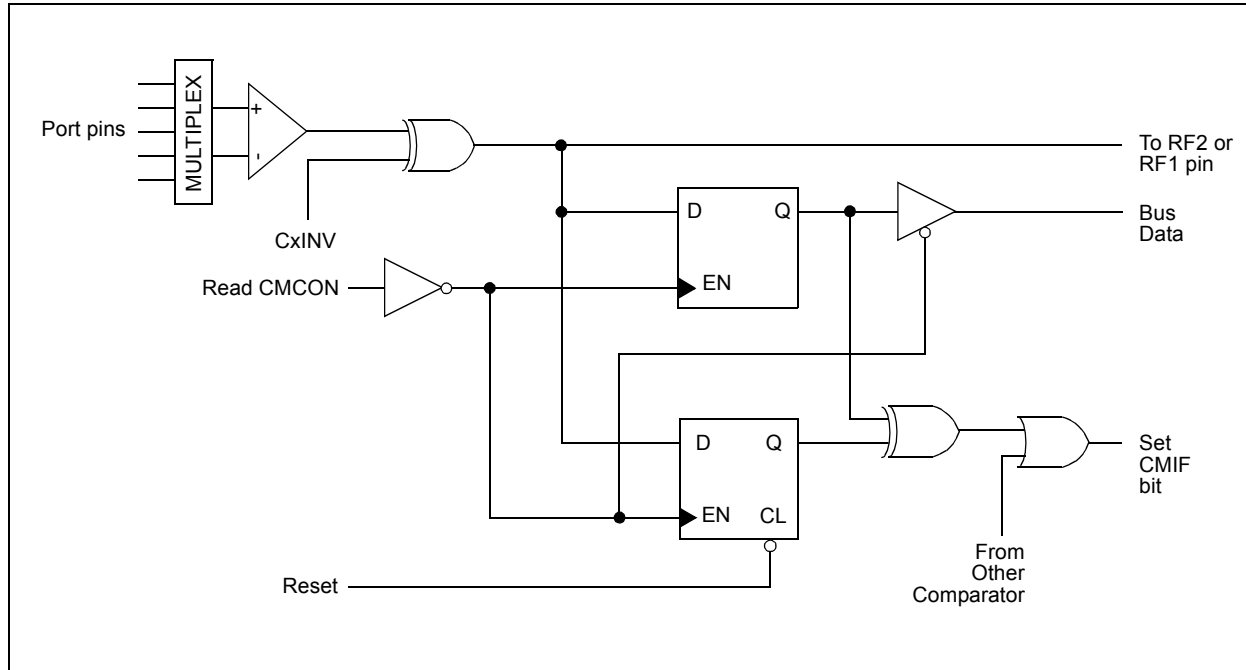
The application code routine, *RTCisr*, shown in Example 11-1, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow, triggers the interrupt and calls the routine, which increments the seconds counter by one; additional counters for minutes and hours are incremented as the previous counter overflows.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it. The simplest method is to set the Most Significant bit of TMR1H with a BSF instruction. Note that the TMR1L register is never preloaded or altered; doing so may introduce cumulative error over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (PIE1<0> = 1), as shown in the routine, *RTCinit*. The Timer1 oscillator must also be enabled and running at all times.

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FIGURE 19-3: COMPARATOR OUTPUT BLOCK DIAGRAM



19.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that occurred. The CMIF bit (PIR2<6>) is the Comparator Interrupt Flag. The CMIF bit must be reset by clearing it. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

Both the CMIE bit (PIE2<6>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit (INTCON<7>) must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR2<6>) interrupt flag may not get set.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of CMCON will end the mismatch condition.
- Clear flag bit, CMIF.

A mismatch condition will continue to set flag bit, CMIF. Reading CMCON will end the mismatch condition and allow flag bit, CMIF, to be cleared.

19.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake-up the device from Sleep mode, when enabled. While the comparator is powered up, higher Sleep currents than shown in the power-down current specification will occur. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in Sleep mode, turn off the comparators (CM2:CM0 = 111) before entering Sleep. If the device wakes up from Sleep, the contents of the CMCON register are not affected.

19.8 Effects of a Reset

A device Reset forces the CMCON register to its Reset state, causing the comparator module to be in the Comparator Reset mode (CM2:CM0 = 000). This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at Reset time. The comparators are powered down during the Reset interval.

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TABLE 22-2: LCDDATA REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS

Segments	COM Lines			
	0	1	2	3
0 through 7	LCDDATA0	LCDDATA6	LCDDATA12	LCDDATA18
	S00C0:S07C0	S00C1:S07C1	S00C2:S07C2	S00C3:S07C3
8 through 15	LCDDATA1	LCDDATA7	LCDDATA13	LCDDATA19
	S08C0:S15C0	S08C1:S15C1	S08C2:S15C2	S08C3:S15C3
16 through 23	LCDDATA2	LCDDATA8	LCDDATA14	LCDDATA20
	S16C0:S23C0	S16C1:S23C1	S16C2:S23C2	S16C3:S23C3
24 through 31	LCDDATA3	LCDDATA9	LCDDATA15	LCDDATA21
	S24C0:S31C0	S24C1:S31C1	S24C2:S31C2	S24C3:S31C3
32 through 39	LCDDATA4 ⁽¹⁾	LCDDATA10 ⁽¹⁾	LCDDATA16 ⁽¹⁾	LCDDATA22 ⁽¹⁾
	S32C0:S39C0	S32C1:S39C1	S32C2:S39C2	S32C3:S39C3
40 through 47	LCDDATA5 ⁽¹⁾	LCDDATA11 ⁽¹⁾	LCDDATA17 ⁽¹⁾	LCDDATA23 ⁽¹⁾
	S40C0:S47C0	S40C1:S47C1	S40C2:S47C2	S40C3:S47C3

Note 1: These registers are implemented but not used as LCD data registers in 64-pin devices. They may be used as general purpose data memory.

REGISTER 22-4: LCDDATAx: LCD DATAx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n + 7)Cy	S(n + 6)Cy	S(n + 5)Cy	S(n + 4)Cy	S(n + 3)Cy	S(n + 2)Cy	S(n + 1)Cy	S(n)Cy
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

S(n + 7)Cy:S(n)Cy: Pixel On bits

For LCDDATA0 through LCDDATA5: n = (8x), y = 0

For LCDDATA6 through LCDDATA11: n = (8(x - 6)), y = 1

For LCDDATA12 through LCDDATA17: n = (8(x - 12)), y = 2

For LCDDATA18 through LCDDATA23: n = (8(x - 18)), y = 3

1 = Pixel on (dark)

0 = Pixel off (clear)

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BNOV Branch if Not Overflow

Syntax: BNOV n

Operands: $-128 \leq n \leq 127$

Operation: if Overflow bit is '0',
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0101	nnnn	nnnn
------	------	------	------

Description: If the Overflow bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNOV Jump

Before Instruction
PC = address (HERE)

After Instruction
If Overflow = 0;
PC = address (Jump)
If Overflow = 1;
PC = address (HERE + 2)

BNZ Branch if Not Zero

Syntax: BNZ n

Operands: $-128 \leq n \leq 127$

Operation: if Zero bit is '0',
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0001	nnnn	nnnn
------	------	------	------

Description: If the Zero bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNZ Jump

Before Instruction
PC = address (HERE)

After Instruction
If Zero = 0;
PC = address (Jump)
If Zero = 1;
PC = address (HERE + 2)

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POP Pop Top of Return Stack

Syntax: POP

Operands: None

Operation: (TOS) → bit bucket

Status Affected: None

Encoding:

0000	0000	0000	0110
------	------	------	------

Description: The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack.

This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	POP TOS value	No operation

Example:

	POP	
	GOTO	NEW

Before Instruction

TOS	=	0031A2h
Stack (1 level down)	=	014332h

After Instruction

TOS	=	014332h
PC	=	NEW

PUSH Push Top of Return Stack

Syntax: PUSH

Operands: None

Operation: (PC + 2) → TOS

Status Affected: None

Encoding:

0000	0000	0000	0101
------	------	------	------

Description: The PC + 2 is pushed onto the top of the return stack. The previous TOS value is pushed down on the stack.

This instruction allows implementing a software stack by modifying TOS and then pushing it onto the return stack.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	PUSH PC + 2 onto return stack	No operation	No operation

Example:

	PUSH	
--	------	--

Before Instruction

TOS	=	345Ah
PC	=	0124h

After Instruction

PC	=	0126h
TOS	=	0126h
Stack (1 level down)	=	345Ah

24.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB® IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set of the PIC18FXX90 family of devices. This includes the MPLAB C18 C compiler, MPASM assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '0', disabling the extended instruction set and Indexed Literal Offset Addressing mode. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option, or dialog box within the environment, that allows the user to configure the language tool and its settings for the project
- A command line option
- A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.

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26.2 DC Characteristics: Power-Down and Supply Current PIC18F6390/6490/8390/8490 (Industrial) PIC18LF6390/6490/8390/8490 (Industrial) (Continued)

PIC18LF6390/6490/8390/8490 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F6390/6490/8390/8490 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ⁽²⁾						
	PIC18LF6390/6490/8390/8490	13	40	μA	-40°C	VDD = 2.0V	Fosc = 32 kHz (SEC_RUN mode, Timer1 as clock) ⁽⁴⁾
		14	40	μA	+25°C		
		16	40	μA	+80°C		
	PIC18LF6390/6490/8390/8490	34	70	μA	-40°C	VDD = 3.0V	
		31	70	μA	+25°C		
		28	70	μA	+80°C		
	All devices	72	150	μA	-40°C	VDD = 5.0V	
		65	150	μA	+25°C		
		59	150	μA	+80°C		
	PIC18LF6390/6490/8390/8490	5.5	15	μA	-40°C	VDD = 2.0V	Fosc = 32 kHz (SEC_IDLE mode, Timer1 as clock) ⁽⁴⁾
		5.8	15	μA	+25°C		
		6.1	18	μA	+80°C		
	PIC18LF6390/6490/8390/8490	8.2	30	μA	-40°C	VDD = 3.0V	
		8.6	30	μA	+25°C		
		8.8	35	μA	+80°C		
	All devices	13	80	μA	-40°C	VDD = 5.0V	
		13	80	μA	+25°C		
13		85	μA	+80°C			

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;

MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power Timer1 oscillator selected.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

PIC18F6390/6490/8390/8490

26.3 DC Characteristics: PIC18F6390/6490/8390/8490 (Industrial) PIC18LF6390/6490/8390/8490 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D080	VOL	Output Low Voltage I/O Ports	—	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D083		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	—	0.6	V	$I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D090	VOH	Output High Voltage ⁽³⁾ I/O Ports	$V_{DD} - 0.7$	—	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D092		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	$V_{DD} - 0.7$	—	V	$I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D150	VOD	Open-Drain High Voltage	—	8.5	V	RA4 pin
Capacitive Loading Specs on Output Pins						
D100 ⁽⁴⁾	COSC2	OSC2 pin	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	50	pF	To meet the AC Timing Specifications
D102	CB	SCL, SDA	—	400	pF	I ² C™ Specification

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

PIC18F6390/6490/8390/8490

APPENDIX A: REVISION HISTORY

Revision A (July 2004)

Original data sheet for PIC18F6390/6490/8390/8490 devices.

Revision B (August 2004)

Updated preliminary “electrical characteristics” data.

Revision C (November 2007)

Revised I²C™ Slave Mode Timing figure. Updated DC Power-Down and Supply Current table and package drawings.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F6390	PIC18F6490	PIC18F8390	PIC18F8490
Number of Pixels the LCD Driver can Drive	128 (4 x 32)	128 (4 x 32)	192 (4 x 48)	192 (4 x 48)
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Flash Program Memory	8 Kbytes	16 Kbytes	8 Kbytes	16 Kbytes
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

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Reset	51	SUBULNK	341
MCLR Reset, during Power-Managed Modes	51	SUBWFB	331
MCLR Reset, Normal Operation	51	SUBWFB	332
Power-on Reset (POR)	51	SWAPF	332
Programmable Brown-out Reset (BOR)	51	T	
Stack Full Reset	51	T0CON Register	
Stack Underflow Reset	51	PSA Bit	133
Watchdog Timer (WDT) Reset	51	T0CS Bit	132
Resets	281	T0PS2:T0PS0 Bits	133
RETFIE	326	T0SE Bit	132
RETLW	326	Table Pointer Operations (table)	88
RETURN	327	Table Reads	68
Return Address Stack	66	TBLRD	333
Return Stack Pointer (STKPTR)	67	TBLWT	334
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RLCF	327	Timer0	131
RLNCF	328	16-Bit Mode Timer Reads and Writes	132
RRCF	328	Associated Registers	133
RRNCF	329	Clock Source Edge Select (T0SE Bit)	132
S		Clock Source Select (T0CS Bit)	132
SCK	157	Operation	132
SDI	157	Overflow Interrupt	133
SDO	157	Prescaler. <i>See</i> Prescaler, Timer0.	
Serial Clock, SCK	157	Timer1	135
Serial Data In (SDI)	157	16-Bit Read/Write Mode	137
Serial Data Out (SDO)	157	Associated Registers	139
Serial Peripheral Interface. <i>See</i> SPI Mode.		Interrupt	138
SETF	329	Operation	136
Slave Select (SS)	157	Oscillator	135, 137
SLEEP	330	Layout Considerations	138
Sleep		Overflow Interrupt	135
OSC1 and OSC2 Pin States	39	Resetting, Using a Special Event Trigger	
Software Enabled BOR	54	Output (CCP)	138
Software Simulator (MPLAB SIM)	346	TMR1H Register	135
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Special Function Registers	74	Timer2	141
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SPI Mode (MSSP)		Interrupt	142
Associated Registers	165	Operation	141
Bus Mode Compatibility	165	Output	142
Effects of a Reset	165	PR2 Register	153
Enabling SPI I/O	161	TMR2 to PR2 Match Interrupt	153
Master Mode	162	Timer3	143
Master/Slave Connection	161	16-Bit Read/Write Mode	145
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Serial Clock	157	Operation	144
Serial Data In	157	Oscillator	143, 145
Serial Data Out	157	Overflow Interrupt	143, 145
Slave Mode	163	Special Event Trigger (CCP)	145
Slave Select	157	TMR3H Register	143
Slave Select Synchronization	163	TMR3L Register	143
Sleep Operation	165	Timing Diagrams	
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Typical Connection	161	Acknowledge Sequence	190
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SSPOV	187	Asynchronous Transmission	207, 223
SSPOV Status Flag	187	Asynchronous Transmission	
SSPSTAT Register		(Back-to-Back)	207, 223
R/W Bit	170, 171	Automatic Baud Rate Calculation	205
Stack Full/Underflow Resets	68	Auto-Wake-up Bit (WUE) During	
STATUS Register	80	Normal Operation	210
SUBFSR	341	Auto-Wake-up Bit (WUE) During Sleep	210
SUBFWB	330	Baud Rate Generator with Clock Arbitration	184
SUBLW	331	BRG Overflow Sequence	205