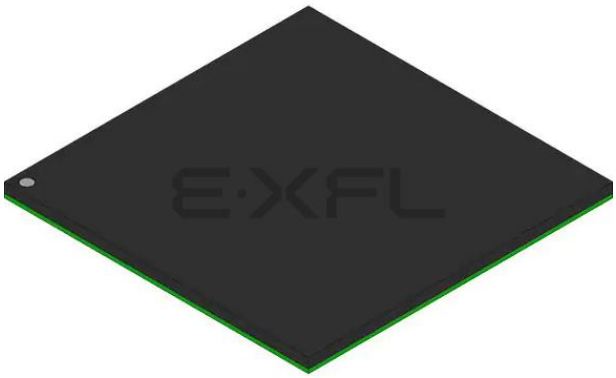

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	94
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53281cvm240

Table 1. MCF532*x* Family Configurations (continued)

Module	MCF5327	MCF5328	MCF53281	MCF5329
LCD Controller	•	•	•	•
SDR/DDR SDRAM Controller	•	•	•	•
USB 2.0 Host	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	—	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•
Fast Ethernet Controller (FEC)	—	•	•	•
Cryptography Hardware Accelerators	—	—	—	•
Embedded Voice-over-IP System Solution	—	—	•	—
FlexCAN 2.0B communication module	—	—	•	•
UARTs	3	3	3	3
I^2C	•	•	•	•
QSPI	•	•	•	•
PWM Module	•	•	•	•
Real Time Clock	•	•	•	•
32-bit DMA Timers	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•
FlexBus External Interface	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•
Package	196 MAPBGA	256 MAPBGA	256 MAPBGA	256 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5327CVM240	MCF5327 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF5328CVM240	MCF5328 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF53281CVM240	MCF53281 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF5329CVM240	MCF5329 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 2 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

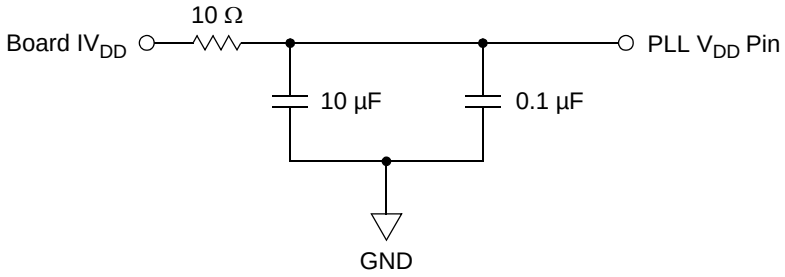


Figure 2. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 3 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

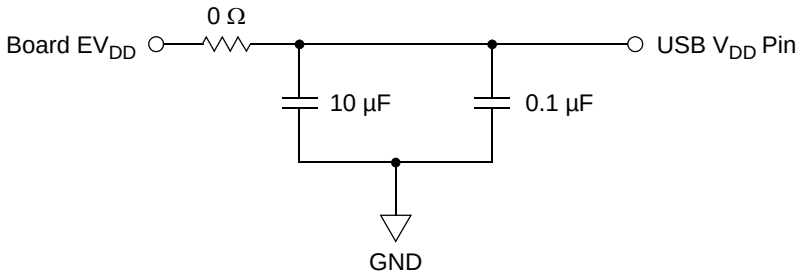


Figure 3. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there is

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
Mode Selection								
$\overline{\text{RCON}}$[2]	—	—	—	I	EVDD	M7	M8	M8
DRAMSEL	—	—	—	I	EVDD	G11	H12	H12
FlexBus								
A[23:22]	—	$\overline{\text{FB\_CS}}$[5:4]	—	O	SDVDD	B11,C11	C13, D13	C13, D13
A[21:16]	—	—	—	O	SDVDD	B12, A12, D11, C12, B13, A13	E13, A14, B14, C14, A15, B15	E13, A14, B14, C14, A15, B15
A[15:14]	—	SD_BA[1:0][3]	—	O	SDVDD	A14, B14	D14, B16	D14, B16
A[13:11]	—	SD_A[13:11][3]	—	O	SDVDD	C13, C14, D12	C15, C16, D15	C15, C16, D15
A10	—	—	—	O	SDVDD	D13	D16	D16
A[9:0]	—	SD_A[9:0][3]	—	O	SDVDD	D14, E11–14, F11–F14, G14	E14–E16, F13–F16, G16– G14	E14–E16, F13–F16, G16– G14
D[31:16]	—	SD_D[31:16][4]	—	I/O	SDVDD	H3–H1, J4–J1, K1, L4, M2, M3, N1, N2, P1, P2, N3	M1–M4, N1–N4, T3, P4, R4, T4, N5, P5, R5, T5	M1–M4, N1–N4, T3, P4, R4, T4, N5, P5, R5, T5
D[15:1]	—	FB_D[31:17][4]	—	I/O	SDVDD	F4–F1, G5–G2, L5, N4, P4, M5, N5, P5, L6	J3–J1, K4–K1, L2, R6, N7, P7, R7, T7, P8, R8	J3–J1, K4–K1, L2, R6, N7, P7, R7, T7, P8, R8
D0[2]	—	FB_D[16][4]	—	I/O	SDVDD	M6	T8	T8
$\overline{\text{BE/BWE}}$[3:0]	PBE[3:0]	$\overline{\text{SD\_DQM}}$[3:0][3]	—	O	SDVDD	H4, P3, G1, M4	L4, P6, L3, N6	L4, P6, L3, N6
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	P6	R9	R9
$\overline{\text{TA}}$[2]	PBUSCTL2	—	—	I	SDVDD	G13	G13	G13
R/$\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	N6	N8	N8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	SDVDD	D2	H4	H4
Chip Selects								
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	O	SDVDD	—	B13, A13	B13, A13
$\overline{\text{FB\_CS}}$[3:1]	PCS[3:1]			O	SDVDD	A11, D10, C10	A12, B12, C12	A12, B12, C12
$\overline{\text{FB\_CS0}}$	—	—	—	O	SDVDD	B10	D12	D12

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
SDRAM Controller								
SD_A10	—	—	—	O	SDVDD	L2	P2	P2
SD_CKE	—	—	—	O	SDVDD	E1	H2	H2
SD_CLK	—	—	—	O	SDVDD	K3	R1	R1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	K2	R2	R2
$\overline{\text{SD\_CS1}}$	—	—	—	O	SDVDD	—	J4	J4
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	E2	H1	H1
SD_DQS3	—	—	—	O	SDVDD	H5	L1	L1
SD_DQS2	—	—	—	O	SDVDD	K6	T6	T6
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	L3	P3	P3
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	M1	R3	R3
SD_SDR_DQS	—	—	—	O	SDVDD	K4	P1	P1
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	D1	H3	H3
External Interrupts Port[5]								
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	J13	J13	J13
$\overline{\text{IRQ6}}$[2]	PIRQ6[2]	USBHOST_ VBUS_EN	—	I	EVDD	—	J14	J14
$\overline{\text{IRQ5}}$[2]	PIRQ5[2]	USBHOST_ VBUS_OC	—	I	EVDD	—	J15	J15
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	SSI_MCLK	—	I	EVDD	L13	J16	J16
$\overline{\text{IRQ3}}$[2]	PIRQ3[2]	—	—	I	EVDD	M14	K14	K14
$\overline{\text{IRQ2}}$[2]	PIRQ2[2]	USB_CLKIN	—	I	EVDD	M13	K15	K15
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	$\overline{\text{DREQ1}}$[2]	SSI_CLKIN	I	EVDD	N13	K16	K16
FEC								
FEC_MDC	PFECI2C3	I2C_SCL[2]	—	O	EVDD	—	C1	C1
FEC_MDIO	PFECI2C2	I2C_SDA[2]	—	I/O	EVDD	—	C2	C2
FEC_TXCLK	PFECH7	—	—	I	EVDD	—	A2	A2
FEC_TXEN	PFECH6	—	—	O	EVDD	—	B2	B2
FEC_TXD0	PFECH5	ULPI_DATA0	—	O	EVDD	—	E4	E4
FEC_COL	PFECH4	ULPI_CLK	—	I	EVDD	—	A8	A8
FEC_RXCLK	PFECH3	ULPI_NXT	—	I	EVDD	—	C8	C8
FEC_RXDV	PFECH2	ULPI_STP	—	I	EVDD	—	D8	D8
FEC_RXD0	PFECH1	ULPI_DATA4	—	I	EVDD	—	C6	C6

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
USB Host & USB On-the-Go								
USBOTG_M	—	—	—	I/O	USB VDD	G12	L15	L15
USBOTG_P	—	—	—	I/O	USB VDD	H13	L16	L16
USBHOST_M	—	—	—	I/O	USB VDD	K13	M15	M15
USBHOST_P	—	—	—	I/O	USB VDD	J12	M16	M16
FlexCAN (MCF53281 & MCF5329 only)								
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA, SSI_RXD, or LCD_D16 for CANRX and I2C_SCL, SSI_TXD, or LCD_D17 for CANTX.								
PWM								
PWM7	PPWM7	—	—	I/O	EVDD	—	H13	H13
PWM5	PPWM5	—	—	I/O	EVDD	—	H14	H14
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	H14	H15	H15
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	J14	H16	H16
SSI								
SSI_MCLK	PSSI4	—	—	I/O	EVDD	—	G4	G4
SSI_BCLK	PSSI3	$\overline{\text{U2CTS}}$	PWM7	I/O	EVDD	—	F4	F4
SSI_FS	PSSI2	$\overline{\text{U2RTS}}$	PWM5	I/O	EVDD	—	G3	G3
SSI_RXD[2]	PSSI1	U2RXD	CANRX	I	EVDD	—	—	G2
SSI_TXD[2]	PSSI0	U2TXD	CANTX	O	EVDD	—	—	G1
SSI_RXD[2]	PSSI1	U2RXD	—	I	EVDD	—	G2	—
SSI_TXD[2]	PSSI0	U2TXD	—	O	EVDD	—	G1	—
I^2C								
I2C_SCL[2]	PFECI2C1	CANTX	U2TXD	I/O	EVDD	—	—	F3
I2C_SDA[2]	PFECI2C0	CANRX	U2RXD	I/O	EVDD	—	—	F2
I2C_SCL[2]	PFECI2C1	—	U2TXD	I/O	EVDD	E3	F3	—
I2C_SDA[2]	PFECI2C0	—	U2RXD	I/O	EVDD	E4	F2	—
DMA								
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.								

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5. Thermal Characteristics

Characteristic		Symbol	256MBGA	196MBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	37[1,2]	42[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	38[1,2]	°C/W
Junction to board	—	θ_{JB}	27[3]	32[3]	°C/W
Junction to case	—	θ_{JC}	16[4]	19[4]	°C/W
Junction to top of package	—	Ψ_{jt}	4[1,5]	5[1,5]	°C/W
Maximum operating junction temperature	—	T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} – 0.35 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 8. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488 x 10^{-6} 163 x 10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF

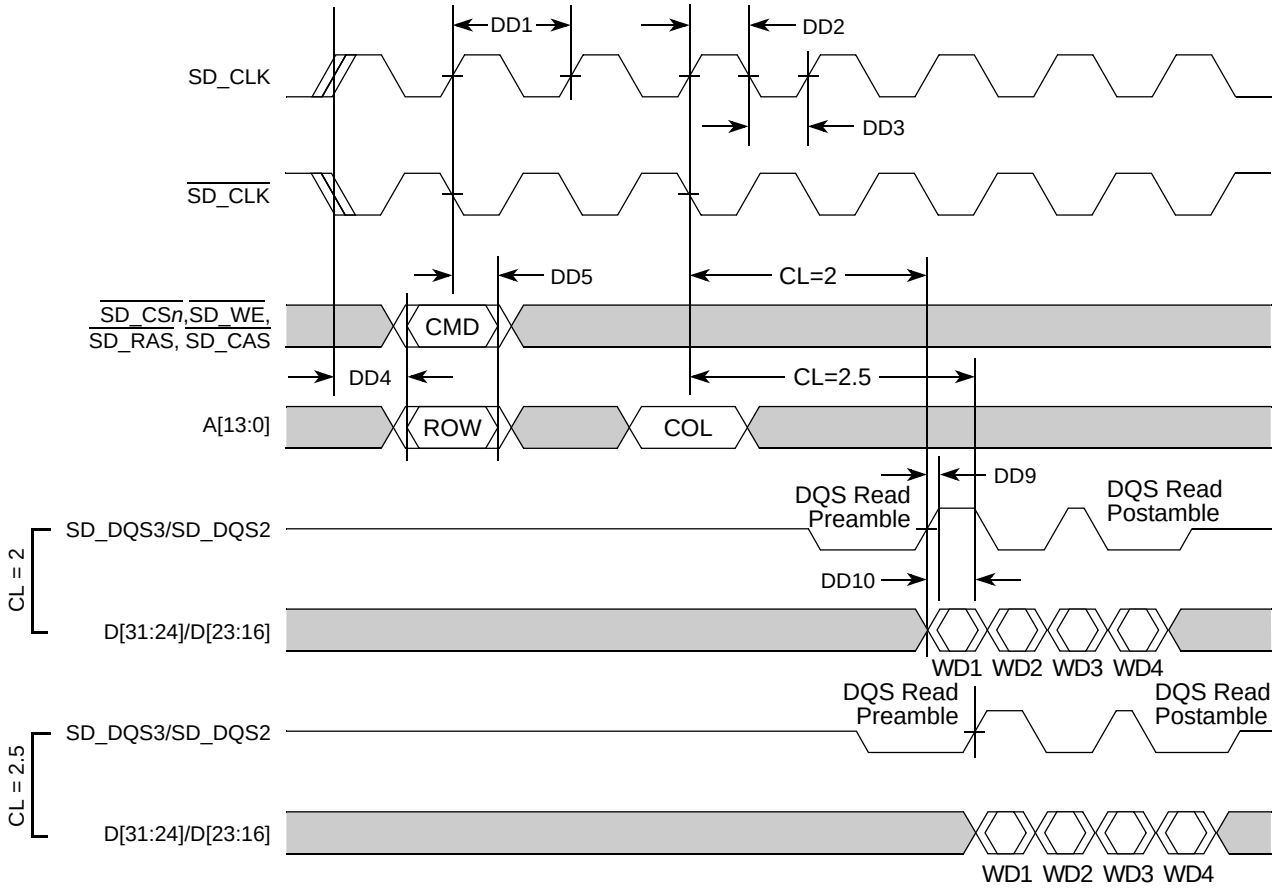


Figure 12. DDR Read Timing

5.8 General Purpose I/O Timing

Table 12. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, FlexCAN, and Timer pins.

5.10 LCD Controller Timing Specifications

This sections lists the timing specifications for the LCD Controller.

Table 14. LCD_LSCLK Timing

Num	Parameter	Minimum	Maximum	Unit
T1	LCD_LSCLK Period	25	2000	ns
T2	Pixel data setup time	11	—	ns
T3	Pixel data up time	11	—	ns

Note: The pixel clock is equal to LCD_LSCLK / (PCD + 1). When it is in CSTN, TFT or monochrome mode with bus width is set and LCD_LSCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, LCD_LSCLK is equal to the pixel clock divided by bus width. The polarity of LCD_LSCLK and LCD_LD signals can also be programmed.

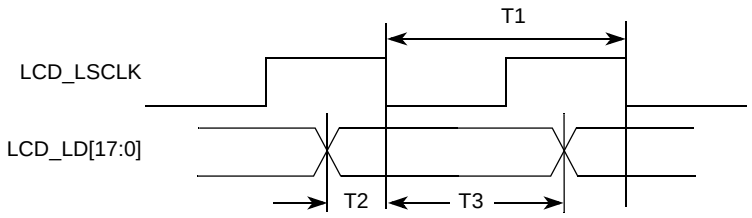


Figure 15. LCD_LSCLK to LCD_LD[17:0] timing diagram

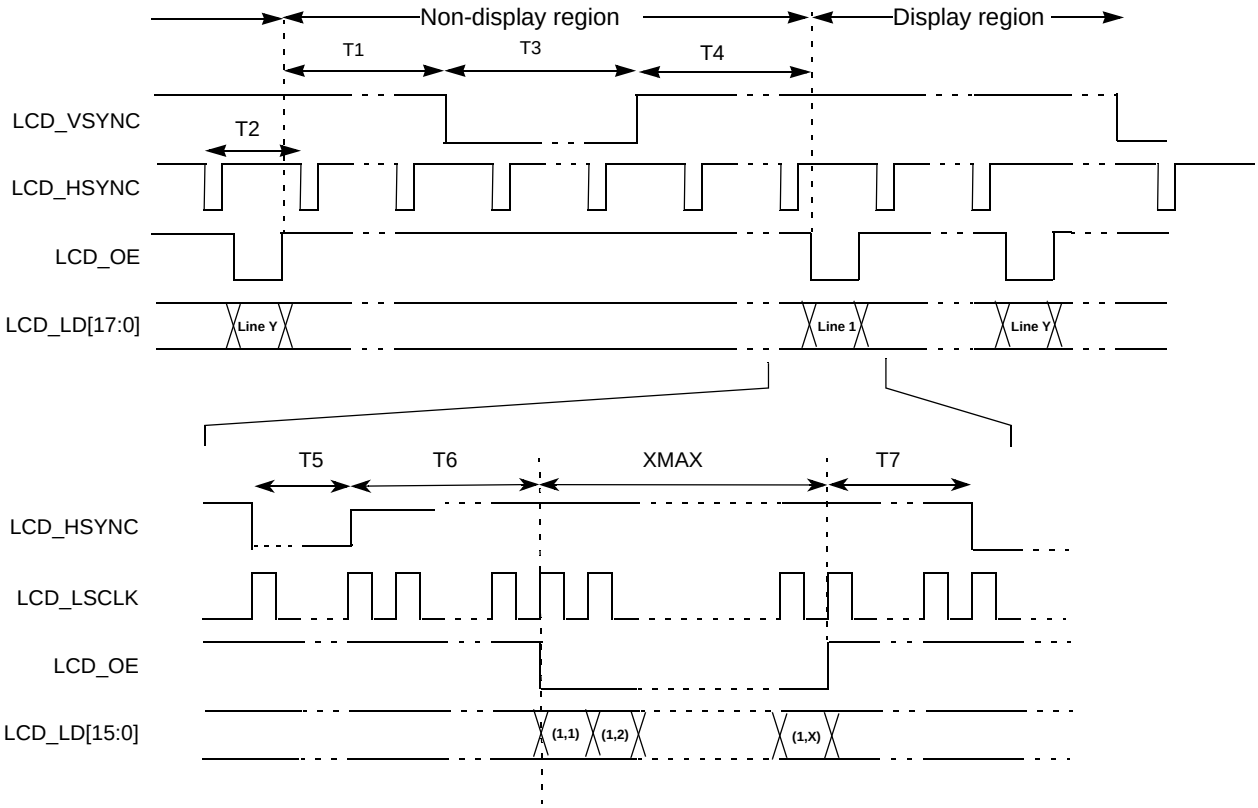


Figure 16. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 16. Sharp TFT Panel Timing

Num	Description	Minimum	Value	Unit
T1	LCD_SPL/LCD_SPR pulse width	—	1	Ts
T2	End of LCD_LD of line to beginning of LCD_HSYNC	1	HWAIT1+1	Ts
T3	End of LCD_HSYNC to beginning of LCD_LD of line	4	HWAIT2 + 4	Ts
T4	LCD_CLS rise delay from end of LCD_LD of line	3	CLS_RISE_DELAY+1	Ts
T5	LCD_CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	LCD_PS rise delay from LCD_CLS negation	0	PS_RISE_DELAY	Ts
T7	LCD_REV toggle delay from last LCD_LD of line	1	REV_TOGGLE_DELAY+1	Ts

Note: Falling of LCD_SPL/LCD_SPR aligns with first LCD_LD of line.
Note: Falling of LCD_PS aligns with rising edge of LCD_CLS.
Note: LCD_REV toggles in every LCD_HSYN period.

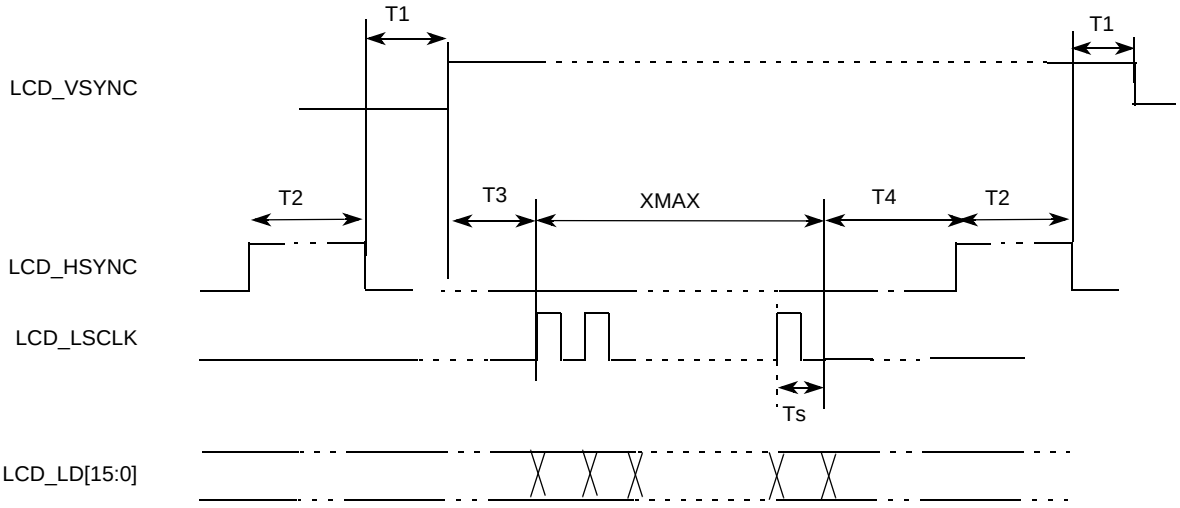


Figure 18. Non-TFT Mode Panel Timing

Table 17. Non-TFT Mode Panel Timing

Num	Description	Minimum	Value	Unit
T1	LCD_HSYNC to LCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	LCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	LCD_VSYNC to LCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	LCD_LSCLK to LCD_HSYNC	1	HWAIT1 + 1	Tpix

Note: Ts is the LCD_LSCLK period while Tpix is the pixel clock period. LCD_VSYNC, LCD_HSYNC and LCD_LSCLK can be programmed as active high or active low. In Figure 18, all three signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

Table 19. SSI Timing – Master Modes[1] (continued)

Num	Description	Symbol	Min	Max	Units
S6	SSI_BCLK to SSI_FS output invalid		-2	—	ns
S7	SSI_BCLK to SSI_TXD valid		—	15	ns
S8	SSI_BCLK to SSI_TXD invalid / high impedence		-4	—	ns
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		15	—	ns
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 20. SSI Timing – Slave Modes[1]

Num	Description	Symbol	Min	Max	Units
S11	SSI_BCLK cycle time	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S12	SSI_BCLK pulse width high/low		45%	55%	t_{BCLK}
S13	SSI_FS input setup before SSI_BCLK		10	—	ns
S14	SSI_FS input hold after SSI_BCLK		3	—	ns
S15	SSI_BCLK to SSI_TXD/SSI_FS output valid		—	15	ns
S16	SSI_BCLK to SSI_TXD/SSI_FS output invalid/high impedence		-2	—	ns
S17	SSI_RXD setup before SSI_BCLK		10	—	ns
S18	SSI_RXD hold after SSI_BCLK		3	—	ns

1 All timings specified with a capactive load of 25pF.

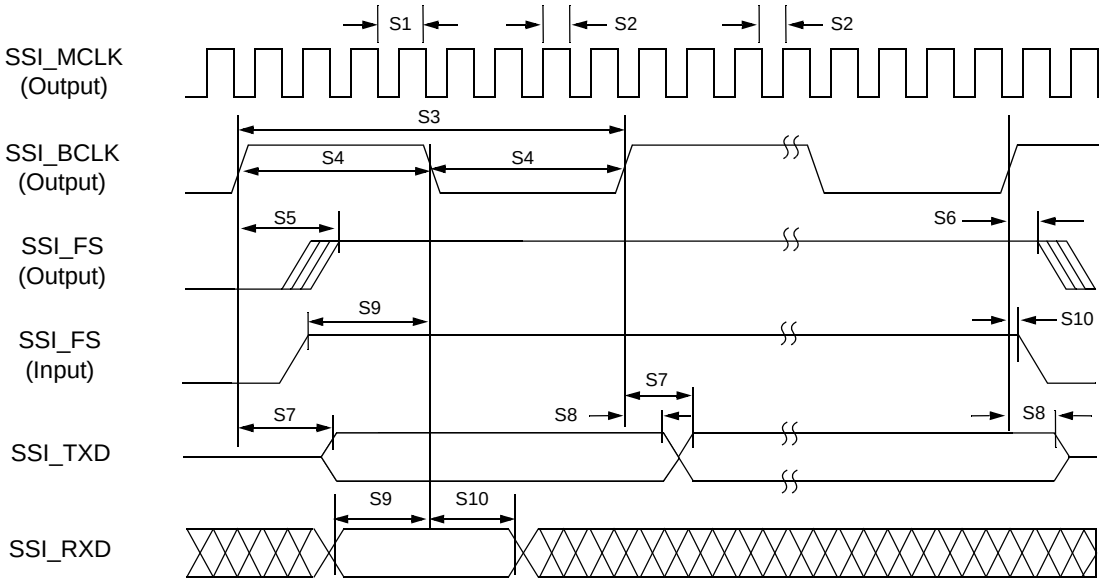


Figure 20. SSI Timing – Master Modes

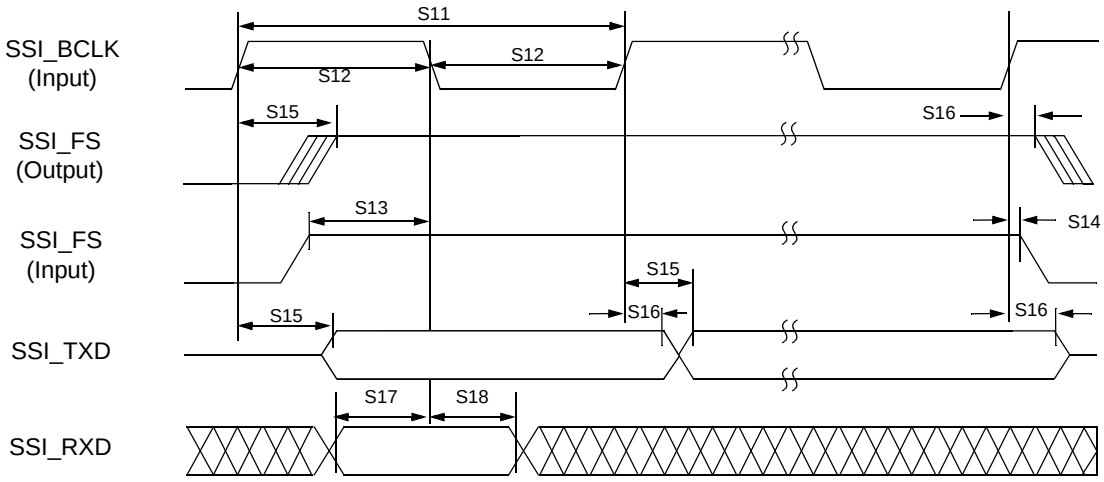


Figure 21. SSI Timing – Slave Modes

5.14 I²C Input/Output Timing Specifications

Table 21 lists specifications for the I²C input timing parameters shown in Figure 22.

Table 21. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

Table 21. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 22 lists specifications for the I²C output timing parameters shown in Figure 22.

Table 22. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 22. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 22 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 22 shows timing for the values in Table 22 and Table 21.

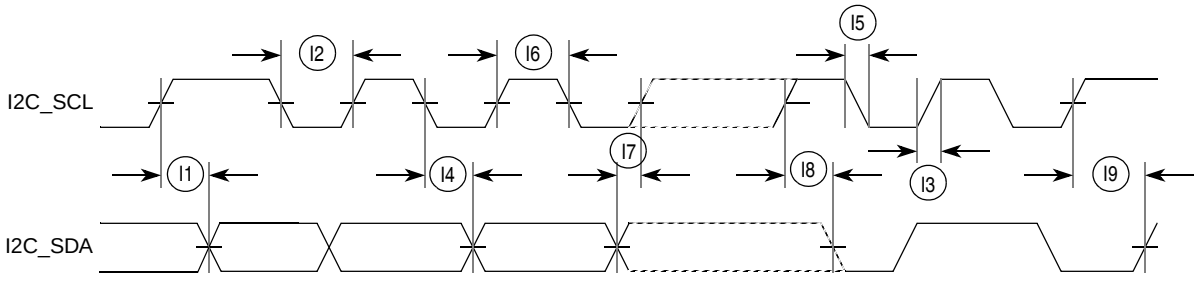


Figure 22. I²C Input/Output Timings

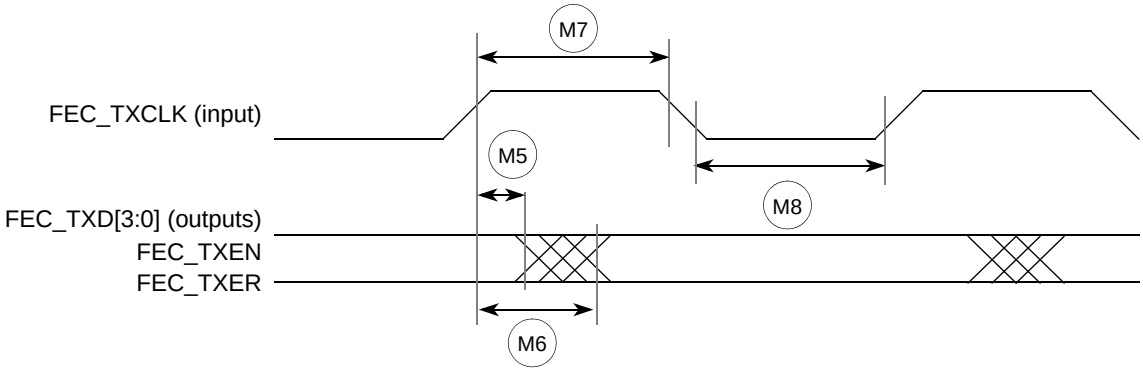


Figure 24. MII Transmit Signal Timing Diagram

5.15.3 MII Async Inputs Signal Timing

Table 25 lists MII asynchronous inputs signal timing.

Table 25. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

Figure 25. MII Async Inputs Timing Diagram

5.15.4 MII Serial Management Channel Timing

Table 26 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 26. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

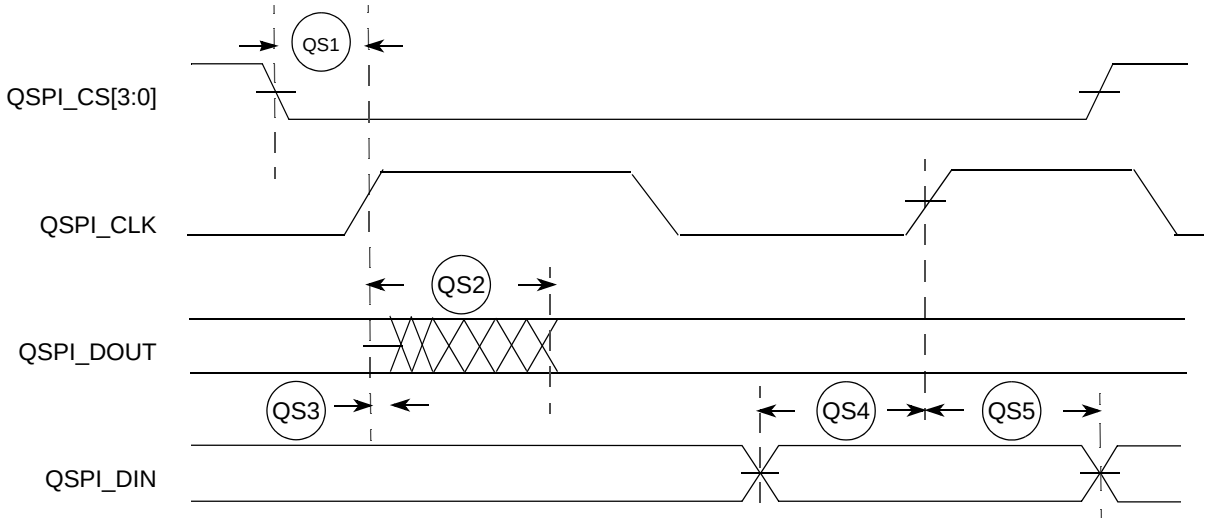


Figure 27. QSPI Timing

5.18 JTAG and Boundary Scan Timing

Table 29. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

Table 32. Typical Active Current Consumption Specifications[1]

$f_{sys/3}$ Frequency	Voltage	Typical[2] Active (Flash)	Peak[3]	Unit
1.333 MHz	3.3V	7.73	7.74	mA
	1.5V	2.87	3.56	
2.666 MHz	3.3V	8.57	8.60	
	1.5V	4.37	5.52	
58 MHz	3.3V	40.10	49.3	
	1.5V	65.90	91.70	
64 MHz	3.3V	44.40	54.0	
	1.5V	69.50	97.0	
72 MHz	3.3V	53.6	63.7	
	1.5V	74.6	104.7	
80 MHz	3.3V	63.0	73.7	
	1.5V	79.6	112.9	

1 All values are measured with a 3.30 V EV_{DD}, 3.30 V SDV_{DD} and 1.5 V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.

2 CPU polling a status register. All peripheral clocks except UART0, FlexBus, INTC0, reset controller, PLL, and edge port disabled.

3 Peak current measured while running a while(1) loop with all modules active.

Figure 35 shows the estimated maximum power consumption.

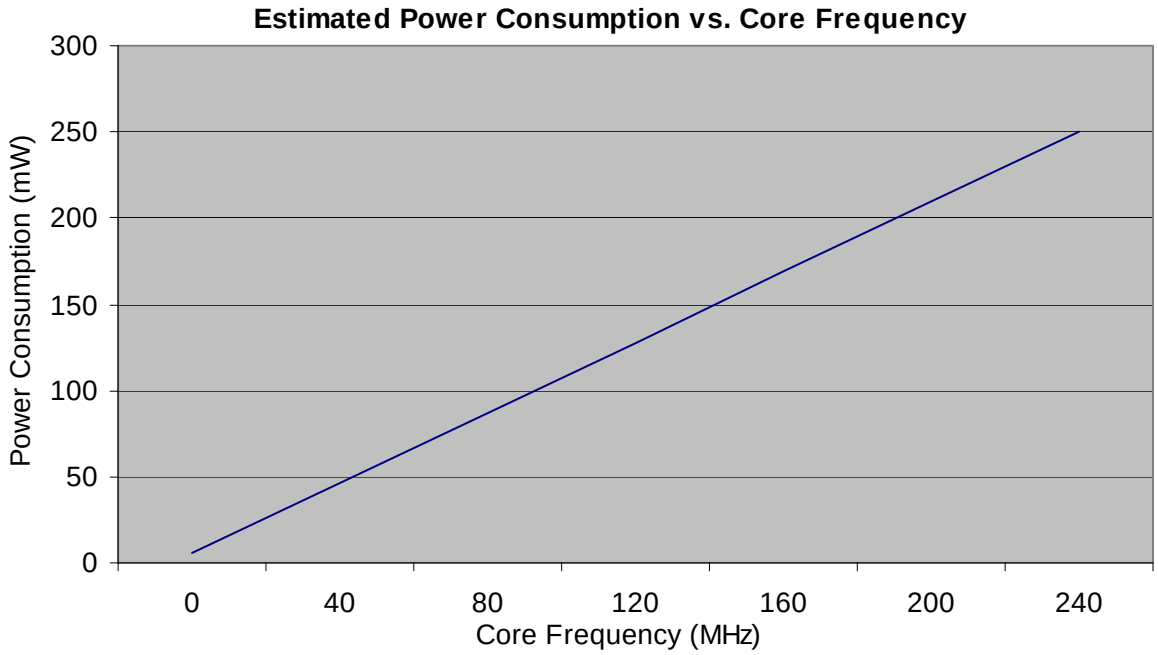


Figure 35. Estimated Maximum Power Consumption

7 Package Information

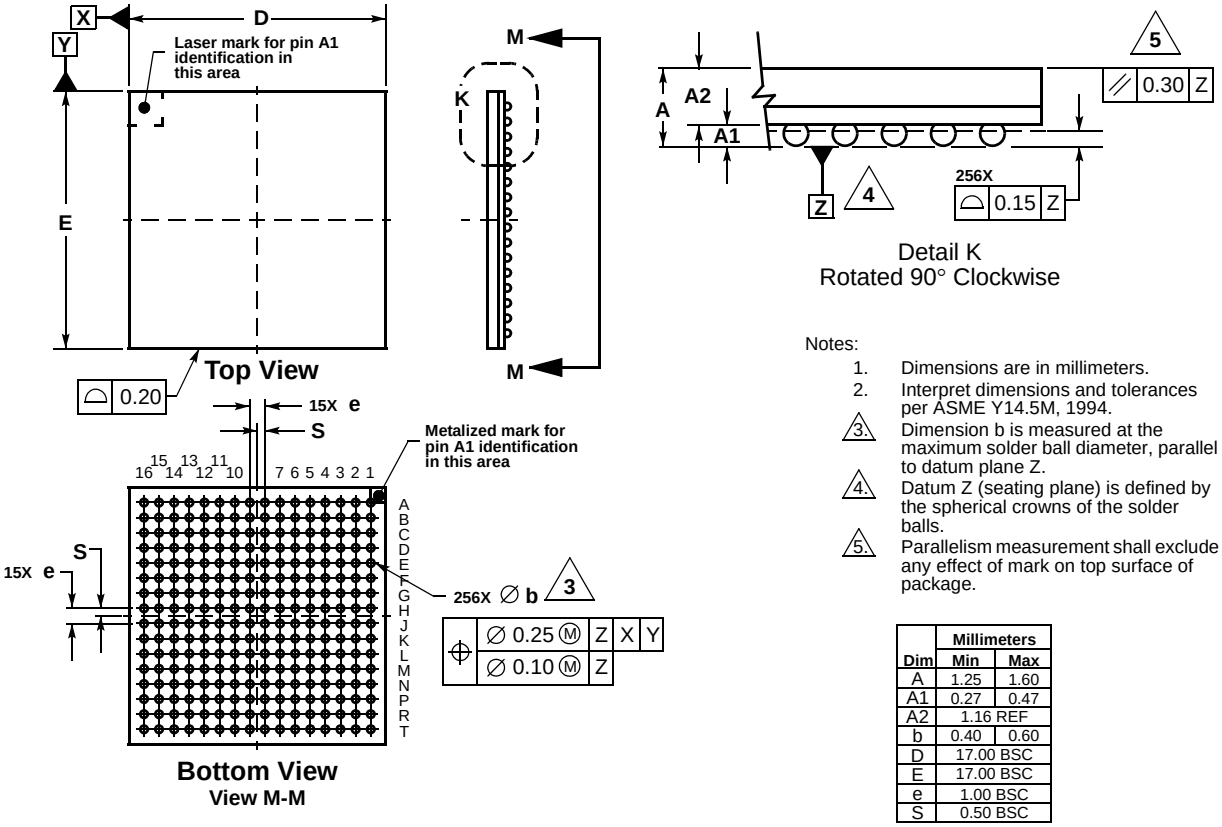
This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF532*x* devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

7.1 Package Dimensions—256 MAPBGA

Figure 36 shows MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 package dimensions.



Dim	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 36. 256 MAPBGA Package Outline

7.2 Package Dimensions—196 MAPBGA

Figure 37 shows the MCF5327CVM240 package dimensions.

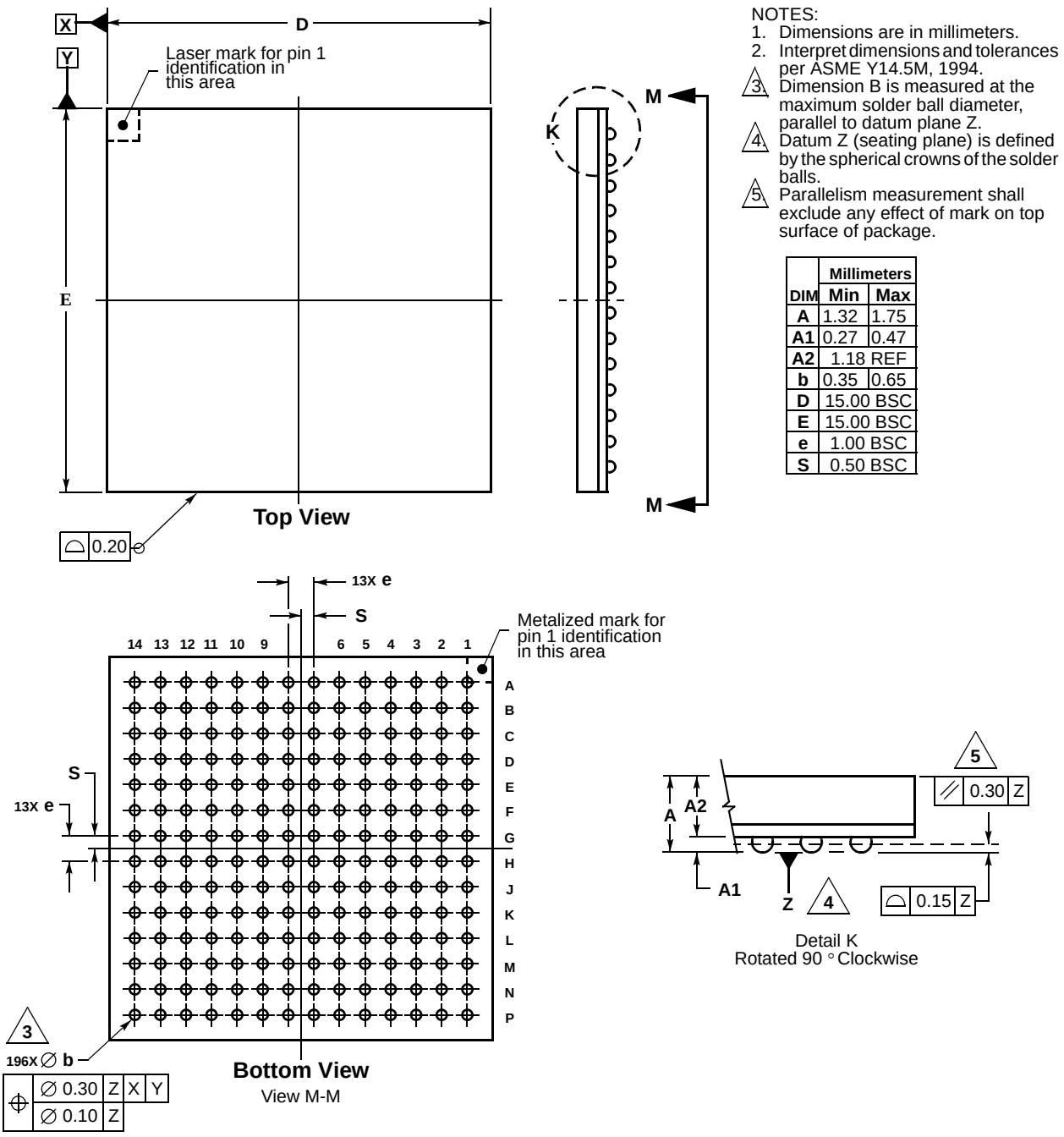


Figure 37. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

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