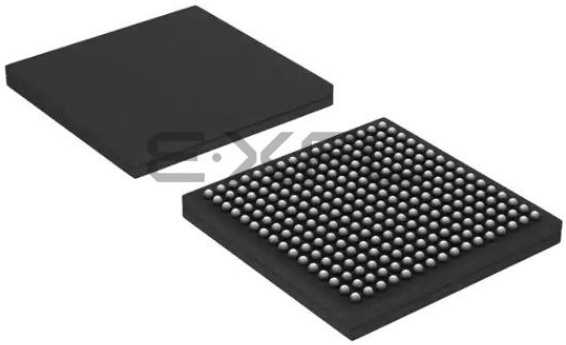

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	94
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf53281cvm240j

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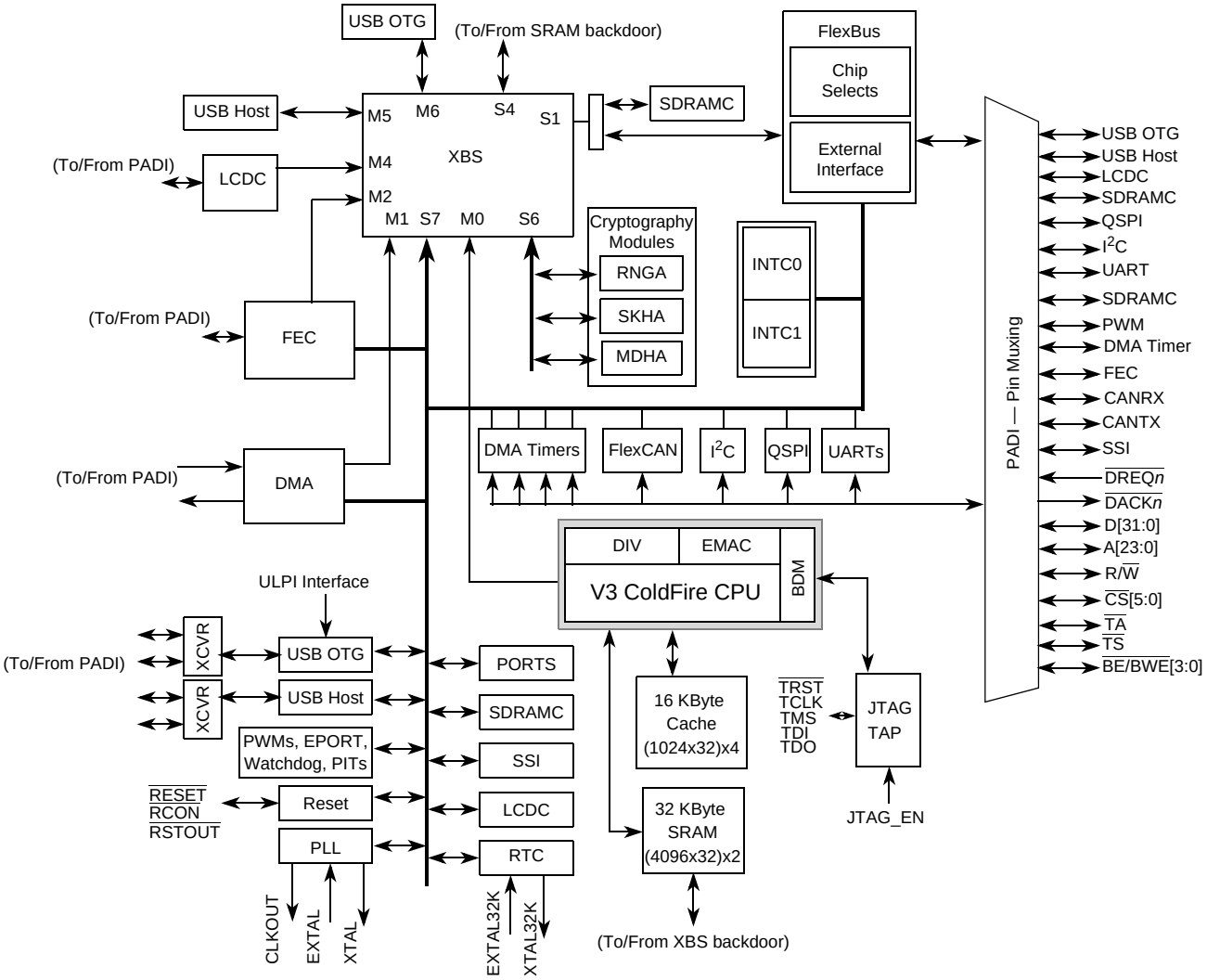

Figure 1. MCF5329 Block Diagram

1 MCF532*x* Family Comparison

The following table compares the various device derivatives available within the MCF532*x* family.

Table 1. MCF532*x* Family Configurations

Module	MCF5327	MCF5328	MCF53281	MCF5329
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•
Core (System) Clock	up to 240 MHz			
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 80 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 211			
Unified Cache	16 Kbytes			
Static RAM (SRAM)	32 Kbytes			

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
USB Host & USB On-the-Go								
USBOTG_M	—	—	—	I/O	USB VDD	G12	L15	L15
USBOTG_P	—	—	—	I/O	USB VDD	H13	L16	L16
USBHOST_M	—	—	—	I/O	USB VDD	K13	M15	M15
USBHOST_P	—	—	—	I/O	USB VDD	J12	M16	M16
FlexCAN (MCF53281 & MCF5329 only)								
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA, SSI_RXD, or LCD_D16 for CANRX and I2C_SCL, SSI_TXD, or LCD_D17 for CANTX.								
PWM								
PWM7	PPWM7	—	—	I/O	EVDD	—	H13	H13
PWM5	PPWM5	—	—	I/O	EVDD	—	H14	H14
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	H14	H15	H15
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	J14	H16	H16
SSI								
SSI_MCLK	PSSI4	—	—	I/O	EVDD	—	G4	G4
SSI_BCLK	PSSI3	$\overline{\text{U2CTS}}$	PWM7	I/O	EVDD	—	F4	F4
SSI_FS	PSSI2	$\overline{\text{U2RTS}}$	PWM5	I/O	EVDD	—	G3	G3
SSI_RXD[2]	PSSI1	U2RXD	CANRX	I	EVDD	—	—	G2
SSI_TXD[2]	PSSI0	U2TXD	CANTX	O	EVDD	—	—	G1
SSI_RXD[2]	PSSI1	U2RXD	—	I	EVDD	—	G2	—
SSI_TXD[2]	PSSI0	U2TXD	—	O	EVDD	—	G1	—
I^2C								
I2C_SCL[2]	PFECI2C1	CANTX	U2TXD	I/O	EVDD	—	—	F3
I2C_SDA[2]	PFECI2C0	CANRX	U2RXD	I/O	EVDD	—	—	F2
I2C_SCL[2]	PFECI2C1	—	U2TXD	I/O	EVDD	E3	F3	—
I2C_SDA[2]	PFECI2C0	—	U2RXD	I/O	EVDD	E4	F2	—
DMA								
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.								

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
QSPI								
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	EVDD	P10	T12	T12
QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	O	EVDD	L11	T13	T13
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	P11	P11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	N10	R12	R12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	EVDD	L10	N12	N12
QSPI_DOUT	PQSPI0	I2C_SDA	—	O	EVDD	M10	P12	P12
UARTs								
$\overline{\text{U1CTS}}$	PUARTL7	SSI_BCLK	—	I	EVDD	C9	D11	D11
$\overline{\text{U1RTS}}$	PUARTL6	SSI_FS	—	O	EVDD	D9	E10	E10
U1TXD	PUARTL5	SSI_TXD[2]	—	O	EVDD	A9	E11	E11
U1RXD	PUARTL4	SSI_RXD[2]	—	I	EVDD	A10	E12	E12
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	EVDD	P13	R15	R15
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	EVDD	N12	T15	T15
U0TXD	PUARTL1	—	—	O	EVDD	P12	T14	T14
U0RXD	PUARTL0	—	—	I	EVDD	P11	R14	R14
Note: The UART2 signals are multiplexed on the QSPI, SSI, DMA Timers, and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	I	EVDD	C1	F1	F1
DT2IN	PTIMER2	DT2OUT	U2TXD	I	EVDD	B1	E1	E1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{DACK1}}$	I	EVDD	A1	E2	E2
DT0IN	PTIMER0	DT0OUT	$\overline{\text{DREQ0}}$[2]	I	EVDD	C2	E3	E3
BDM/JTAG[6]								
JTAG_EN[7]	—	—	—	I	EVDD	L12	M13	M13
DSCLK	—	$\overline{\text{TRST}}$[2]	—	I	EVDD	N14	P15	P15
PSTCLK	—	TCLK[2]	—	O	EVDD	L7	T9	T9
$\overline{\text{BKPT}}$	—	TMS[2]	—	I	EVDD	M12	R16	R16
DSI	—	TDI[2]	—	I	EVDD	K12	N14	N14
DSO	—	TDO	—	O	EVDD	N9	N11	N11
DDATA[3:0]	—	—	—	O	EVDD	N7, P7, L8, M8	N9, P9, N10, P10	N9, P9, N10, P10

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
PST[3:0]	—	—	—	O	EVDD	N8, P8, L9, M9	R10, T10, R11, T11	R10, T10, R11, T11
Test								
TEST[7]	—	—	—	I	EVDD	E10	A16	A16
PLL_TEST[8]	—	—	—	I	EVDD	—	N13	N13
Power Supplies								
EVDD	—	—	—	—	—	E6, E7, F5–F7, H9, J8, J9, K8, K9, K11	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10
IVDD	—	—	—	—	—	E5, K5, K10, J10	E5, G12, M5, M11, M12	E5, G12, M5, M11, M12
PLL_VDD	—	—	—	—	—	H10	J12	J12
SD_VDD	—	—	—	—	—	E8, E9, F8–F10, J5–J7, K7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7
USB_VDD	—	—	—	—	—	G10	L14	L14
VSS	—	—	—	—	—	G6–G9, H6–H8, P9	G7–G10, H7–H10, J7–10, K7–K10, L12, L13	G7–G10, H7–H10, J7–10, K7–K10, L12, L13
PLL_VSS	—	—	—	—	—	H11	K13	K13
USB_VSS	—	—	—	—	—	H12	M14	M14

1 Refers to pin's primary function.

2 Pull-up enabled internally on this signal for this mode.

3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

7 Pull-down enabled internally on this signal for this mode.

8 Must be left floating for proper operation of the PLL.

4.3 Pinout—196 MAPBGA

The pinout for the MCF5327CVM240 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DT1IN	LCD_ D4	LCD_ D5	LCD_ D9	LCD_ D13	LCD_ D17	LCD_FLM/ VSYNC	LCD_LP/ HSYNC	U1TXD	U1RXD	FB_CS3	A20	A16	A15	A
B	D2TIN	LCD_ D0	LCD_ D6	LCD_ D8	LCD_ D12	LCD_ D16	LCD_CON TRAST	LCD_ LSCLK	LCD_ SPL_SPR	FB_CS0	A23	A21	A17	A14	B
C	DT3IN	DT0IN	LCD_ D2	LCD_ D7	LCD_ D11	LCD_ D15	LCD_ CLS	LCD_ PS	U1CTS	FB_CS1	A22	A18	A13	A12	C
D	SD_WE	TS	LCD_ D1	LCD_ D3	LCD_ D10	LCD_ D14	LCD_ ACD/OE	LCD_ REV	U1RTS	FB_CS2	A19	A11	A10	A9	D
E	SD_CKE	SD_CS0	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	A8	A7	A6	A5	E
F	D12	D13	D14	D15	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	A4	A3	A2	A1	F
G	BE/ BWE1	D8	D9	D10	D11	VSS	VSS	VSS	VSS	USB OTG_VDD	DRAM SEL	USB OTG_M	TA	A0	G
H	D29	D30	D31	BE/ BWE3	SD_ DQS3	VSS	VSS	VSS	EVDD	PLL_ VDD	PLL_ VSS	USBHOST _VSS	USB OTG_P	PWM3	H
J	D25	D26	D27	D28	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	RESET	USB HOST_P	IRQ7	PWM1	J
K	D24	SD_CLK	SD_CLK	SD_DR_ DQS	IVDD	SD_ DQS2	SD_VDD	EVDD	EVDD	IVDD	EVDD	TDI/DSI	USB HOST_M	XTAL	K
L	FB_CLK	SD_A10	SD_CAS	D23	D7	D1	TCLK/ PSTCLK	DDATA1	PST1	QSPI_ DIN	QSPI_ CS1	JTAG_ EN	IRQ4	EXTAL	L
M	SD_RAS	D22	D21	BE/ BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_ DOUT	EXTAL 32K	TMS/ BKPT	IRQ2	IRQ3	M
N	D20	D19	D16	D6	D3	R/W	DDATA3	PST3	TDO/ DSO	QSPI_ CLK	XTAL 32K	U0RTS	IRQ1	TRST/ DSCLK	N
P	D18	D17	BE/ BWE2	D5	D2	OE	DDATA2	PST2	VSS	QSPI_ CS2	U0RXD	U0TXD	U0CTS	RSTOUT	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 5. MCF5327CVM240 Pinout Top View (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5329 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5329.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

5.2 Thermal Characteristics

Table 5. Thermal Characteristics

Characteristic		Symbol	256MBGA	196MBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	37[1,2]	42[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	38[1,2]	°C/W
Junction to board	—	θ_{JB}	27[3]	32[3]	°C/W
Junction to case	—	θ_{JC}	16[4]	19[4]	°C/W
Junction to top of package	—	Ψ_{jt}	4[1,5]	5[1,5]	°C/W
Maximum operating junction temperature	—	T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 6. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} – 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} _ 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3 V_{SS} – 0.3	 0.45 0.8 0.8	V

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} – 0.35 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 8. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488 x 10^{-6} 163 x 10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF

Table 8. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
12	Crystal capacitive load	C_L		See crystal spec	
13	Discrete load capacitance for XTAL	C_{L_XTAL}		$2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}		$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$	f_{vco}	350	540	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.

2 All internal registers retain data at 0 Hz.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This parameter is guaranteed by design rather than 100% tested.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10 μs, or equivalently the modulation rate is 100 KHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 9 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 9 are shown in Figure 7 and Figure 8.

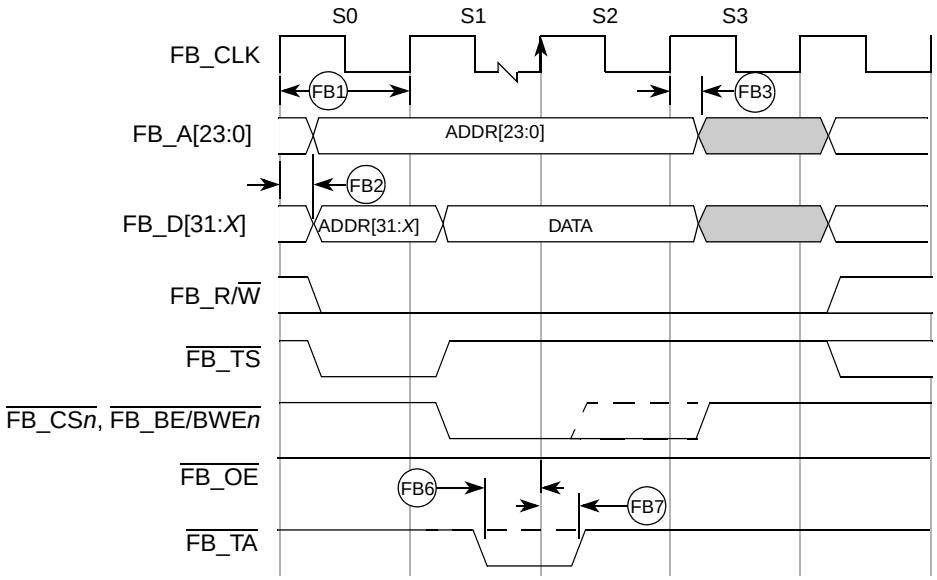

Figure 8. FlexBus Write Timing

5.7 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must remain supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 10. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit
•	Frequency of Operation[1]	•	60	80	MHz
SD1	Clock Period[2]	t_{SDCK}	12.5	16.67	ns
SD3	Pulse Width High[3]	t_{SDCKH}	0.45	0.55	SD_CLK
SD4	Pulse Width Low[4]	t_{SDCKH}	0.45	0.55	SD_CLK
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns
SD6	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns
SD7	SD_SDR_DQS Output Valid[5]	t_{DQSOV}	—	Self timed	ns
SD8	SD_DQS[3:0] input setup relative to SD_CLK[6]	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns

Table 10. SDR Timing Specifications (continued)

Symbol	Characteristic	Symbol	Min	Max	Unit
SD9	SD_DQS[3:2] input hold relative to SD_CLK[7]	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.		
SD10	Data (D[31:0]) Input Setup relative to SD_CLK (reference only)[8]	t_{DVSDCH}	0.25 × SD_CLK	—	ns
SD11	Data Input Hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns
SD12	Data (D[31:0]) and Data Mask(SD_DQM[3:0]) Output Valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns
SD13	Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold	$t_{SDCHDMI}$	1.5	—	ns

1 The FlexBus and SDRAM clock operates at the same frequency of the internal bus clock. See the PLL chapter of the *MCF5329 Reference Manual* for more information on setting the SDRAM clock rate.

2 SD_CLK is one SDRAM clock in (ns).

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 Pulse width high plus pulse width low cannot exceed min and max clock period.

5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS only pulses during a read cycle and one pulse occurs for each data beat.

6 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.

7 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

8 Because a read cycle in SDR mode uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens results in successful SDR reads. The input setup spec is provided as guidance.

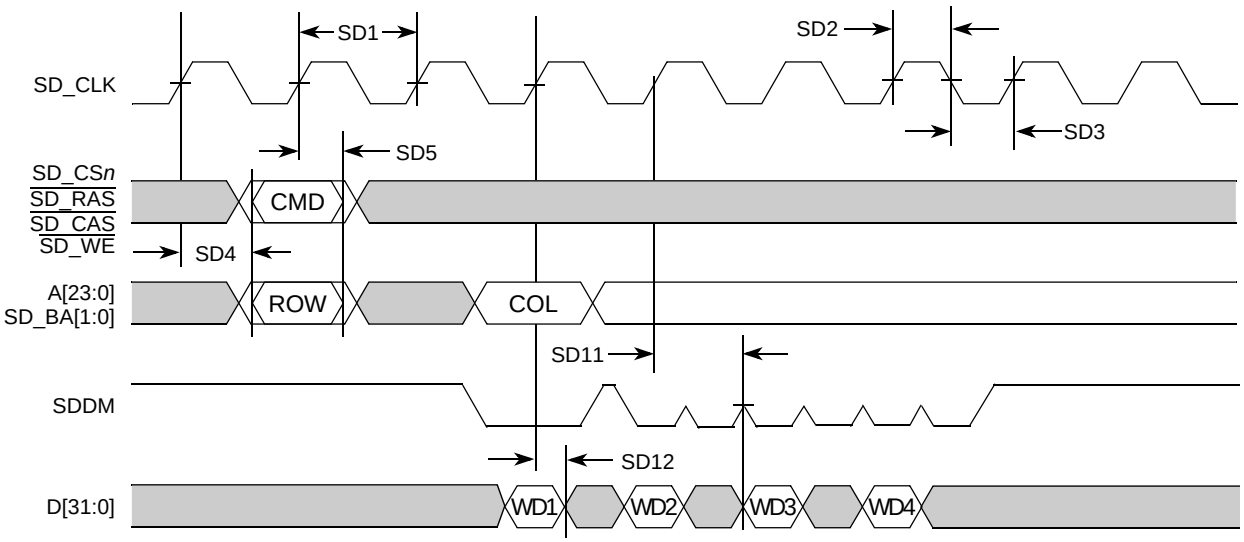

Figure 9. SDR Write Timing

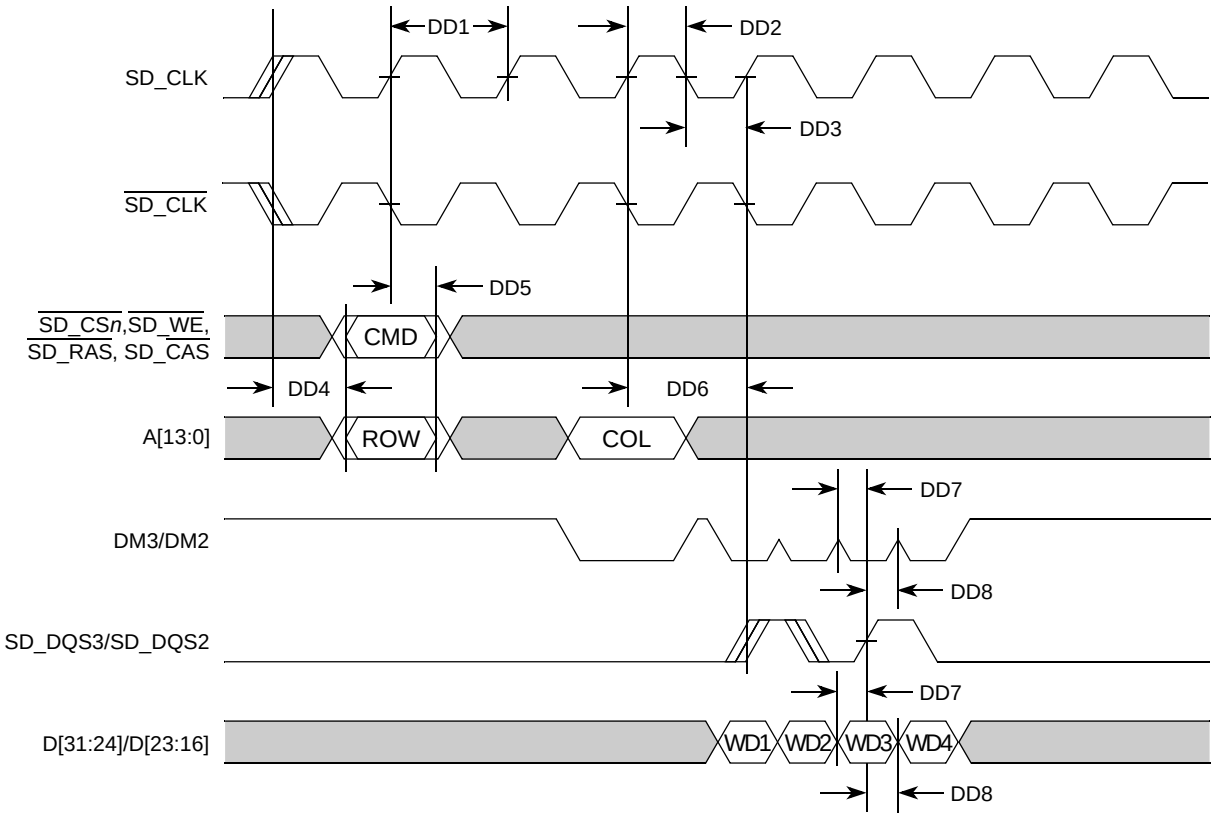

Figure 11. DDR Write Timing

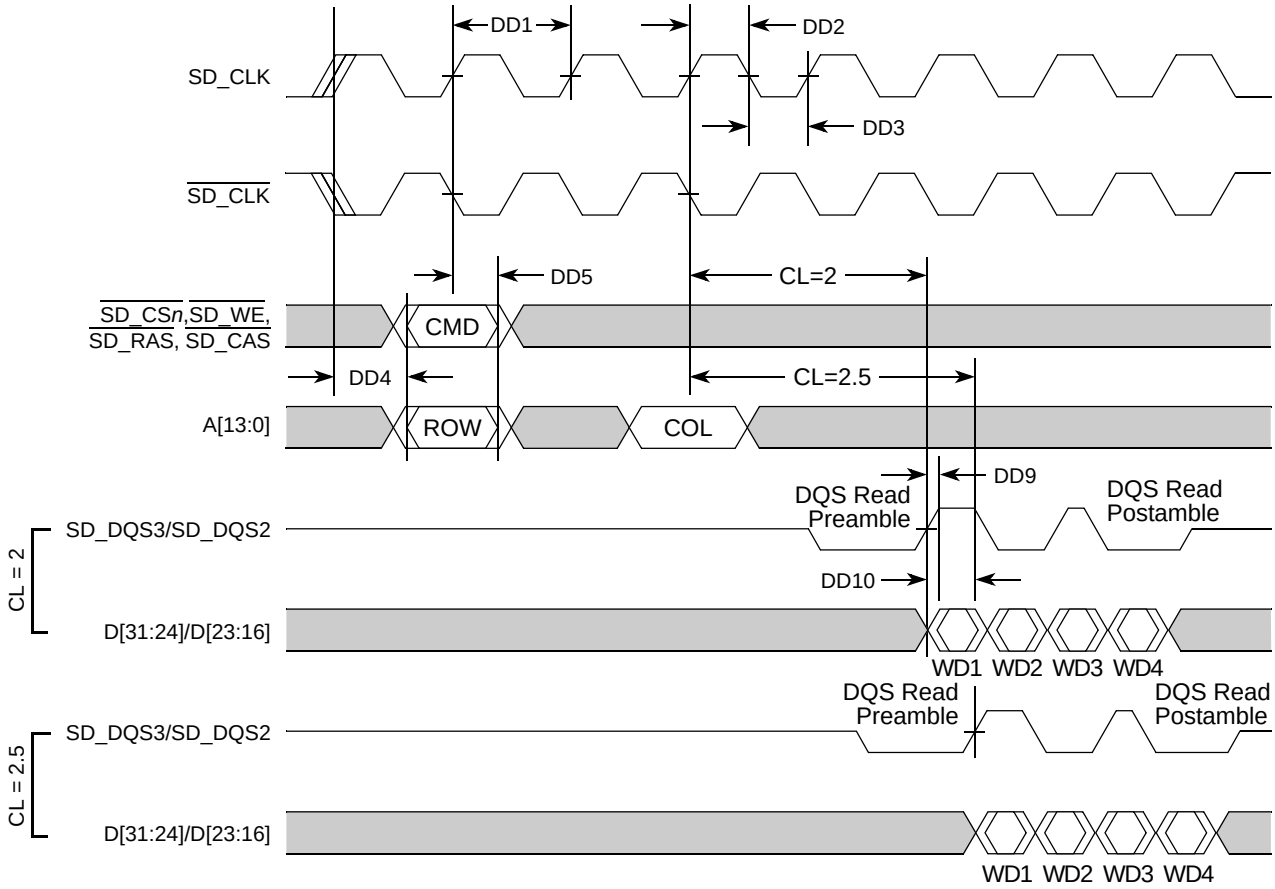

Figure 12. DDR Read Timing

5.8 General Purpose I/O Timing

Table 12. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, FlexCAN, and Timer pins.

Table 21. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Units
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 22 lists specifications for the I²C output timing parameters shown in Figure 22.

Table 22. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 22. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 22 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 22 shows timing for the values in Table 22 and Table 21.

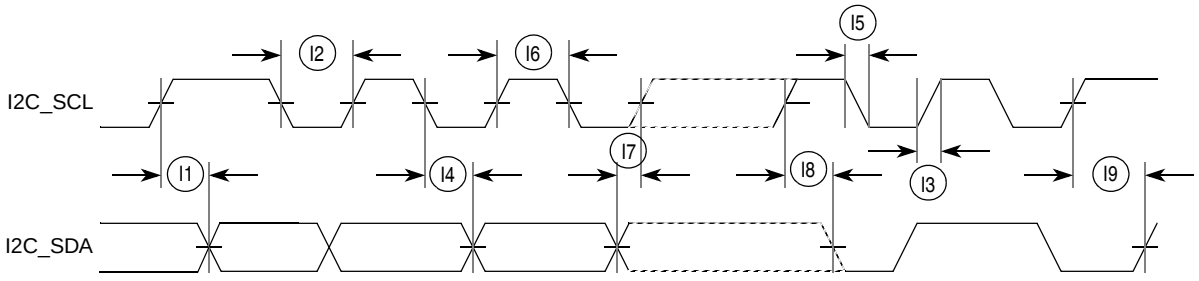

Figure 22. I²C Input/Output Timings

5.15 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

5.15.1 MII Receive Signal Timing

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 23 lists MII receive channel timings.

Table 23. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup	5	—	ns
M2	FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold	5	—	ns
M3	FEC_RXCLK pulse width high	35%	65%	FEC_RXCLK period
M4	FEC_RXCLK pulse width low	35%	65%	FEC_RXCLK period

Figure 23 shows MII receive signal timings listed in Table 23.

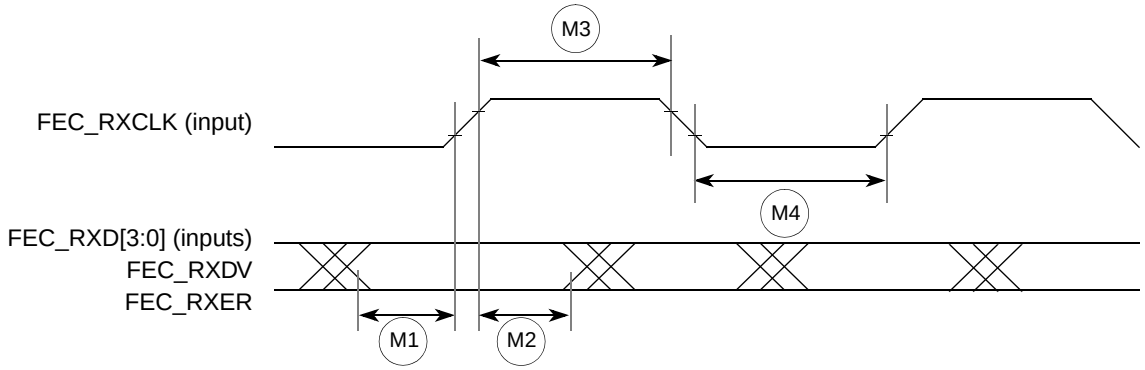

Figure 23. MII Receive Signal Timing Diagram

5.15.2 MII Transmit Signal Timing

Table 24 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC_TXCLK frequency.

Table 24. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid	5	—	ns
M6	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid	—	25	ns
M7	FEC_TXCLK pulse width high	35%	65%	FEC_TXCLK period
M8	FEC_TXCLK pulse width low	35%	65%	FEC_TXCLK period

Figure 24 shows MII transmit signal timings listed in Table 24.

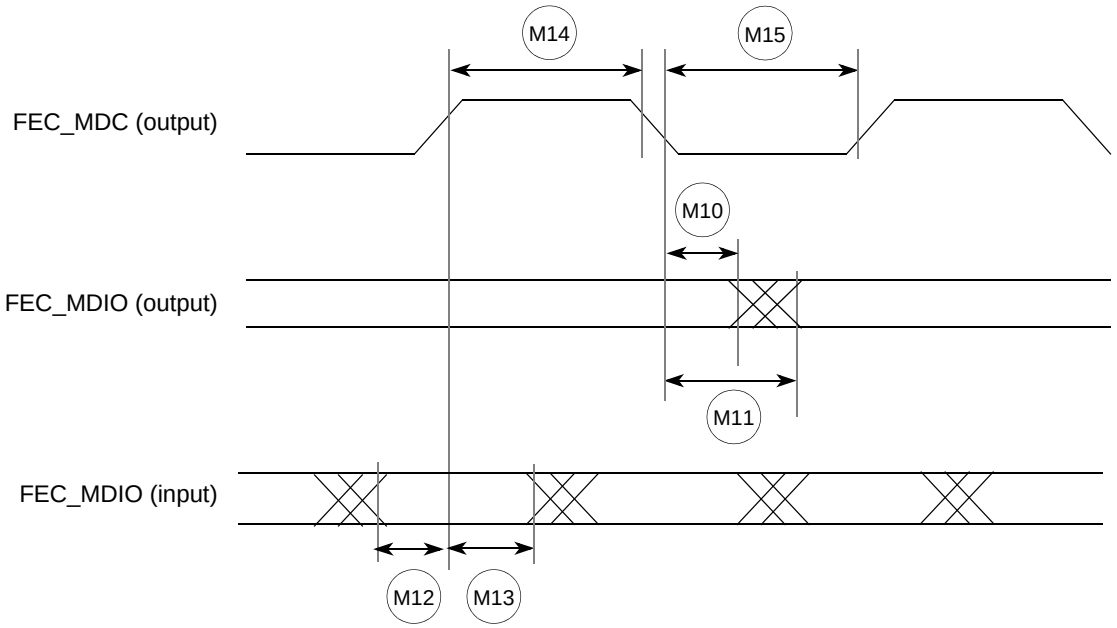

Figure 26. MII Serial Management Channel Timing Diagram

5.16 32-Bit Timer Module Timing Specifications

Table 27 lists timer module AC timings.

Table 27. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.17 QSPI Electrical Specifications

Table 28 lists QSPI timings.

Table 28. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

5.19 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 32.

Table 30. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	2	2	$t_{SYS} = 1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

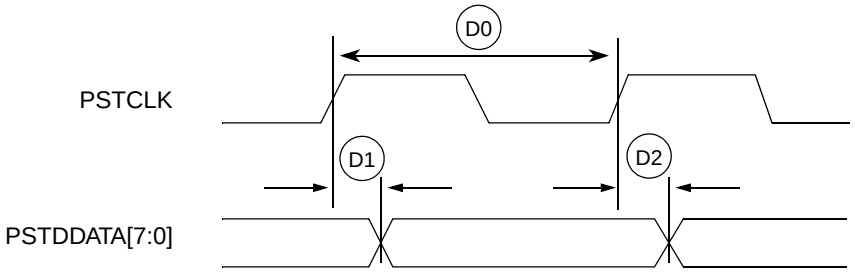

Figure 32. Real-Time Trace AC Timing

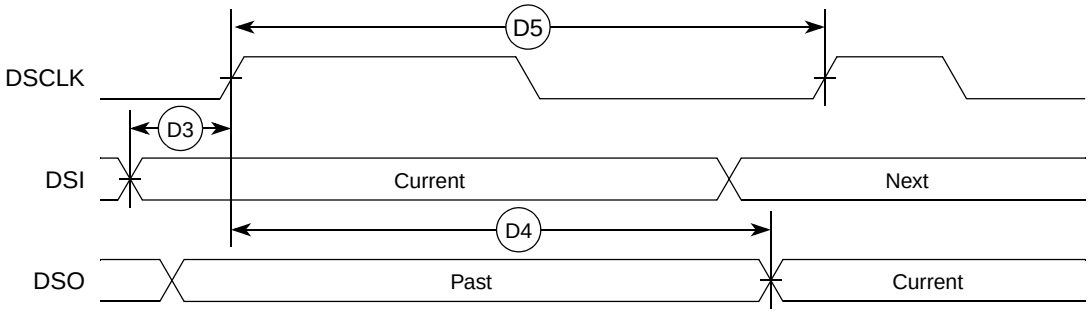

Figure 33. BDM Serial Port AC Timing

6 Current Consumption

All current consumption data is lab data measured on a single device using an evaluation board. Table 31 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

8 Revision History

Table 33. MCF5329DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release.	11/2005
0.1	• Added not to Section 7, “Package Information.” • Added top view and bottom view where appropriate in mechanical drawings and pinout figures. • Figure 6: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006
1	• Corrected MCF5327 196MAPBGA ball map locations in Table 5 for the following signals: RCON, D1, D0, OE, R/W, SD_DQS2, PSTCLK, DDATA[3:0], PST[3:0], EVDD, IVDD, and SD_VDD. Figure 5 was correct. • Updated thermal characteristic values in Table 5. • Updated DC electricals values in Table 7. • Updated Section 3.3, “Supply Voltage Sequencing and Separation Cautions” and subsections. • Updated and added Oscillator/PLL characteristics in Table 8. • Table 9: Swapped min/max for FB1; Removed FB8 & FB9. • Updated SDRAM write timing diagram, Figure 9. • Table 11: Added values for frequency of operation and DD1. • Reworded first paragraph in Section 5.12, “ULPI Timing Specification.” • Updated Figure 19. • Replaced figure & table Section 5.13, “SSI Timing Specifications,” with slave & master mode versions. • Removed second sentence from Section 5.15.2, “MII Transmit Signal Timing,” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.15.2, “MII Transmit Signal Timing,” as this feature is not supported on this device. • Updated figure & table Section 5.19, “Debug AC Timing Specifications.” • Renamed & moved previous version’s Section 5.5 “Power Consumption” to Section 6, “Current Consumption.” Added additional real-world data to this section as well.	7/2007
2	• Added MCF53281 device information throughout: features list, family configuration table, ordering information table, signals description table, and relevant package diagram titles • Remove Footnote 1 from Table 11. • Changed document type from Advance Information to Technical Data.	8/2007
3	• Corrected MCF53281 in features list table. This device contains CAN, but does not feature the cryptography accelerators. • In pin-multiplexing table, moved MCF53281 label from the MCF5328 column to the MCF5329 column, because this device contains CAN output signals.	10/2007

Table 33. MCF5329DS Document Revision History (continued)

Rev. No.	Substantive Changes	Date of Release
4	• Corrected pinouts in Signal Information and Pin-Muxing table for 196 MAPBGA device: Changed D[15:1] entry from “F4–F1, G4–G2...” to “F4–F1, G5–G2...” Changed DSO/TDO entry from “P9” to “N9” • Corrected D0 spec in Table 30 from 1.5 x t_{sys} to 2 x t_{sys} for min and max balues. • Updated FlexBus read and write timing diagrams in Figure 7 and Figure 8. • Removed footnote 2 from the IRQ[7:1] alternate functions USBHOST VBUS_EN, USBHOST VBUS_OC, SSI_MCLK, USB_CLKIN, and SSI_CLKIN signals in Signal Information and Pin-Muxing table. • Updated pinouts for 196 MAPBGA device, MCF5327CVM240 in both Figure 5 and Table 2. The following locations are affected: G10–12, H12–14, J11–14, K12–13, L12–13, M12–14, N13. The following signals are affected: USBOTG_VDD, USBHOST_VSS, USBOTG_M, USBOTG_P, USBHOST_M, USBHOST_P, DRAMSEL, PWM3, PWM1, $\overline{\text{IRQ}}$[7,4,3,2,1], $\overline{\text{RESET}}$, TDI/DSI, JTAG_EN, TMS/$\overline{\text{BKPT}}$.	4/2008
5	Changed the following specs in Table 10 and Table 11: • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns	11/2008