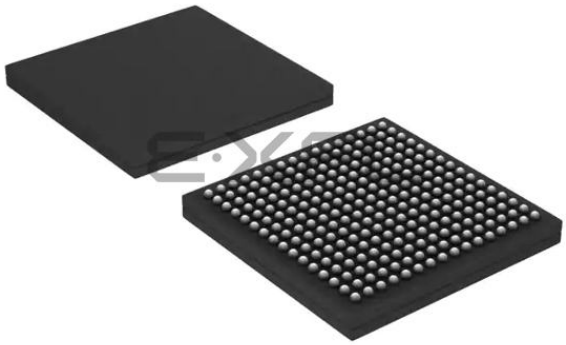

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Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
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Oscillator Type	External
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Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5328cvm240

high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

3.3.2 Power Down Sequence

If IV_{DD}/$PLLV_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there is undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/$PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF532*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 7, "Package Information," for package diagrams. For a more detailed discussion of the MCF532*x* signals, consult the *MCF5329 Reference Manual* (MCF5329RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 3. MCF5327/8/9 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
Reset								
$\overline{\text{RESET}}$[2]	—	—	—	I	EVDD	J11	N15	N15
$\overline{\text{RSTOUT}}$	—	—	—	O	EVDD	P14	P14	P14
Clock								
EXTAL	—	—	—	I	EVDD	L14	P16	P16
XTAL[2]	—	—	—	O	EVDD	K14	N16	N16
EXTAL32K	—	—	—	I	EVDD	M11	P13	P13
XTAL32K	—	—	—	O	EVDD	N11	R13	R13
FB_CLK	—	—	—	O	SDVDD	L1	T2	T2

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
FEC_CRS	PFECH0	ULPI_DIR	—	I	EVDD	—	B8	B8
FEC_TXD[3:1]	PFECL[7:5]	ULPI_DATA[3:1]	—	O	EVDD	—	D3–D1	D3–D1
FEC_TXER	PFECL4	—	—	O	EVDD	—	B1	B1
FEC_RXD[3:1]	PFECL[3:1]	ULPI_DATA[7:5]	—	I	EVDD	—	E7, A6, B6	E7, A6, B6
FEC_RXER	PFECL0	—	—	I	EVDD	—	D4	D4
LCD Controller								
LCD_D17	PLCDDH1	CANTX	—	O	EVDD	—	—	C9
LCD_D16	PLCDDH0	CANRX	—	O	EVDD	—	—	D9
LCD_D17	PLCDDH1	—	—	O	EVDD	A6	C9	—
LCD_D16	PLCDDH0	—	—	O	EVDD	B6	D9	—
LCD_D15	PLCDDM7	—	—	O	EVDD	C6	A7	A7
LCD_D14	PLCDDM6	—	—	O	EVDD	D6	B7	B7
LCD_D13	PLCDDM5	—	—	O	EVDD	A5	C7	C7
LCD_D12	PLCDDM4	—	—	O	EVDD	B5	D7	D7
LCD_D[11:8]	PLCDDM[3:0]	—	—	O	EVDD	C5, D5, A4, B4	D6, E6, A5, B5	D6, E6, A5, B5
LCD_D7	PLCDDL7	—	—	O	EVDD	C4	C5	C5
LCD_D6	PLCDDL6	—	—	O	EVDD	B3	D5	D5
LCD_D5	PLCDDL5	—	—	O	EVDD	A3	A4	A4
LCD_D4	PLCDDL4	—	—	O	EVDD	A2	A3	A3
LCD_D[3:0]	PLCDDL[3:0]	—	—	O	EVDD	D4, C3, D3, B2	B4, C4, B3, C3	B4, C4, B3, C3
LCD_ACD/ LCD_OE	PLCDCTLH0	—	—	O	EVDD	D7	B9	B9
LCD_CLS	PLCDCTLL7	—	—	O	EVDD	C7	A9	A9
LCD_CONTRAST	PLCDCTLL6	—	—	O	EVDD	B7	D10	D10
LCD_FLM/ LCD_VSYNC	PLCDCTLL5	—	—	O	EVDD	A7	C10	C10
LCD_LP/ LCD_HSYNC	PLCDCTLL4	—	—	O	EVDD	A8	B10	B10
LCD_LSCLK	PLCDCTLL3	—	—	O	EVDD	B8	A10	A10
LCD_PS	PLCDCTLL2	—	—	O	EVDD	C8	A11	A11
LCD_REV	PLCDCTLL1	—	—	O	EVDD	D8	B11	B11
LCD_SPL_SPR	PLCDCTLL0	—	—	O	EVDD	B9	C11	C11

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
USB Host & USB On-the-Go								
USBOTG_M	—	—	—	I/O	USB VDD	G12	L15	L15
USBOTG_P	—	—	—	I/O	USB VDD	H13	L16	L16
USBHOST_M	—	—	—	I/O	USB VDD	K13	M15	M15
USBHOST_P	—	—	—	I/O	USB VDD	J12	M16	M16
FlexCAN (MCF53281 & MCF5329 only)								
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA, SSI_RXD, or LCD_D16 for CANRX and I2C_SCL, SSI_TXD, or LCD_D17 for CANTX.								
PWM								
PWM7	PPWM7	—	—	I/O	EVDD	—	H13	H13
PWM5	PPWM5	—	—	I/O	EVDD	—	H14	H14
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	H14	H15	H15
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	J14	H16	H16
SSI								
SSI_MCLK	PSSI4	—	—	I/O	EVDD	—	G4	G4
SSI_BCLK	PSSI3	$\overline{\text{U2CTS}}$	PWM7	I/O	EVDD	—	F4	F4
SSI_FS	PSSI2	$\overline{\text{U2RTS}}$	PWM5	I/O	EVDD	—	G3	G3
SSI_RXD[2]	PSSI1	U2RXD	CANRX	I	EVDD	—	—	G2
SSI_TXD[2]	PSSI0	U2TXD	CANTX	O	EVDD	—	—	G1
SSI_RXD[2]	PSSI1	U2RXD	—	I	EVDD	—	G2	—
SSI_TXD[2]	PSSI0	U2TXD	—	O	EVDD	—	G1	—
I^2C								
I2C_SCL[2]	PFECI2C1	CANTX	U2TXD	I/O	EVDD	—	—	F3
I2C_SDA[2]	PFECI2C0	CANRX	U2RXD	I/O	EVDD	—	—	F2
I2C_SCL[2]	PFECI2C1	—	U2TXD	I/O	EVDD	E3	F3	—
I2C_SDA[2]	PFECI2C0	—	U2RXD	I/O	EVDD	E4	F2	—
DMA								
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.								

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
QSPI								
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	EVDD	P10	T12	T12
QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	O	EVDD	L11	T13	T13
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	P11	P11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	N10	R12	R12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	EVDD	L10	N12	N12
QSPI_DOUT	PQSPI0	I2C_SDA	—	O	EVDD	M10	P12	P12
UARTs								
$\overline{\text{U1CTS}}$	PUARTL7	SSI_BCLK	—	I	EVDD	C9	D11	D11
$\overline{\text{U1RTS}}$	PUARTL6	SSI_FS	—	O	EVDD	D9	E10	E10
U1TXD	PUARTL5	SSI_TXD[2]	—	O	EVDD	A9	E11	E11
U1RXD	PUARTL4	SSI_RXD[2]	—	I	EVDD	A10	E12	E12
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	EVDD	P13	R15	R15
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	EVDD	N12	T15	T15
U0TXD	PUARTL1	—	—	O	EVDD	P12	T14	T14
U0RXD	PUARTL0	—	—	I	EVDD	P11	R14	R14
Note: The UART2 signals are multiplexed on the QSPI, SSI, DMA Timers, and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	I	EVDD	C1	F1	F1
DT2IN	PTIMER2	DT2OUT	U2TXD	I	EVDD	B1	E1	E1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{DACK1}}$	I	EVDD	A1	E2	E2
DT0IN	PTIMER0	DT0OUT	$\overline{\text{DREQ0}}$[2]	I	EVDD	C2	E3	E3
BDM/JTAG[6]								
JTAG_EN[7]	—	—	—	I	EVDD	L12	M13	M13
DSCLK	—	$\overline{\text{TRST}}$[2]	—	I	EVDD	N14	P15	P15
PSTCLK	—	TCLK[2]	—	O	EVDD	L7	T9	T9
$\overline{\text{BKPT}}$	—	TMS[2]	—	I	EVDD	M12	R16	R16
DSI	—	TDI[2]	—	I	EVDD	K12	N14	N14
DSO	—	TDO	—	O	EVDD	N9	N11	N11
DDATA[3:0]	—	—	—	O	EVDD	N7, P7, L8, M8	N9, P9, N10, P10	N9, P9, N10, P10

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
PST[3:0]	—	—	—	O	EVDD	N8, P8, L9, M9	R10, T10, R11, T11	R10, T10, R11, T11
Test								
TEST[7]	—	—	—	I	EVDD	E10	A16	A16
PLL_TEST[8]	—	—	—	I	EVDD	—	N13	N13
Power Supplies								
EVDD	—	—	—	—	—	E6, E7, F5–F7, H9, J8, J9, K8, K9, K11	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10
IVDD	—	—	—	—	—	E5, K5, K10, J10	E5, G12, M5, M11, M12	E5, G12, M5, M11, M12
PLL_VDD	—	—	—	—	—	H10	J12	J12
SD_VDD	—	—	—	—	—	E8, E9, F8–F10, J5–J7, K7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7
USB_VDD	—	—	—	—	—	G10	L14	L14
VSS	—	—	—	—	—	G6–G9, H6–H8, P9	G7–G10, H7–H10, J7–10, K7–K10, L12, L13	G7–G10, H7–H10, J7–10, K7–K10, L12, L13
PLL_VSS	—	—	—	—	—	H11	K13	K13
USB_VSS	—	—	—	—	—	H12	M14	M14

1 Refers to pin's primary function.

2 Pull-up enabled internally on this signal for this mode.

3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

7 Pull-down enabled internally on this signal for this mode.

8 Must be left floating for proper operation of the PLL.

4.3 Pinout—196 MAPBGA

The pinout for the MCF5327CVM240 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DT1IN	LCD_ D4	LCD_ D5	LCD_ D9	LCD_ D13	LCD_ D17	LCD_FLM/ VSYNC	LCD_LP/ HSYNC	U1TXD	U1RXD	FB_CS3	A20	A16	A15	A
B	D2TIN	LCD_ D0	LCD_ D6	LCD_ D8	LCD_ D12	LCD_ D16	LCD_CON TRAST	LCD_ LSCLK	LCD_ SPL_SPR	FB_CS0	A23	A21	A17	A14	B
C	DT3IN	DT0IN	LCD_ D2	LCD_ D7	LCD_ D11	LCD_ D15	LCD_ CLS	LCD_ PS	U1CTS	FB_CS1	A22	A18	A13	A12	C
D	SD_WE	TS	LCD_ D1	LCD_ D3	LCD_ D10	LCD_ D14	LCD_ ACD/OE	LCD_ REV	U1RTS	FB_CS2	A19	A11	A10	A9	D
E	SD_CKE	SD_CS0	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	A8	A7	A6	A5	E
F	D12	D13	D14	D15	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	A4	A3	A2	A1	F
G	BE/ BWE1	D8	D9	D10	D11	VSS	VSS	VSS	VSS	USB OTG_VDD	DRAM SEL	USB OTG_M	TA	A0	G
H	D29	D30	D31	BE/ BWE3	SD_ DQS3	VSS	VSS	VSS	EVDD	PLL_ VDD	PLL_ VSS	USBHOST _VSS	USB OTG_P	PWM3	H
J	D25	D26	D27	D28	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	RESET	USB HOST_P	IRQ7	PWM1	J
K	D24	SD_CLK	SD_CLK	SD_DR_ DQS	IVDD	SD_ DQS2	SD_VDD	EVDD	EVDD	IVDD	EVDD	TDI/DSI	USB HOST_M	XTAL	K
L	FB_CLK	SD_A10	SD_CAS	D23	D7	D1	TCLK/ PSTCLK	DDATA1	PST1	QSPI_ DIN	QSPI_ CS1	JTAG_ EN	IRQ4	EXTAL	L
M	SD_RAS	D22	D21	BE/ BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_ DOUT	EXTAL 32K	TMS/ BKPT	IRQ2	IRQ3	M
N	D20	D19	D16	D6	D3	R/W	DDATA3	PST3	TDO/ DSO	QSPI_ CLK	XTAL 32K	U0RTS	IRQ1	TRST/ DSCLK	N
P	D18	D17	BE/ BWE2	D5	D2	OE	DDATA2	PST2	VSS	QSPI_ CS2	U0RXD	U0TXD	U0CTS	RSTOUT	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 5. MCF5327CVM240 Pinout Top View (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5329 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5329.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} – 0.35 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 8. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488 x 10^{-6} 163 x 10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF

Table 8. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
12	Crystal capacitive load	C_L		See crystal spec	
13	Discrete load capacitance for XTAL	C_{L_XTAL}		$2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}		$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$	f_{vco}	350	540	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.

2 All internal registers retain data at 0 Hz.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This parameter is guaranteed by design rather than 100% tested.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10 μs, or equivalently the modulation rate is 100 KHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 9 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 9 are shown in Figure 7 and Figure 8.

Table 11. DDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)[6]	t_{DQDMI}	1.0	—	ns
DD9	Input Data Skew Relative to DQS (Input Setup)[7]	t_{DVDQ}	—	1	ns
DD10	Input Data Hold Relative to DQS[8]	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK
DD14	DQS output write preamble width	t_{DQWPRE}	0.25		SD_CLK
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK

1 SD_CLK is one SDRAM clock in (ns).

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of today's DDR memories. The processor's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

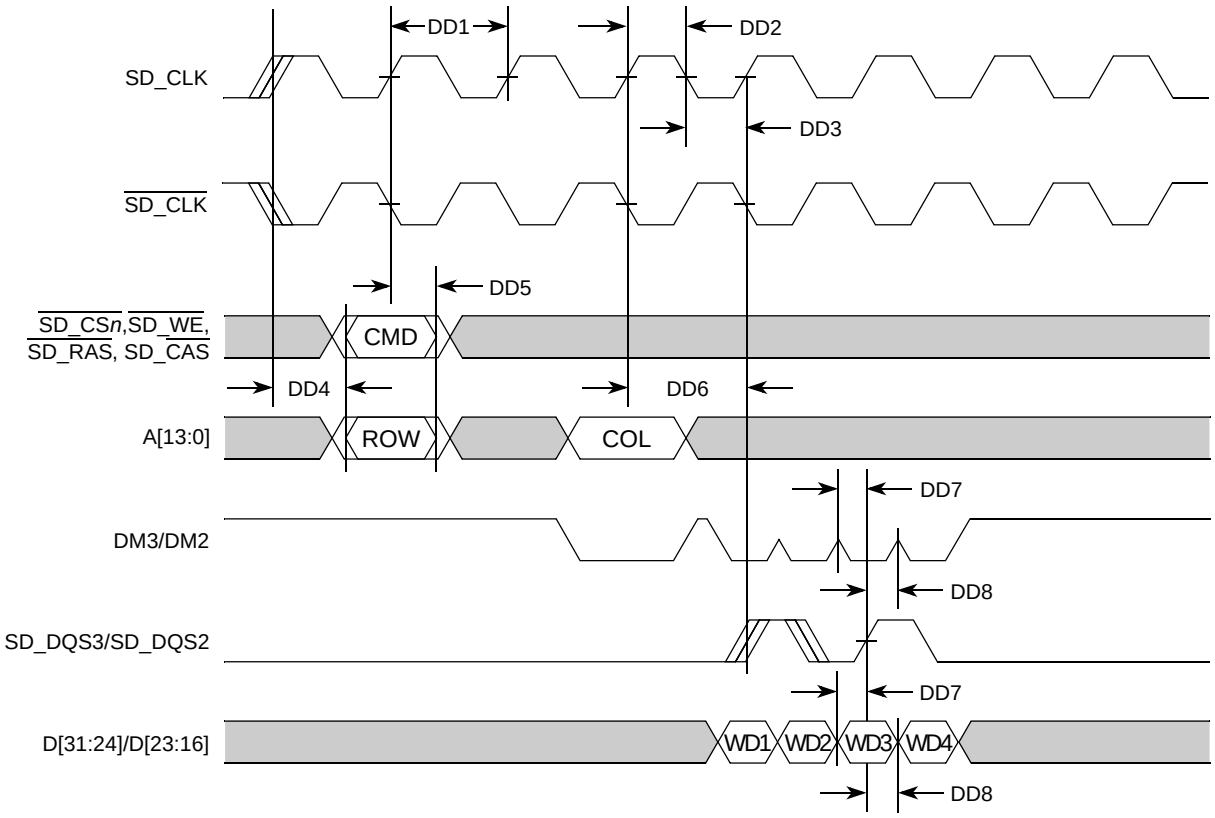


Figure 11. DDR Write Timing

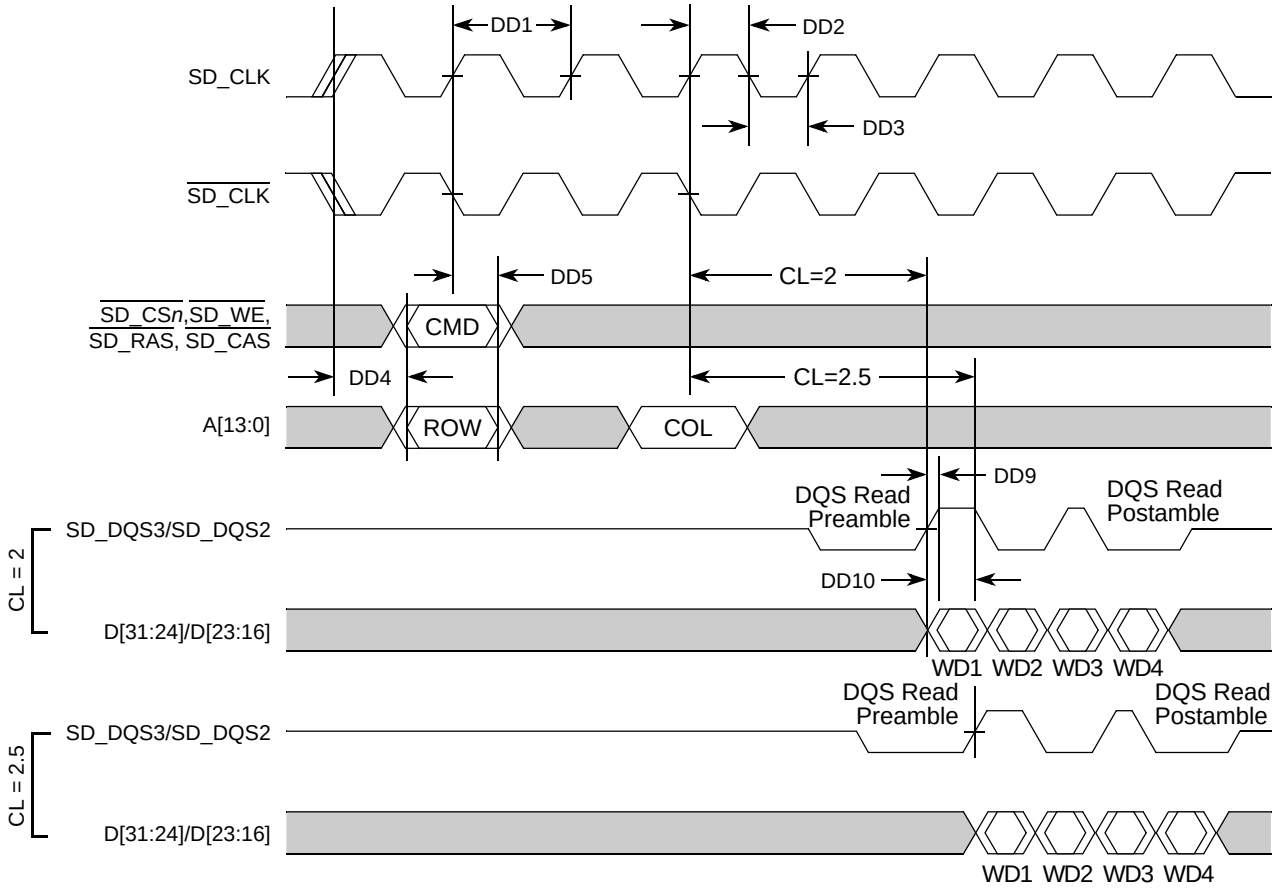


Figure 12. DDR Read Timing

5.8 General Purpose I/O Timing

Table 12. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: $\overline{IRQn}$, PWM, UART, FlexCAN, and Timer pins.

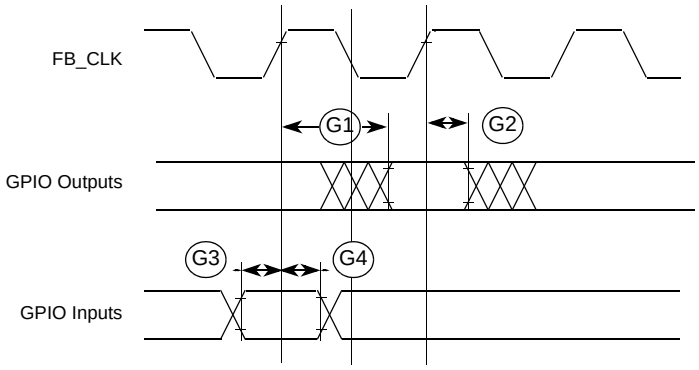


Figure 13. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 13. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

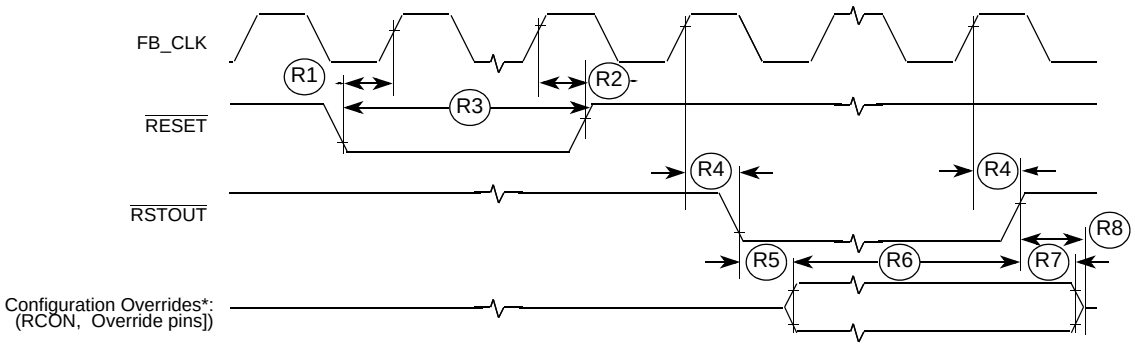


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5329 Reference Manual* for more information.

Table 15. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Number	Description	Minimum	Value	Unit
T1	End of LCD_OE to beginning of LCD_VSYNC	T5+T6+T7-1	(VWAIT1·T2)+T5+T6+T7-1	Ts
T2	LCD_HSYNC period	—	XMAX+T5+T6+T7	Ts
T3	LCD_VSYNC pulse width	T2	VWIDTH·T2	Ts
T4	End of LCD_VSYNC to beginning of LCD_OE	1	(VWAIT2·T2)+1	Ts
T5	LCD_HSYNC pulse width	1	HWIDTH+1	Ts
T6	End of LCD_HSYNC to beginning to LCD_OE	3	HWAIT2+3	Ts
T7	End of LCD_OE to beginning of LCD_HSYNC	1	HWAIT1+1	Ts

Note: Ts is the LCD_LSCLK period. LCD_VSYNC, LCD_HSYNC and LCD_OE can be programmed as active high or active low. In Figure 16, all 3 signals are active low. LCD_LSCLK can be programmed to be deactivated during the LCD_VSYNC pulse or the LCD_OE deasserted period. In Figure 16, LCD_LSCLK is always active.

Note: XMAX is defined in number of pixels in one line.

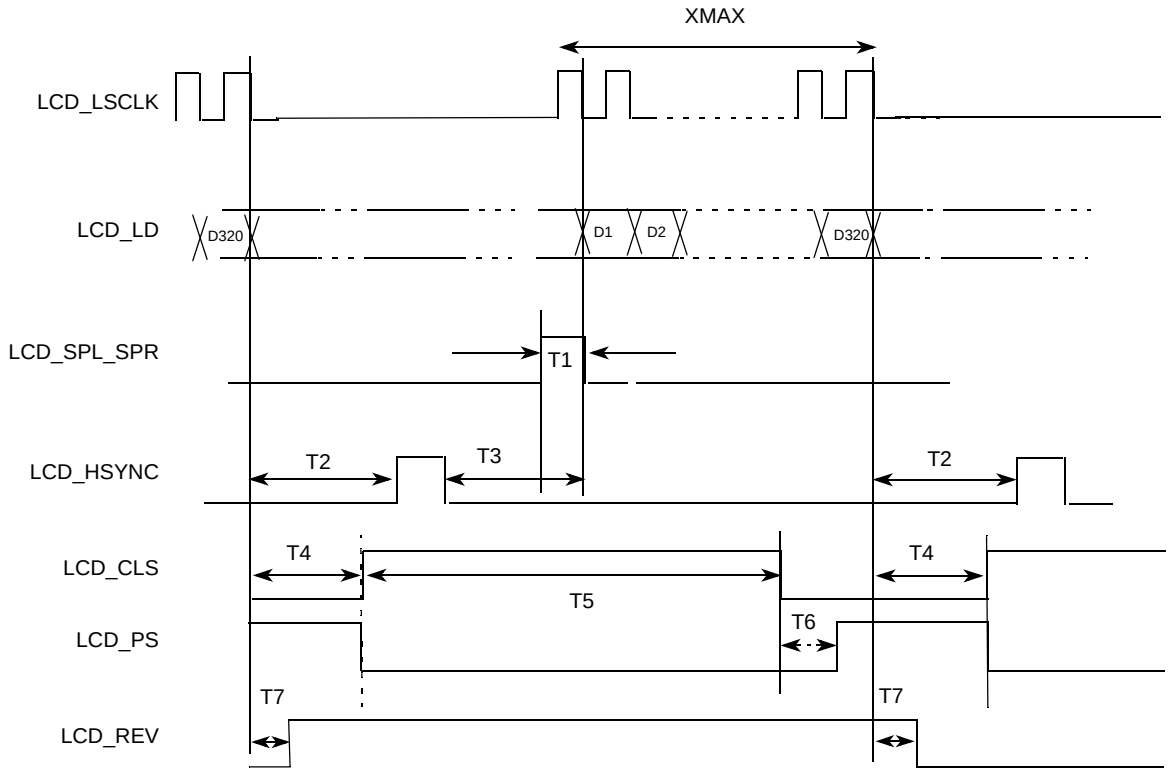


Figure 17. Sharp TFT Panel Timing

5.11 USB On-The-Go

The MCF5329 device is compliant with industry standard USB 2.0 specification.

5.12 ULPI Timing Specification

Control and data timing requirements for the ULPI pins are given in Table 18. These timings apply in synchronous mode only. All timings are measured with either a 60 MHz input clock from the USB_CLKIN pin. The USB_CLKIN needs to maintain a 50% duty cycle. Control signals and 8-bit data are always clocked on the rising edge.

The ULPI interface on the MCF5329 processor is compliant with the industry standard definition.

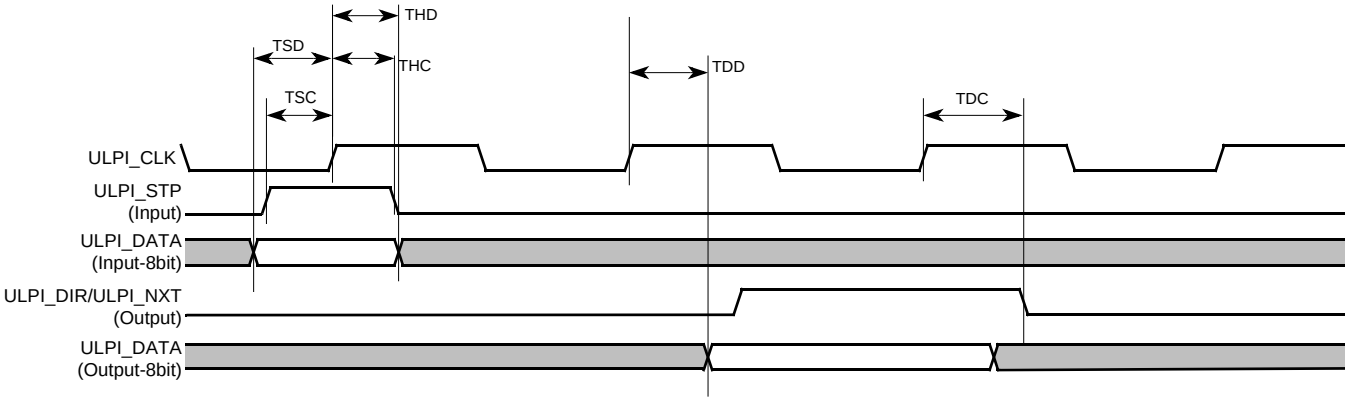


Figure 19. ULPI Timing Diagram

Table 18. ULPI Interface Timing

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	TSC, TSD	—	3.0	ns
Hold time (control in, 8-bit data in)	THC, THD	–1.5	—	ns
Output delay (control out, 8-bit data out)	TDC, TDD	—	6.0	ns

5.13 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 19. SSI Timing – Master Modes[1]

Num	Description	Symbol	Min	Max	Units
S1	SSI_MCLK cycle time[2]	t_{MCLK}	$8 \times t_{SYS}$	—	ns
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}
S3	SSI_BCLK cycle time[3]	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}
S5	SSI_BCLK to SSI_FS output valid		—	15	ns

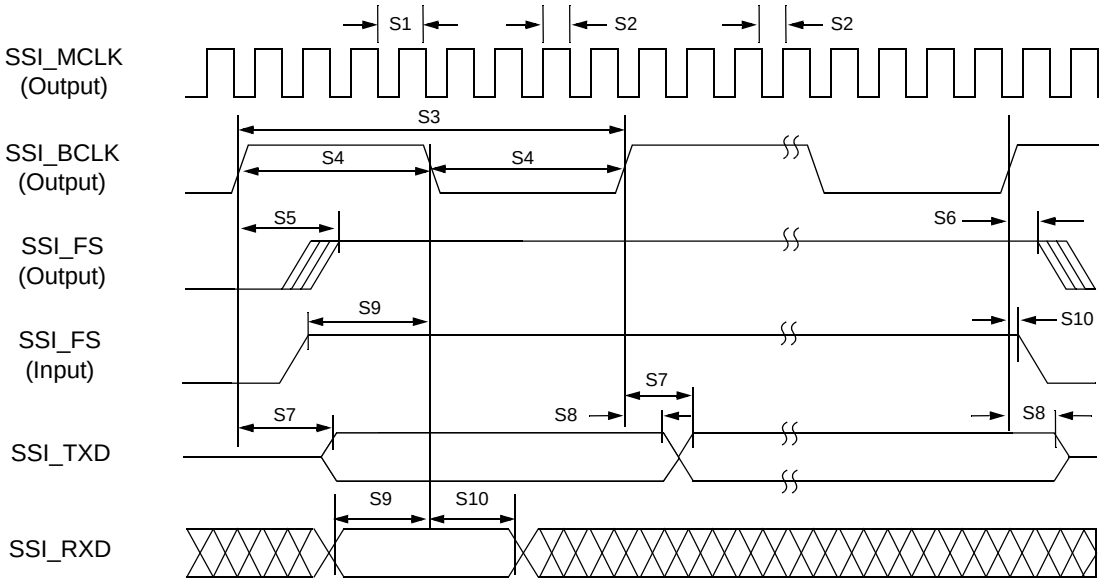


Figure 20. SSI Timing – Master Modes

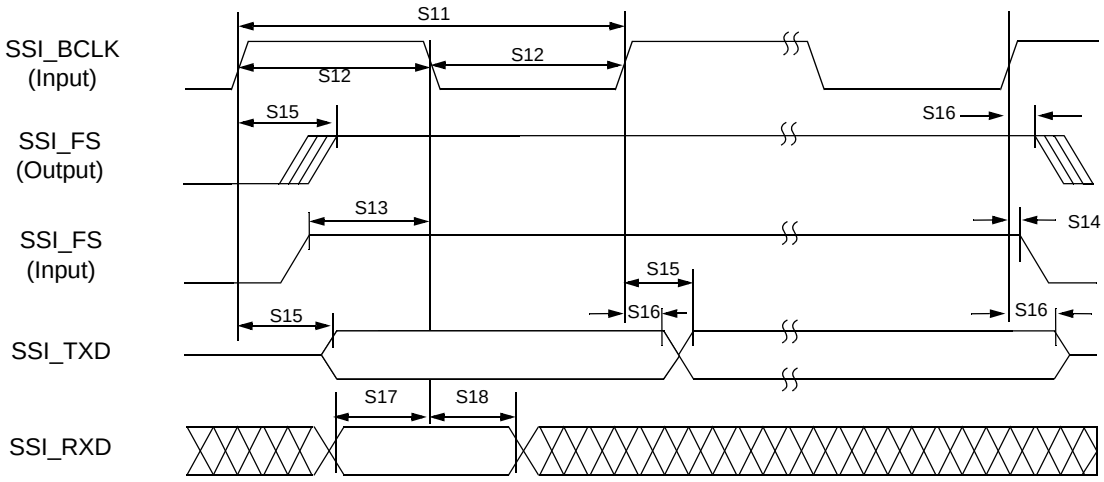


Figure 21. SSI Timing – Slave Modes

5.14 I²C Input/Output Timing Specifications

Table 21 lists specifications for the I²C input timing parameters shown in Figure 22.

Table 21. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

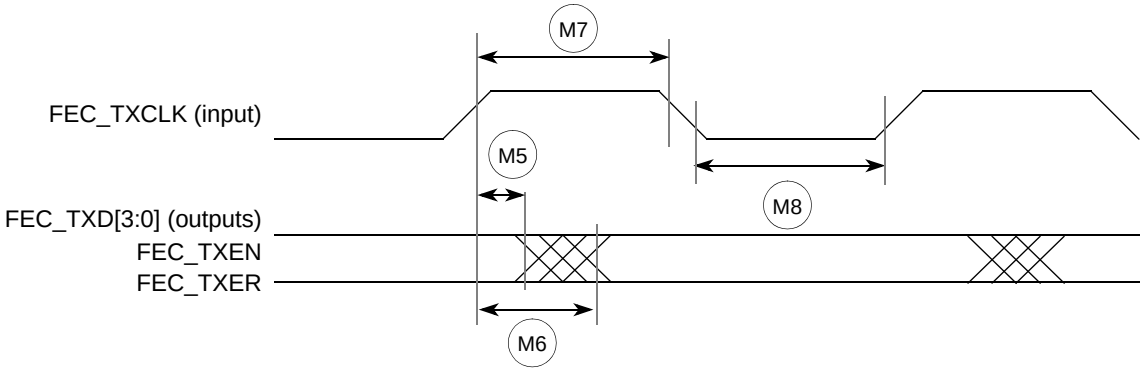


Figure 24. MII Transmit Signal Timing Diagram

5.15.3 MII Async Inputs Signal Timing

Table 25 lists MII asynchronous inputs signal timing.

Table 25. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

Figure 25. MII Async Inputs Timing Diagram

5.15.4 MII Serial Management Channel Timing

Table 26 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 26. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

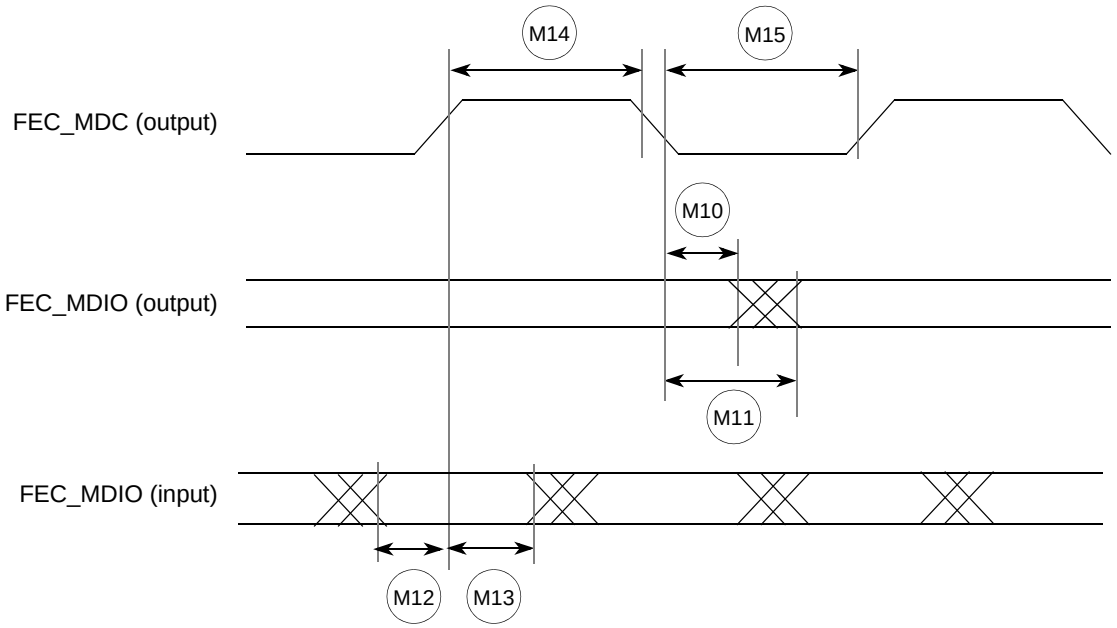


Figure 26. MII Serial Management Channel Timing Diagram

5.16 32-Bit Timer Module Timing Specifications

Table 27 lists timer module AC timings.

Table 27. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.17 QSPI Electrical Specifications

Table 28 lists QSPI timings.

Table 28. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

7 Package Information

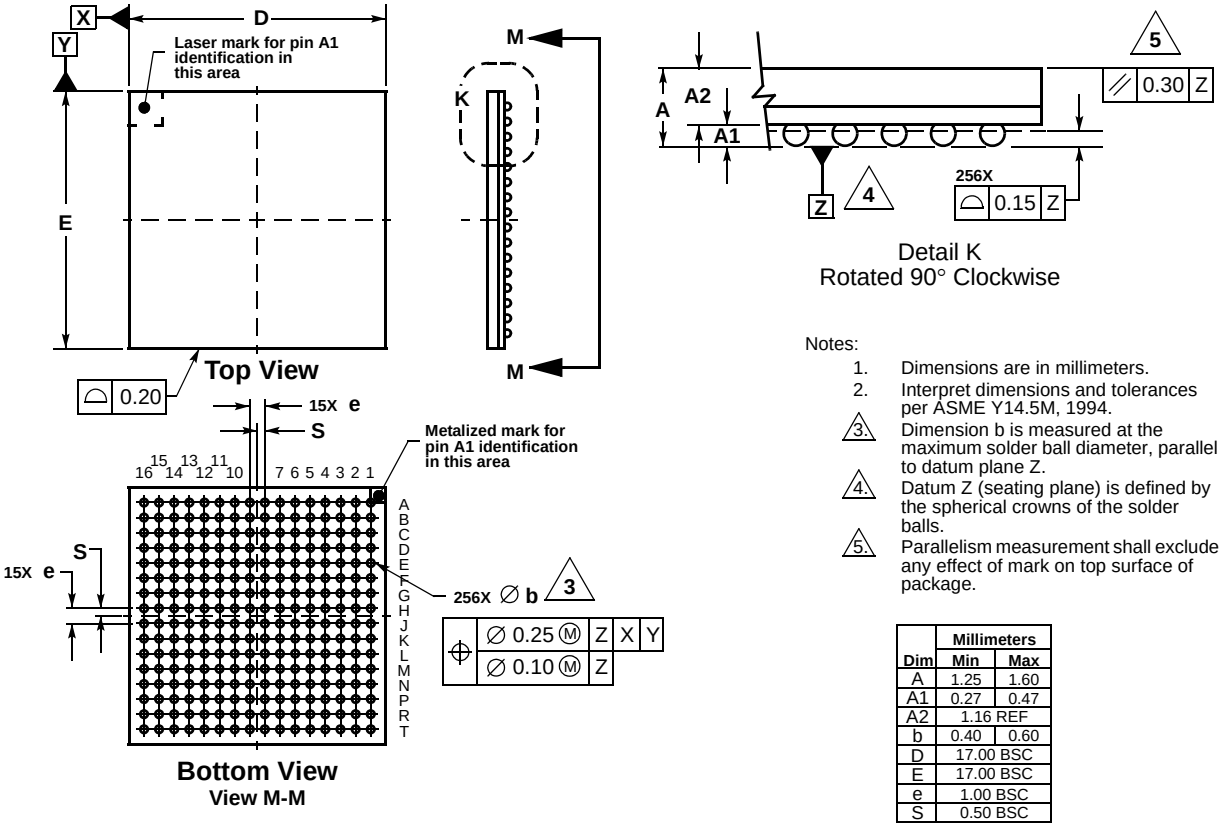
This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF532*x* devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

7.1 Package Dimensions—256 MAPBGA

Figure 36 shows MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 package dimensions.



Dim	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 36. 256 MAPBGA Package Outline

8 Revision History

Table 33. MCF5329DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release.	11/2005
0.1	• Added not to Section 7, “Package Information.” • Added top view and bottom view where appropriate in mechanical drawings and pinout figures. • Figure 6: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006
1	• Corrected MCF5327 196MAPBGA ball map locations in Table 5 for the following signals: RCON, D1, D0, OE, R/W, SD_DQS2, PSTCLK, DDATA[3:0], PST[3:0], EVDD, IVDD, and SD_VDD. Figure 5 was correct. • Updated thermal characteristic values in Table 5. • Updated DC electricals values in Table 7. • Updated Section 3.3, “Supply Voltage Sequencing and Separation Cautions” and subsections. • Updated and added Oscillator/PLL characteristics in Table 8. • Table 9: Swapped min/max for FB1; Removed FB8 & FB9. • Updated SDRAM write timing diagram, Figure 9. • Table 11: Added values for frequency of operation and DD1. • Reworded first paragraph in Section 5.12, “ULPI Timing Specification.” • Updated Figure 19. • Replaced figure & table Section 5.13, “SSI Timing Specifications,” with slave & master mode versions. • Removed second sentence from Section 5.15.2, “MII Transmit Signal Timing,” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.15.2, “MII Transmit Signal Timing,” as this feature is not supported on this device. • Updated figure & table Section 5.19, “Debug AC Timing Specifications.” • Renamed & moved previous version’s Section 5.5 “Power Consumption” to Section 6, “Current Consumption.” Added additional real-world data to this section as well.	7/2007
2	• Added MCF53281 device information throughout: features list, family configuration table, ordering information table, signals description table, and relevant package diagram titles • Remove Footnote 1 from Table 11. • Changed document type from Advance Information to Technical Data.	8/2007
3	• Corrected MCF53281 in features list table. This device contains CAN, but does not feature the cryptography accelerators. • In pin-multiplexing table, moved MCF53281 label from the MCF5328 column to the MCF5329 column, because this device contains CAN output signals.	10/2007