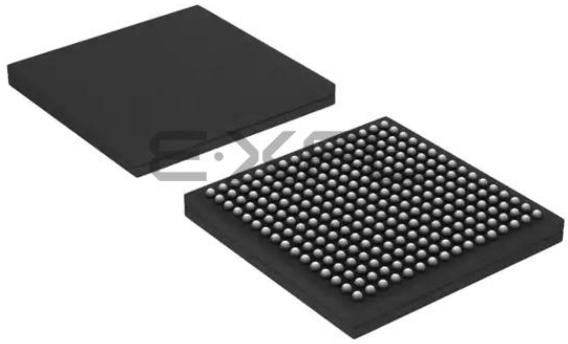


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	94
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5329cvm240

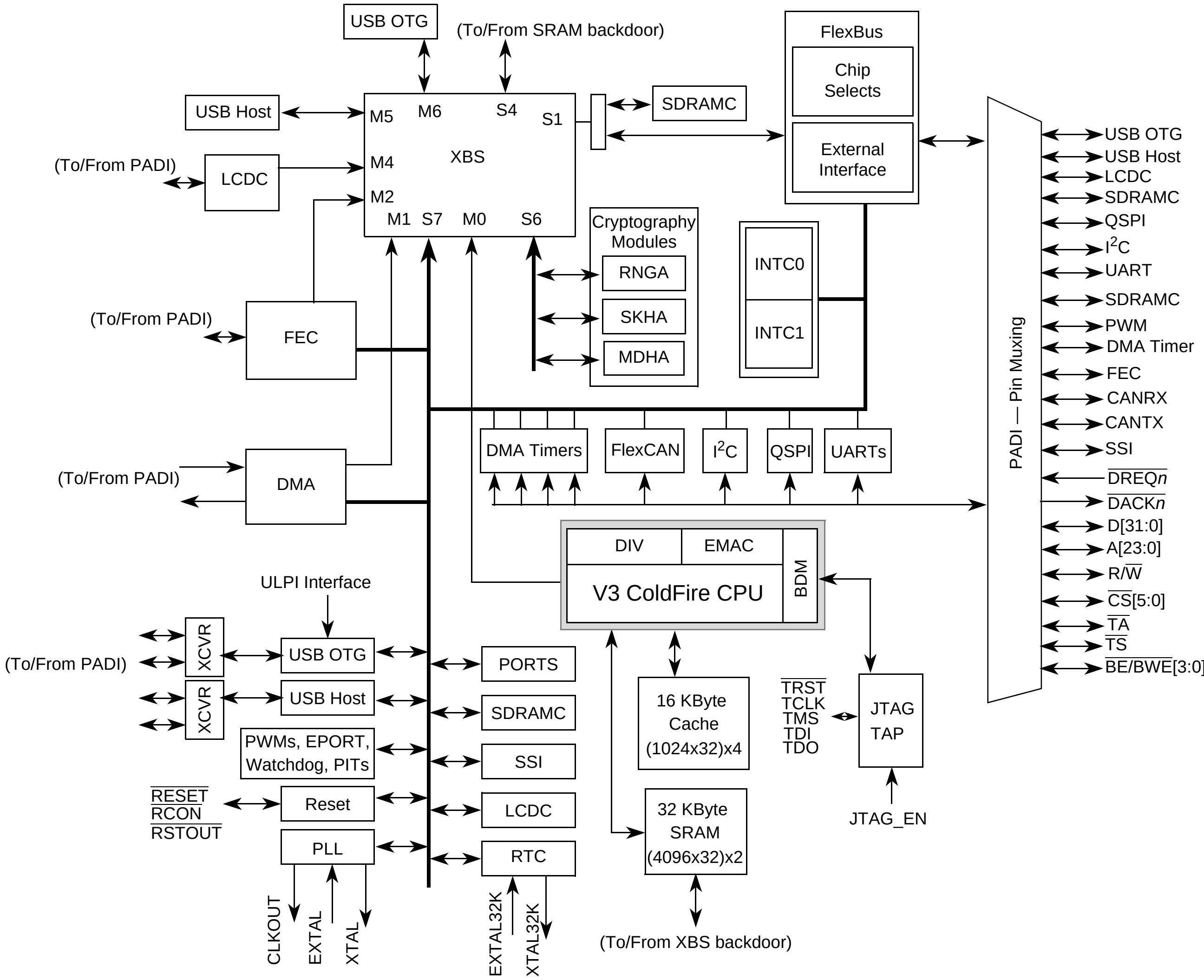


Figure 1. MCF5329 Block Diagram

1 MCF532*x* Family Comparison

The following table compares the various device derivatives available within the MCF532*x* family.

Table 1. MCF532*x* Family Configurations

Module	MCF5327	MCF5328	MCF53281	MCF5329
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•
Core (System) Clock	up to 240 MHz			
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 80 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 211			
Unified Cache	16 Kbytes			
Static RAM (SRAM)	32 Kbytes			

Table 1. MCF532*x* Family Configurations (continued)

Module	MCF5327	MCF5328	MCF53281	MCF5329
LCD Controller	•	•	•	•
SDR/DDR SDRAM Controller	•	•	•	•
USB 2.0 Host	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	—	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•
Fast Ethernet Controller (FEC)	—	•	•	•
Cryptography Hardware Accelerators	—	—	—	•
Embedded Voice-over-IP System Solution	—	—	•	—
FlexCAN 2.0B communication module	—	—	•	•
UARTs	3	3	3	3
I^2C	•	•	•	•
QSPI	•	•	•	•
PWM Module	•	•	•	•
Real Time Clock	•	•	•	•
32-bit DMA Timers	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•
FlexBus External Interface	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•
Package	196 MAPBGA	256 MAPBGA	256 MAPBGA	256 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5327CVM240	MCF5327 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF5328CVM240	MCF5328 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF53281CVM240	MCF53281 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF5329CVM240	MCF5329 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 2 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

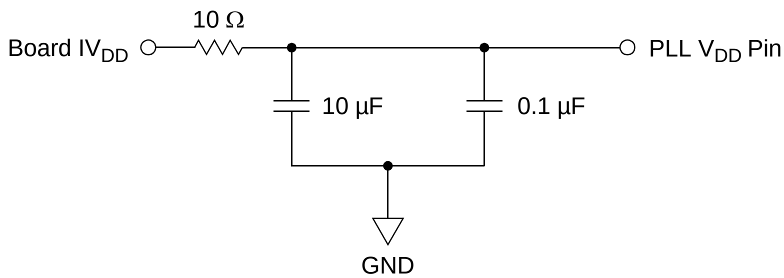


Figure 2. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 3 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

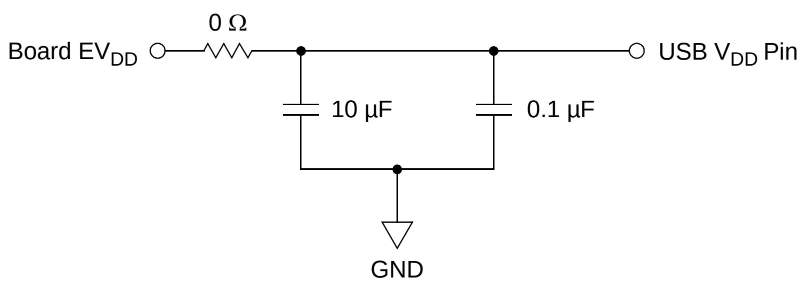


Figure 3. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there is

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
Mode Selection								
RCON[2]	—	—	—	I	EVDD	M7	M8	M8
DRAMSEL	—	—	—	I	EVDD	G11	H12	H12
FlexBus								
A[23:22]	—	FB_CS[5:4]	—	O	SDVDD	B11,C11	C13, D13	C13, D13
A[21:16]	—	—	—	O	SDVDD	B12, A12, D11, C12, B13, A13	E13, A14, B14, C14, A15, B15	E13, A14, B14, C14, A15, B15
A[15:14]	—	SD_BA[1:0][3]	—	O	SDVDD	A14, B14	D14, B16	D14, B16
A[13:11]	—	SD_A[13:11][3]	—	O	SDVDD	C13, C14, D12	C15, C16, D15	C15, C16, D15
A10	—	—	—	O	SDVDD	D13	D16	D16
A[9:0]	—	SD_A[9:0][3]	—	O	SDVDD	D14, E11–14, F11–F14, G14	E14–E16, F13–F16, G16– G14	E14–E16, F13–F16, G16– G14
D[31:16]	—	SD_D[31:16][4]	—	I/O	SDVDD	H3–H1, J4–J1, K1, L4, M2, M3, N1, N2, P1, P2, N3	M1–M4, N1–N4, T3, P4, R4, T4, N5, P5, R5, T5	M1–M4, N1–N4, T3, P4, R4, T4, N5, P5, R5, T5
D[15:1]	—	FB_D[31:17][4]	—	I/O	SDVDD	F4–F1, G5–G2, L5, N4, P4, M5, N5, P5, L6	J3–J1, K4–K1, L2, R6, N7, P7, R7, T7, P8, R8	J3–J1, K4–K1, L2, R6, N7, P7, R7, T7, P8, R8
D0[2]	—	FB_D[16][4]	—	I/O	SDVDD	M6	T8	T8
BE/BWE[3:0]	PBE[3:0]	SD_DQM[3:0][3]	—	O	SDVDD	H4, P3, G1, M4	L4, P6, L3, N6	L4, P6, L3, N6
OE	PBUSCTL3	—	—	O	SDVDD	P6	R9	R9
TA[2]	PBUSCTL2	—	—	I	SDVDD	G13	G13	G13
R/W	PBUSCTL1	—	—	O	SDVDD	N6	N8	N8
TS	PBUSCTL0	DACK0	—	O	SDVDD	D2	H4	H4
Chip Selects								
FB_CS[5:4]	PCS[5:4]	—	—	O	SDVDD	—	B13, A13	B13, A13
FB_CS[3:1]	PCS[3:1]			O	SDVDD	A11, D10, C10	A12, B12, C12	A12, B12, C12
FB_CS0	—	—	—	O	SDVDD	B10	D12	D12

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
USB Host & USB On-the-Go								
USBOTG_M	—	—	—	I/O	USB VDD	G12	L15	L15
USBOTG_P	—	—	—	I/O	USB VDD	H13	L16	L16
USBHOST_M	—	—	—	I/O	USB VDD	K13	M15	M15
USBHOST_P	—	—	—	I/O	USB VDD	J12	M16	M16
FlexCAN (MCF53281 & MCF5329 only)								
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA, SSI_RXD, or LCD_D16 for CANRX and I2C_SCL, SSI_TXD, or LCD_D17 for CANTX.								
PWM								
PWM7	PPWM7	—	—	I/O	EVDD	—	H13	H13
PWM5	PPWM5	—	—	I/O	EVDD	—	H14	H14
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	H14	H15	H15
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	J14	H16	H16
SSI								
SSI_MCLK	PSSI4	—	—	I/O	EVDD	—	G4	G4
SSI_BCLK	PSSI3	$\overline{\text{U2CTS}}$	PWM7	I/O	EVDD	—	F4	F4
SSI_FS	PSSI2	$\overline{\text{U2RTS}}$	PWM5	I/O	EVDD	—	G3	G3
SSI_RXD[2]	PSSI1	U2RXD	CANRX	I	EVDD	—	—	G2
SSI_TXD[2]	PSSI0	U2TXD	CANTX	O	EVDD	—	—	G1
SSI_RXD[2]	PSSI1	U2RXD	—	I	EVDD	—	G2	—
SSI_TXD[2]	PSSI0	U2TXD	—	O	EVDD	—	G1	—
I^2C								
I2C_SCL[2]	PFECI2C1	CANTX	U2TXD	I/O	EVDD	—	—	F3
I2C_SDA[2]	PFECI2C0	CANRX	U2RXD	I/O	EVDD	—	—	F2
I2C_SCL[2]	PFECI2C1	—	U2TXD	I/O	EVDD	E3	F3	—
I2C_SDA[2]	PFECI2C0	—	U2RXD	I/O	EVDD	E4	F2	—
DMA								
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.								

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
QSPI								
QSPI_CS2	PQSPI5	U2RTS	—	O	EVDD	P10	T12	T12
QSPI_CS1	PQSPI4	PWM7	USBOTG_ PU_EN	O	EVDD	L11	T13	T13
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	P11	P11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	N10	R12	R12
QSPI_DIN	PQSPI1	U2CTS	—	I	EVDD	L10	N12	N12
QSPI_DOUT	PQSPI0	I2C_SDA	—	O	EVDD	M10	P12	P12
UARTs								
U1CTS	PUARTL7	SSI_BCLK	—	I	EVDD	C9	D11	D11
U1RTS	PUARTL6	SSI_FS	—	O	EVDD	D9	E10	E10
U1TXD	PUARTL5	SSI_TXD[2]	—	O	EVDD	A9	E11	E11
U1RXD	PUARTL4	SSI_RXD[2]	—	I	EVDD	A10	E12	E12
U0CTS	PUARTL3	—	—	I	EVDD	P13	R15	R15
U0RTS	PUARTL2	—	—	O	EVDD	N12	T15	T15
U0TXD	PUARTL1	—	—	O	EVDD	P12	T14	T14
U0RXD	PUARTL0	—	—	I	EVDD	P11	R14	R14
Note: The UART2 signals are multiplexed on the QSPI, SSI, DMA Timers, and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	I	EVDD	C1	F1	F1
DT2IN	PTIMER2	DT2OUT	U2TXD	I	EVDD	B1	E1	E1
DT1IN	PTIMER1	DT1OUT	DACK1	I	EVDD	A1	E2	E2
DT0IN	PTIMER0	DT0OUT	DREQ0[2]	I	EVDD	C2	E3	E3
BDM/JTAG[6]								
JTAG_EN[7]	—	—	—	I	EVDD	L12	M13	M13
DSCLK	—	TRST[2]	—	I	EVDD	N14	P15	P15
PSTCLK	—	TCLK[2]	—	O	EVDD	L7	T9	T9
BKPT	—	TMS[2]	—	I	EVDD	M12	R16	R16
DSI	—	TDI[2]	—	I	EVDD	K12	N14	N14
DSO	—	TDO	—	O	EVDD	N9	N11	N11
DDATA[3:0]	—	—	—	O	EVDD	N7, P7, L8, M8	N9, P9, N10, P10	N9, P9, N10, P10

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
PST[3:0]	—	—	—	O	EVDD	N8, P8, L9, M9	R10, T10, R11, T11	R10, T10, R11, T11
Test								
TEST[7]	—	—	—	I	EVDD	E10	A16	A16
PLL_TEST[8]	—	—	—	I	EVDD	—	N13	N13
Power Supplies								
EVDD	—	—	—	—	—	E6, E7, F5–F7, H9, J8, J9, K8, K9, K11	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10
IVDD	—	—	—	—	—	E5, K5, K10, J10	E5, G12, M5, M11, M12	E5, G12, M5, M11, M12
PLL_VDD	—	—	—	—	—	H10	J12	J12
SD_VDD	—	—	—	—	—	E8, E9, F8–F10, J5–J7, K7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7
USB_VDD	—	—	—	—	—	G10	L14	L14
VSS	—	—	—	—	—	G6–G9, H6–H8, P9	G7–G10, H7–H10, J7–10, K7–K10, L12, L13	G7–G10, H7–H10, J7–10, K7–K10, L12, L13
PLL_VSS	—	—	—	—	—	H11	K13	K13
USB_VSS	—	—	—	—	—	H12	M14	M14

1 Refers to pin's primary function.
2 Pull-up enabled internally on this signal for this mode.
3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.
4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.
5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.
6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.
7 Pull-down enabled internally on this signal for this mode.
8 Must be left floating for proper operation of the PLL.

NOTE

4.2 Pinout—256 MAPBGA

Figure 4 shows a pinout of the MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 devices.

NOTE

The pin at location N13 (PLL_TEST) must be left floating or improper operation of the PLL module occurs.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	FEC_ TXCLK	LCD_ D4	LCD_ D5	LCD_ D9	FEC_ RXD2	LCD_ D15	FEC_ COL	LCD_ CLS	LCD_ LSCLK	LCD_ PS	FB_CS3	FB_CS4	A20	A17	TEST	A
B	FEC_ TXER	FEC_ TXEN	LCD_ D1	LCD_ D3	LCD_ D8	FEC_ RXD1	LCD_ D14	FEC_ CRS	LCD_ ACD/OE	LCD_LP/ HSYNC	LCD_ REV	FB_CS2	FB_CS5	A19	A16	A14	B
C	FEC_ MDC	FEC_ MDIO	LCD_ D0	LCD_ D2	LCD_ D7	FEC_ RXD0	LCD_ D13	FEC_ RXCLK	LCD_ D17	LCD_FLM/ VSYNC	LCD_ SPL_SPR	FB_CS1	A23	A18	A13	A12	C
D	FEC_ TXD1	FEC_ TXD2	FEC_ TXD3	FEC_ RXER	LCD_ D6	LCD_ D11	LCD_ D12	FEC_ RXDV	LCD_ D16	LCD_CON TRAST	U1CTS	FB_CS0	A22	A15	A11	A10	D
E	DT2IN	DT1IN	DT0IN	FEC_ TXD0	IVDD	LCD_ D10	FEC_ RXD3	EVDD	SD_VDD	U1RTS	U1TXD	U1RXD	A21	A9	A8	A7	E
F	DT3IN	I2C_ SDA	I2C_ SCL	SSI_ BCLK	EVDD	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	NC	A6	A5	A4	A3	F
G	SSI_ TXD	SSI_ RXD	SSI_FS	SSI_ MCLK	EVDD	EVDD	VSS	VSS	VSS	VSS	SD_VDD	IVDD	TA	A0	A1	A2	G
H	SD_ CS0	SD_CKE	SD_WE	TS	EVDD	EVDD	VSS	VSS	VSS	VSS	SD_VDD	DRAM SEL	PWM7	PWM5	PWM3	PWM1	H
J	D13	D14	D15	SD_CS1	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	EVDD	PLL_ VDD	IRQ7	IRQ6	IRQ5	IRQ4	J
K	D9	D10	D11	D12	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	EVDD	EVDD	PLL_ VSS	IRQ3	IRQ2	IRQ1	K
L	SD_ DQS3	D8	BE/ BWE1	BE/ BWE3	SD_VDD	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	EVDD	VSS	USB_ VSS	USBOTG _VDD	USB OTG_M	USB OTG_P	L
M	D31	D30	D29	D28	IVDD	SD_VDD	SD_VDD	RCON	EVDD	EVDD	IVDD	IVDD	JTAG_ EN	USBHOST _VSS	USB HOST_M	USB HOST_P	M
N	D27	D26	D25	D24	D19	BE/ BWE0	D6	R/W	DDATA3	DDATA1	TDO/ DSO	QSPI_ DIN	PLL_ TEST	TDI/DSI	RESET	XTAL	N
P	SD_DR _DQS	SD_A10	SD_CAS	D22	D18	BE/ BWE2	D5	D2	DDATA2	DDATA0	QSPI_ CS0	QSPI_ DOUT	EXTAL 32K	RSTOUT	TRST/ DSCLK	EXTAL	P
R	SD_CLK	SD_CLK	SD_RAS	D21	D17	D7	D4	D1	OE	PST3	PST1	QSPI_ CLK	XTAL 32K	U0RXD	U0CTS	TMS/ BKPT	R
T	NC	FB_CLK	D23	D20	D16	SD_ DQS2	D3	D0	TCLK/ PSTCLK	PST2	PST0	QSPI_ CS2	QSPI_ CS1	U0TXD	U0RTS	NC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 Pinout Top View (256 MAPBGA)

4.3 Pinout—196 MAPBGA

The pinout for the MCF5327CVM240 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DT1IN	LCD_D4	LCD_D5	LCD_D9	LCD_D13	LCD_D17	LCD_FLM/VSYNC	LCD_LP/HSYNC	U1TXD	U1RXD	FB_CS3	A20	A16	A15	A
B	D2TIN	LCD_D0	LCD_D6	LCD_D8	LCD_D12	LCD_D16	LCD_CONTRAST	LCD_LSCLK	LCD_SPL_SPR	FB_CS0	A23	A21	A17	A14	B
C	DT3IN	DT0IN	LCD_D2	LCD_D7	LCD_D11	LCD_D15	LCD_CLS	LCD_PS	U1CTS	FB_CS1	A22	A18	A13	A12	C
D	SD_WE	TS	LCD_D1	LCD_D3	LCD_D10	LCD_D14	LCD_ACD/OE	LCD_REV	U1RTS	FB_CS2	A19	A11	A10	A9	D
E	SD_CKE	SD_CS0	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	A8	A7	A6	A5	E
F	D12	D13	D14	D15	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	A4	A3	A2	A1	F
G	BE/BWE1	D8	D9	D10	D11	VSS	VSS	VSS	VSS	USB OTG_VDD	DRAM SEL	USB OTG_M	TA	A0	G
H	D29	D30	D31	BE/BWE3	SD_DQS3	VSS	VSS	VSS	EVDD	PLL_VDD	PLL_VSS	USBHOST_VSS	USB OTG_P	PWM3	H
J	D25	D26	D27	D28	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	RESET	USB HOST_P	IRQ7	PWM1	J
K	D24	SD_CLK	SD_CLK	SD_DR_DQS	IVDD	SD_DQS2	SD_VDD	EVDD	EVDD	IVDD	EVDD	TDI/DSI	USB HOST_M	XTAL	K
L	FB_CLK	SD_A10	SD_CAS	D23	D7	D1	TCLK/PSTCLK	DDATA1	PST1	QSPI_DIN	QSPI_CS1	JTAG_EN	IRQ4	EXTAL	L
M	SD_RAS	D22	D21	BE/BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_DOUT	EXTAL32K	TMS/BKPT	IRQ2	IRQ3	M
N	D20	D19	D16	D6	D3	R/W	DDATA3	PST3	TDO/DSO	QSPI_CLK	XTAL32K	U0RTS	IRQ1	TRST/DSCLK	N
P	D18	D17	BE/BWE2	D5	D2	OE	DDATA2	PST2	VSS	QSPI_CS2	U0RXD	U0TXD	U0CTS	RSTOUT	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 5. MCF5327CVM240 Pinout Top View (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5329 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5329.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A $(T_L - T_H)$	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

1 Functional operating conditions are given in Section 5.4, "DC Electrical Specifications." Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 6. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} – 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} – 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3 V_{SS} – 0.3	 0.45 0.8 0.8	V

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} – 0.35 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current $V_{in} = V_{DD}$ or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	μA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	μA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 8. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488×10^{-6} 163×10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF

Table 8. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
12	Crystal capacitive load	C_L		See crystal spec	
13	Discrete load capacitance for XTAL	C_{L_XTAL}		$2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}		$2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 10 TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$	f_{vco}	350	540	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.

2 All internal registers retain data at 0 Hz.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This parameter is guaranteed by design rather than 100% tested.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10 µs, or equivalently the modulation rate is 100 KHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 9 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 9 are shown in Figure 7 and Figure 8.

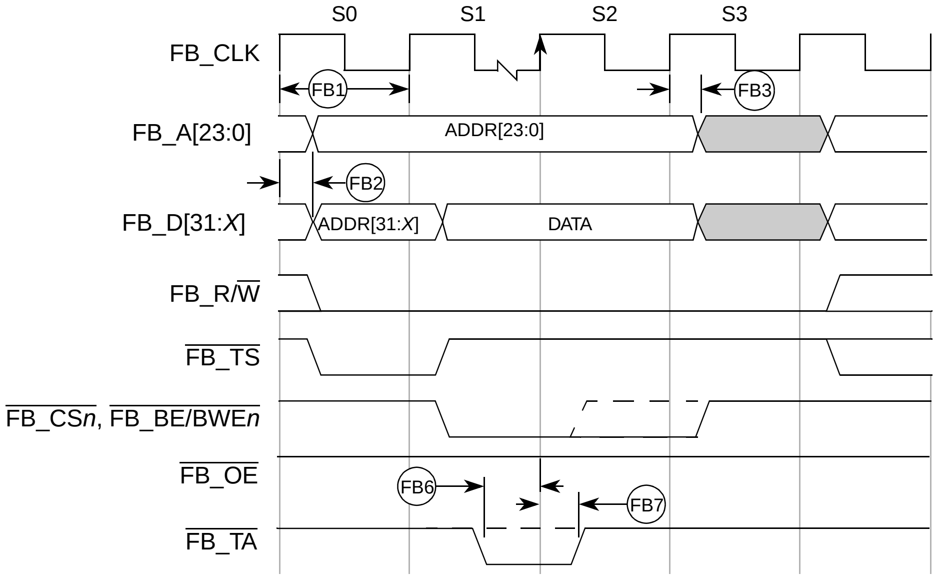


Figure 8. FlexBus Write Timing

5.7 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must remain supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 10. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit
•	Frequency of Operation[1]	•	60	80	MHz
SD1	Clock Period[2]	t_{SDCK}	12.5	16.67	ns
SD3	Pulse Width High[3]	t_{SDCKH}	0.45	0.55	SD_CLK
SD4	Pulse Width Low[4]	t_{SDCKH}	0.45	0.55	SD_CLK
SD5	Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns
SD6	Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns
SD7	SD_SDR_DQS Output Valid[5]	t_{DQSOV}	—	Self timed	ns
SD8	SD_DQS[3:0] input setup relative to SD_CLK[6]	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns

Table 15. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Number	Description	Minimum	Value	Unit
T1	End of LCD_OE to beginning of LCD_VSYNC	T5+T6+T7-1	(VWAIT1·T2)+T5+T6+T7-1	Ts
T2	LCD_HSYNC period	—	XMAX+T5+T6+T7	Ts
T3	LCD_VSYNC pulse width	T2	VWIDTH·T2	Ts
T4	End of LCD_VSYNC to beginning of LCD_OE	1	(VWAIT2·T2)+1	Ts
T5	LCD_HSYNC pulse width	1	HWIDTH+1	Ts
T6	End of LCD_HSYNC to beginning to LCD_OE	3	HWAIT2+3	Ts
T7	End of LCD_OE to beginning of LCD_HSYNC	1	HWAIT1+1	Ts

Note: Ts is the LCD_LSCLK period. LCD_VSYNC, LCD_HSYNC and LCD_OE can be programmed as active high or active low. In Figure 16, all 3 signals are active low. LCD_LSCLK can be programmed to be deactivated during the LCD_VSYNC pulse or the LCD_OE deasserted period. In Figure 16, LCD_LSCLK is always active.

Note: XMAX is defined in number of pixels in one line.

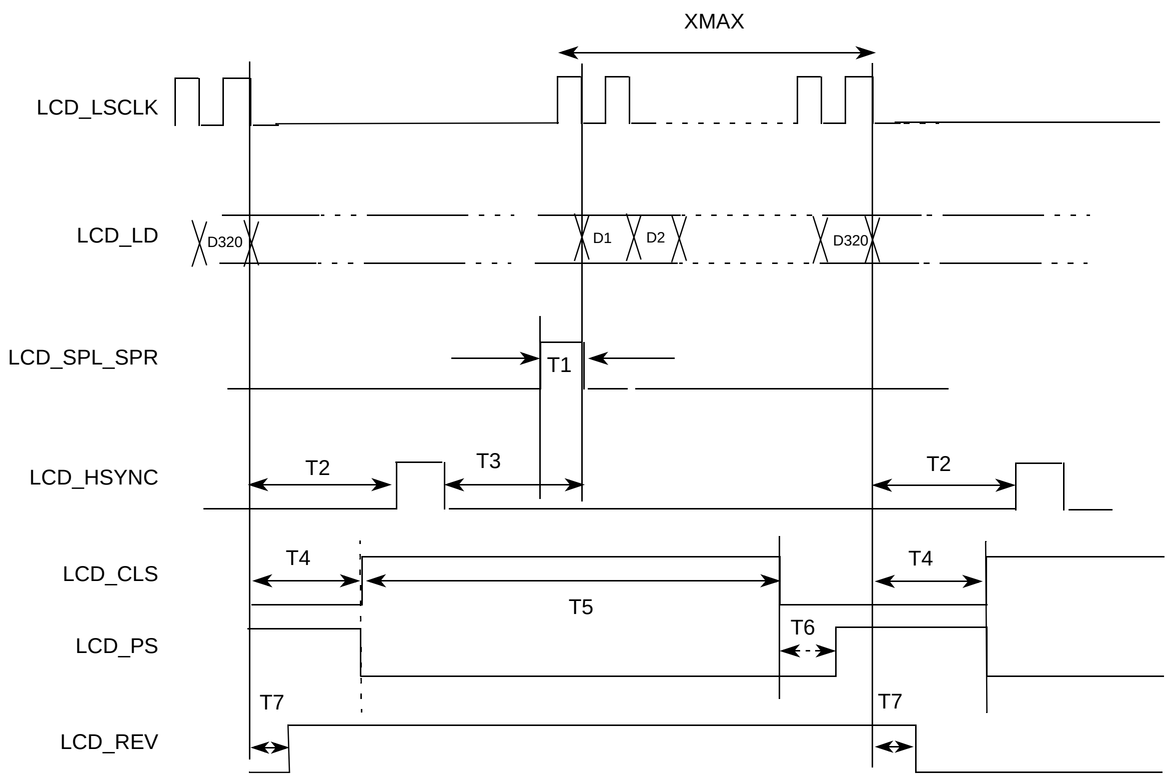


Figure 17. Sharp TFT Panel Timing

5.11 USB On-The-Go

The MCF5329 device is compliant with industry standard USB 2.0 specification.

5.12 ULPI Timing Specification

Control and data timing requirements for the ULPI pins are given in Table 18. These timings apply in synchronous mode only. All timings are measured with either a 60 MHz input clock from the USB_CLKIN pin. The USB_CLKIN needs to maintain a 50% duty cycle. Control signals and 8-bit data are always clocked on the rising edge.

The ULPI interface on the MCF5329 processor is compliant with the industry standard definition.

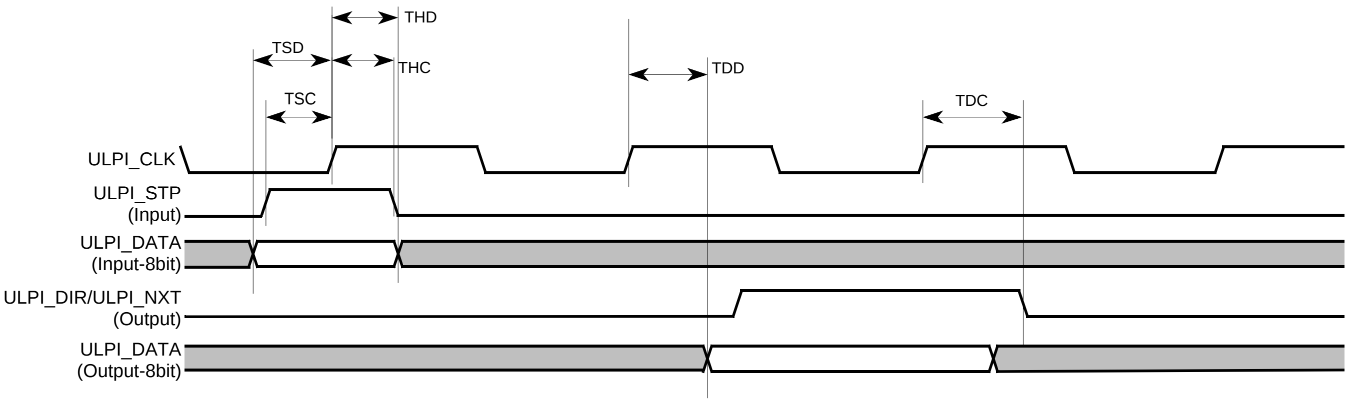


Figure 19. ULPI Timing Diagram

Table 18. ULPI Interface Timing

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	TSC, TSD	—	3.0	ns
Hold time (control in, 8-bit data in)	THC, THD	–1.5	—	ns
Output delay (control out, 8-bit data out)	TDC, TDD	—	6.0	ns

5.13 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 19. SSI Timing – Master Modes[1]

Num	Description	Symbol	Min	Max	Units
S1	SSI_MCLK cycle time[2]	t_{MCLK}	$8 \times t_{SYS}$	—	ns
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}
S3	SSI_BCLK cycle time[3]	t_{BCLK}	$8 \times t_{SYS}$	—	ns
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}
S5	SSI_BCLK to SSI_FS output valid		—	15	ns

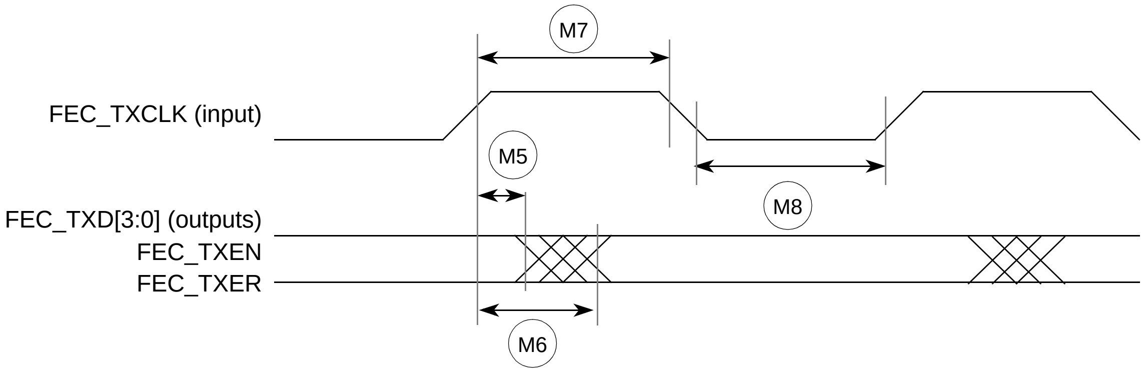


Figure 24. MII Transmit Signal Timing Diagram

5.15.3 MII Async Inputs Signal Timing

Table 25 lists MII asynchronous inputs signal timing.

Table 25. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

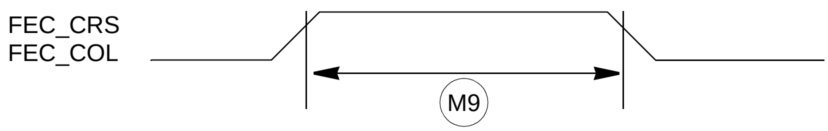


Figure 25. MII Async Inputs Timing Diagram

5.15.4 MII Serial Management Channel Timing

Table 26 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 26. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Table 31. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage	58 MHz (Typ)[3]	64 MHz (Typ)[3]	72 MHz (Typ)[3]	80 MHz (Typ)[3]	80 MHz (Peak)[4]	Units
Stop Mode 3 (Stop 11)[5]	3.3 V	3.9	3.92	4.0	4.0	4.0	mA
	1.5 V	1.04	1.04	1.04	1.04	1.08	
Stop Mode 2 (Stop 10)[4]	3.3 V	4.69	4.72	4.8	4.8	4.8	
	1.5 V	2.69	2.69	2.70	2.70	2.75	
Stop Mode 1(Stop 01)[4]	3.3 V	4.72	4.73	4.81	4.81	4.81	
	1.5 V	15.28	16.44	17.85	19.91	20.42	
Stop Mode 0 (Stop 00)[4]	3.3 V	21.65	21.68	24.33	26.13	26.16	
	1.5 V	15.47	16.63	18.06	20.12	20.67	
Wait/Doze	3.3 V	22.49	22.52	25.21	27.03	39.8	
	1.5 V	26.79	28.85	30.81	34.47	97.4	
Run	3.3 V	33.61	33.61	42.3	50.5	62.6	
	1.5 V	56.3	60.7	65.4	73.4	132.3	

1 All values are measured with a 3.30V EV_{DD}, 3.30V SDV_{DD} and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.

2 Refer to the Power Management chapter in the *MCF532x Reference Manual* for more information on low-power modes.

3 All peripheral clocks except UART0, FlexBus, INTC0, reset controller, PLL, and edge port off before entering low power mode. All code executed from flash.

4 All peripheral clocks on before entering low power mode. All code is executed from flash.

5 See the description of the low-power control register (LCPR) in the *MCF532x Reference Manual* for more information on stop modes 0–3.

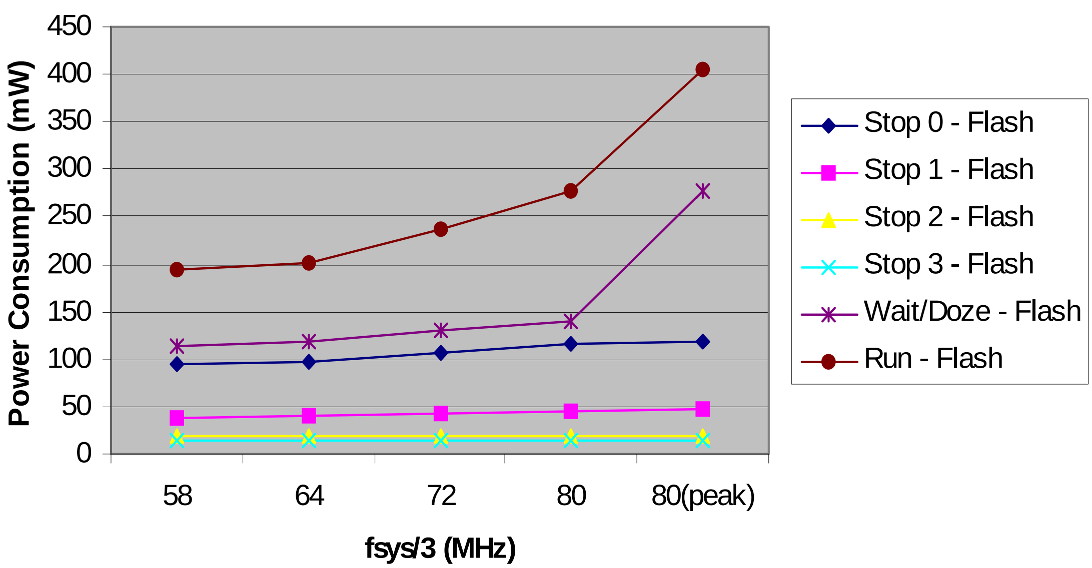
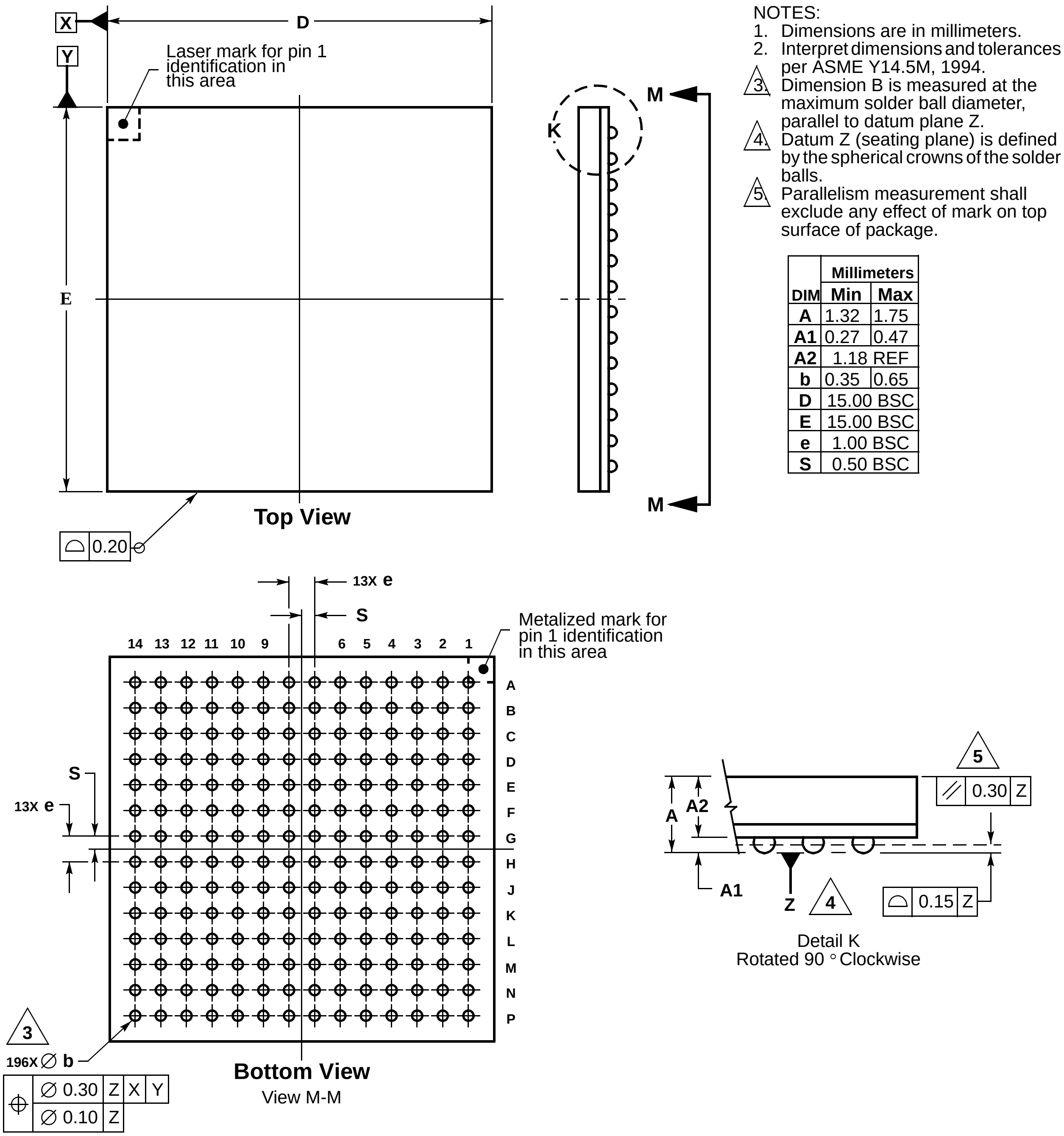


Figure 34. Current Consumption in Low-Power Modes

7.2 Package Dimensions—196 MAPBGA

Figure 37 shows the MCF5327CVM240 package dimensions.



DIM	Millimeters Min	Millimeters Max
A	1.32	1.75
A1	0.27	0.47
A2	1.18 REF	
b	0.35	0.65
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 37. 196 MAPBGA Package Dimensions (Case No. 1128A-01)