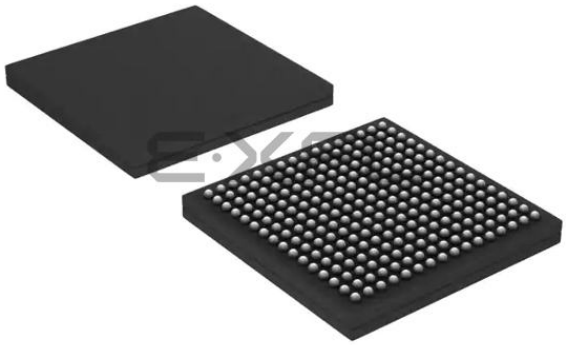

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SSI, UART/USART, USB, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	94
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5329cvm240j

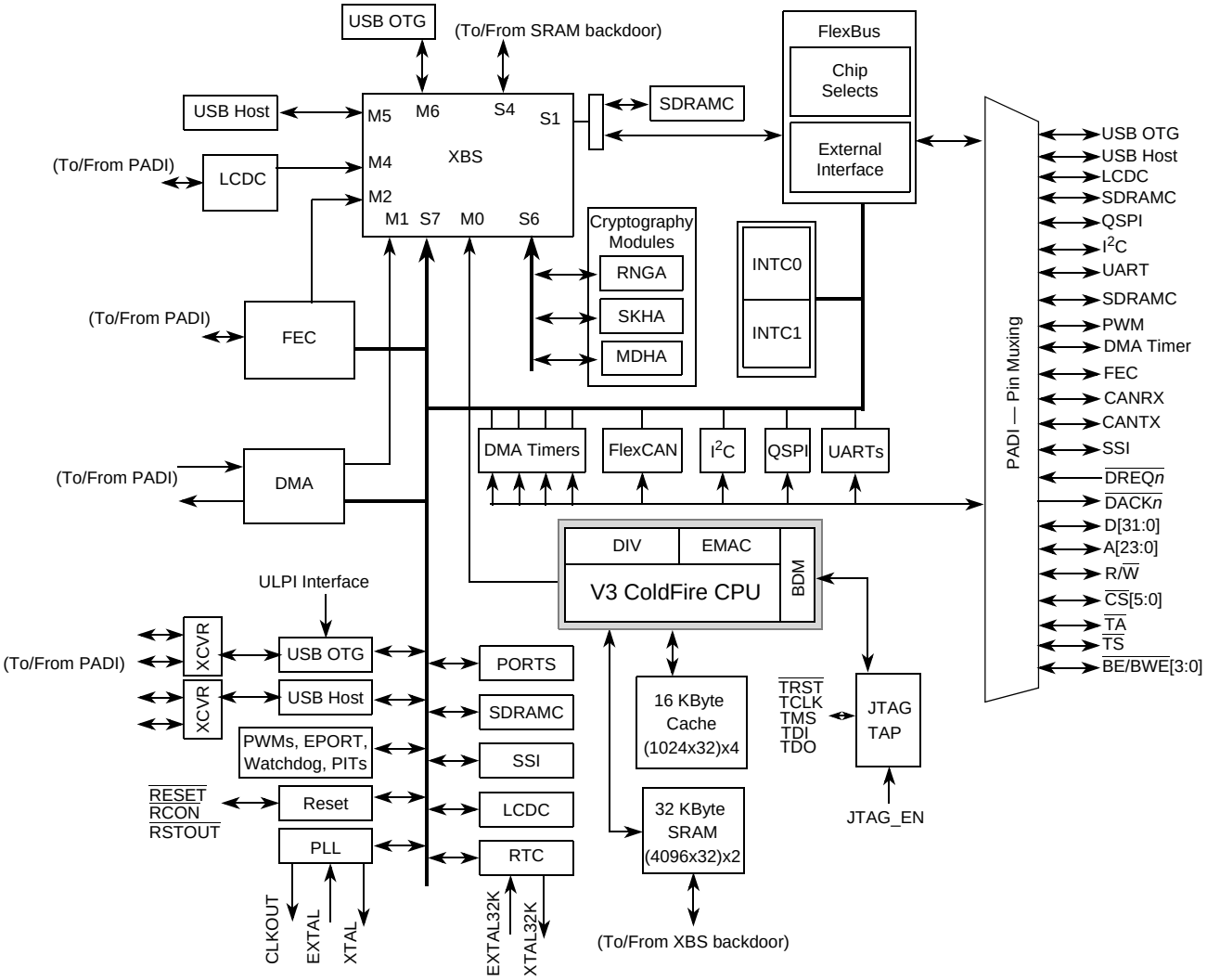


Figure 1. MCF5329 Block Diagram

1 MCF532*x* Family Comparison

The following table compares the various device derivatives available within the MCF532*x* family.

Table 1. MCF532*x* Family Configurations

Module	MCF5327	MCF5328	MCF53281	MCF5329
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•
Core (System) Clock	up to 240 MHz			
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 80 MHz			
Performance (Dhrystone/2.1 MIPS)	up to 211			
Unified Cache	16 Kbytes			
Static RAM (SRAM)	32 Kbytes			

Table 1. MCF532*x* Family Configurations (continued)

Module	MCF5327	MCF5328	MCF53281	MCF5329
LCD Controller	•	•	•	•
SDR/DDR SDRAM Controller	•	•	•	•
USB 2.0 Host	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•
UTMI+ Low Pin Interface (ULPI)	—	•	•	•
Synchronous Serial Interface (SSI)	•	•	•	•
Fast Ethernet Controller (FEC)	—	•	•	•
Cryptography Hardware Accelerators	—	—	—	•
Embedded Voice-over-IP System Solution	—	—	•	—
FlexCAN 2.0B communication module	—	—	•	•
UARTs	3	3	3	3
I^2C	•	•	•	•
QSPI	•	•	•	•
PWM Module	•	•	•	•
Real Time Clock	•	•	•	•
32-bit DMA Timers	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•
FlexBus External Interface	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•
Package	196 MAPBGA	256 MAPBGA	256 MAPBGA	256 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF5327CVM240	MCF5327 RISC Microprocessor	196 MAPBGA	240 MHz	–40° to +85° C
MCF5328CVM240	MCF5328 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF53281CVM240	MCF53281 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF5329CVM240	MCF5329 RISC Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 2 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

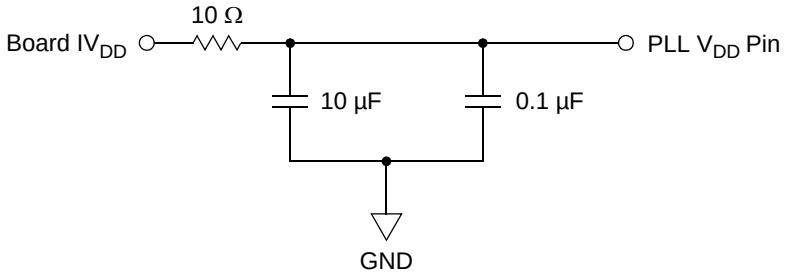


Figure 2. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 3 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

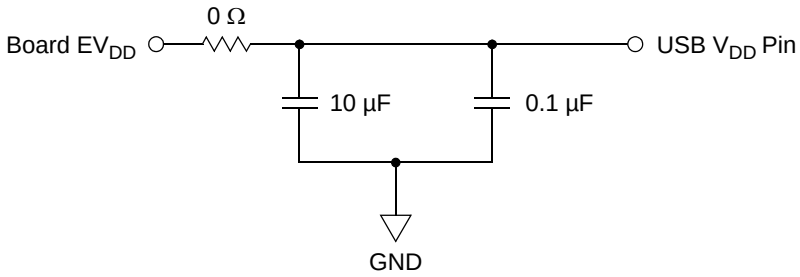


Figure 3. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there is

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
SDRAM Controller								
SD_A10	—	—	—	O	SDVDD	L2	P2	P2
SD_CKE	—	—	—	O	SDVDD	E1	H2	H2
SD_CLK	—	—	—	O	SDVDD	K3	R1	R1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	K2	R2	R2
$\overline{\text{SD\_CS1}}$	—	—	—	O	SDVDD	—	J4	J4
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	E2	H1	H1
SD_DQS3	—	—	—	O	SDVDD	H5	L1	L1
SD_DQS2	—	—	—	O	SDVDD	K6	T6	T6
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	L3	P3	P3
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	M1	R3	R3
SD_SDR_DQS	—	—	—	O	SDVDD	K4	P1	P1
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	D1	H3	H3
External Interrupts Port[5]								
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	J13	J13	J13
$\overline{\text{IRQ6}}$[2]	PIRQ6[2]	USBHOST_ VBUS_EN	—	I	EVDD	—	J14	J14
$\overline{\text{IRQ5}}$[2]	PIRQ5[2]	USBHOST_ VBUS_OC	—	I	EVDD	—	J15	J15
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	SSI_MCLK	—	I	EVDD	L13	J16	J16
$\overline{\text{IRQ3}}$[2]	PIRQ3[2]	—	—	I	EVDD	M14	K14	K14
$\overline{\text{IRQ2}}$[2]	PIRQ2[2]	USB_CLKIN	—	I	EVDD	M13	K15	K15
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	$\overline{\text{DREQ1}}$[2]	SSI_CLKIN	I	EVDD	N13	K16	K16
FEC								
FEC_MDC	PFECI2C3	I2C_SCL[2]	—	O	EVDD	—	C1	C1
FEC_MDIO	PFECI2C2	I2C_SDA[2]	—	I/O	EVDD	—	C2	C2
FEC_TXCLK	PFECH7	—	—	I	EVDD	—	A2	A2
FEC_TXEN	PFECH6	—	—	O	EVDD	—	B2	B2
FEC_TXD0	PFECH5	ULPI_DATA0	—	O	EVDD	—	E4	E4
FEC_COL	PFECH4	ULPI_CLK	—	I	EVDD	—	A8	A8
FEC_RXCLK	PFECH3	ULPI_NXT	—	I	EVDD	—	C8	C8
FEC_RXDV	PFECH2	ULPI_STP	—	I	EVDD	—	D8	D8
FEC_RXD0	PFECH1	ULPI_DATA4	—	I	EVDD	—	C6	C6

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
USB Host & USB On-the-Go								
USBOTG_M	—	—	—	I/O	USB VDD	G12	L15	L15
USBOTG_P	—	—	—	I/O	USB VDD	H13	L16	L16
USBHOST_M	—	—	—	I/O	USB VDD	K13	M15	M15
USBHOST_P	—	—	—	I/O	USB VDD	J12	M16	M16
FlexCAN (MCF53281 & MCF5329 only)								
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA, SSI_RXD, or LCD_D16 for CANRX and I2C_SCL, SSI_TXD, or LCD_D17 for CANTX.								
PWM								
PWM7	PPWM7	—	—	I/O	EVDD	—	H13	H13
PWM5	PPWM5	—	—	I/O	EVDD	—	H14	H14
PWM3	PPWM3	DT3OUT	DT3IN	I/O	EVDD	H14	H15	H15
PWM1	PPWM1	DT2OUT	DT2IN	I/O	EVDD	J14	H16	H16
SSI								
SSI_MCLK	PSSI4	—	—	I/O	EVDD	—	G4	G4
SSI_BCLK	PSSI3	$\overline{\text{U2CTS}}$	PWM7	I/O	EVDD	—	F4	F4
SSI_FS	PSSI2	$\overline{\text{U2RTS}}$	PWM5	I/O	EVDD	—	G3	G3
SSI_RXD[2]	PSSI1	U2RXD	CANRX	I	EVDD	—	—	G2
SSI_TXD[2]	PSSI0	U2TXD	CANTX	O	EVDD	—	—	G1
SSI_RXD[2]	PSSI1	U2RXD	—	I	EVDD	—	G2	—
SSI_TXD[2]	PSSI0	U2TXD	—	O	EVDD	—	G1	—
I^2C								
I2C_SCL[2]	PFECI2C1	CANTX	U2TXD	I/O	EVDD	—	—	F3
I2C_SDA[2]	PFECI2C0	CANRX	U2RXD	I/O	EVDD	—	—	F2
I2C_SCL[2]	PFECI2C1	—	U2TXD	I/O	EVDD	E3	F3	—
I2C_SDA[2]	PFECI2C0	—	U2RXD	I/O	EVDD	E4	F2	—
DMA								
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.								

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
QSPI								
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	EVDD	P10	T12	T12
QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	O	EVDD	L11	T13	T13
QSPI_CS0	PQSPI3	PWM5	—	O	EVDD	—	P11	P11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	EVDD	N10	R12	R12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	EVDD	L10	N12	N12
QSPI_DOUT	PQSPI0	I2C_SDA	—	O	EVDD	M10	P12	P12
UARTs								
$\overline{\text{U1CTS}}$	PUARTL7	SSI_BCLK	—	I	EVDD	C9	D11	D11
$\overline{\text{U1RTS}}$	PUARTL6	SSI_FS	—	O	EVDD	D9	E10	E10
U1TXD	PUARTL5	SSI_TXD[2]	—	O	EVDD	A9	E11	E11
U1RXD	PUARTL4	SSI_RXD[2]	—	I	EVDD	A10	E12	E12
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	EVDD	P13	R15	R15
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	EVDD	N12	T15	T15
U0TXD	PUARTL1	—	—	O	EVDD	P12	T14	T14
U0RXD	PUARTL0	—	—	I	EVDD	P11	R14	R14
Note: The UART2 signals are multiplexed on the QSPI, SSI, DMA Timers, and I2C pins.								
DMA Timers								
DT3IN	PTIMER3	DT3OUT	U2RXD	I	EVDD	C1	F1	F1
DT2IN	PTIMER2	DT2OUT	U2TXD	I	EVDD	B1	E1	E1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{DACK1}}$	I	EVDD	A1	E2	E2
DT0IN	PTIMER0	DT0OUT	$\overline{\text{DREQ0}}$[2]	I	EVDD	C2	E3	E3
BDM/JTAG[6]								
JTAG_EN[7]	—	—	—	I	EVDD	L12	M13	M13
DSCLK	—	$\overline{\text{TRST}}$[2]	—	I	EVDD	N14	P15	P15
PSTCLK	—	TCLK[2]	—	O	EVDD	L7	T9	T9
$\overline{\text{BKPT}}$	—	TMS[2]	—	I	EVDD	M12	R16	R16
DSI	—	TDI[2]	—	I	EVDD	K12	N14	N14
DSO	—	TDO	—	O	EVDD	N9	N11	N11
DDATA[3:0]	—	—	—	O	EVDD	N7, P7, L8, M8	N9, P9, N10, P10	N9, P9, N10, P10

Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF53281 MCF5329 256 MAPBGA
PST[3:0]	—	—	—	O	EVDD	N8, P8, L9, M9	R10, T10, R11, T11	R10, T10, R11, T11
Test								
TEST[7]	—	—	—	I	EVDD	E10	A16	A16
PLL_TEST[8]	—	—	—	I	EVDD	—	N13	N13
Power Supplies								
EVDD	—	—	—	—	—	E6, E7, F5–F7, H9, J8, J9, K8, K9, K11	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10
IVDD	—	—	—	—	—	E5, K5, K10, J10	E5, G12, M5, M11, M12	E5, G12, M5, M11, M12
PLL_VDD	—	—	—	—	—	H10	J12	J12
SD_VDD	—	—	—	—	—	E8, E9, F8–F10, J5–J7, K7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7
USB_VDD	—	—	—	—	—	G10	L14	L14
VSS	—	—	—	—	—	G6–G9, H6–H8, P9	G7–G10, H7–H10, J7–10, K7–K10, L12, L13	G7–G10, H7–H10, J7–10, K7–K10, L12, L13
PLL_VSS	—	—	—	—	—	H11	K13	K13
USB_VSS	—	—	—	—	—	H12	M14	M14

1 Refers to pin's primary function.

2 Pull-up enabled internally on this signal for this mode.

3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.

4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

7 Pull-down enabled internally on this signal for this mode.

8 Must be left floating for proper operation of the PLL.

NOTE

4.2 Pinout—256 MAPBGA

Figure 4 shows a pinout of the MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 devices.

NOTE

The pin at location N13 (PLL_TEST) must be left floating or improper operation of the PLL module occurs.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	FEC_ TXCLK	LCD_ D4	LCD_ D5	LCD_ D9	FEC_ RXD2	LCD_ D15	FEC_ COL	LCD_ CLS	LCD_ LSCLK	LCD_ PS	FB_CS3	FB_CS4	A20	A17	TEST	A
B	FEC_ TXER	FEC_ TXEN	LCD_ D1	LCD_ D3	LCD_ D8	FEC_ RXD1	LCD_ D14	FEC_ CRS	LCD_ ACD/OE	LCD_LP/ HSYNC	LCD_ REV	FB_CS2	FB_CS5	A19	A16	A14	B
C	FEC_ MDC	FEC_ MDIO	LCD_ D0	LCD_ D2	LCD_ D7	FEC_ RXD0	LCD_ D13	FEC_ RXCLK	LCD_ D17	LCD_FLM/ VSYNC	LCD_ SPL_SPR	FB_CS1	A23	A18	A13	A12	C
D	FEC_ TXD1	FEC_ TXD2	FEC_ TXD3	FEC_ RXER	LCD_ D6	LCD_ D11	LCD_ D12	FEC_ RXDV	LCD_ D16	LCD_CON TRAST	U1CTS	FB_CS0	A22	A15	A11	A10	D
E	DT2IN	DT1IN	DT0IN	FEC_ TXD0	IVDD	LCD_ D10	FEC_ RXD3	EVDD	SD_VDD	U1RTS	U1TXD	U1RXD	A21	A9	A8	A7	E
F	DT3IN	I2C_ SDA	I2C_ SCL	SSI_ BCLK	EVDD	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	NC	A6	A5	A4	A3	F
G	SSI_ TXD	SSI_ RXD	SSI_FS	SSI_ MCLK	EVDD	EVDD	VSS	VSS	VSS	VSS	SD_VDD	IVDD	TA	A0	A1	A2	G
H	SD_ CS0	SD_CKE	SD_WE	TS	EVDD	EVDD	VSS	VSS	VSS	VSS	SD_VDD	DRAM SEL	PWM7	PWM5	PWM3	PWM1	H
J	D13	D14	D15	SD_CS1	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	EVDD	PLL_ VDD	IRQ7	IRQ6	IRQ5	IRQ4	J
K	D9	D10	D11	D12	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	EVDD	EVDD	PLL_ VSS	IRQ3	IRQ2	IRQ1	K
L	SD_ DQS3	D8	BE/ BWE1	BE/ BWE3	SD_VDD	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	EVDD	VSS	USB_ VSS	USBOTG _VDD	USB OTG_M	USB OTG_P	L
M	D31	D30	D29	D28	IVDD	SD_VDD	SD_VDD	RCON	EVDD	EVDD	IVDD	IVDD	JTAG_ EN	USBHOST _VSS	USB HOST_M	USB HOST_P	M
N	D27	D26	D25	D24	D19	BE/ BWE0	D6	R/W	DDATA3	DDATA1	TDO/ DSO	QSPI_ DIN	PLL_ TEST	TDI/DSI	RESET	XTAL	N
P	SD_DR _DQS	SD_A10	SD_CAS	D22	D18	BE/ BWE2	D5	D2	DDATA2	DDATA0	QSPI_ CS0	QSPI_ DOUT	EXTAL 32K	RSTOUT	TRST/ DSCLK	EXTAL	P
R	SD_CLK	SD_CLK	SD_RAS	D21	D17	D7	D4	D1	OE	PST3	PST1	QSPI_ CLK	XTAL 32K	U0RXD	U0CTS	TMS/ BKPT	R
T	NC	FB_CLK	D23	D20	D16	SD_ DQS2	D3	D0	TCLK/ PSTCLK	PST2	PST0	QSPI_ CS2	QSPI_ CS1	U0TXD	U0RTS	NC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 Pinout Top View (256 MAPBGA)

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 6. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} – 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} _ 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3 V_{SS} – 0.3	 0.45 0.8 0.8	V

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} – 0.35 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 8. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488 x 10^{-6} 163 x 10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}		1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}		1.5	pF

Table 9. FlexBus AC Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns
FB6	Transfer Acknowledge ($\overline{TA}$) Input Setup	t_{CVFBCH}	4	—	ns
FB7	Transfer Acknowledge ($\overline{TA}$) Input Hold	t_{CIFBCH}	0	—	ns

1 Timing for chip selects only applies to the $\overline{FB\_CS}$[5:0] signals. Please see Section 5.7.2, "DDR SDRAM AC Timing Characteristics" for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the *Reference Manual* for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

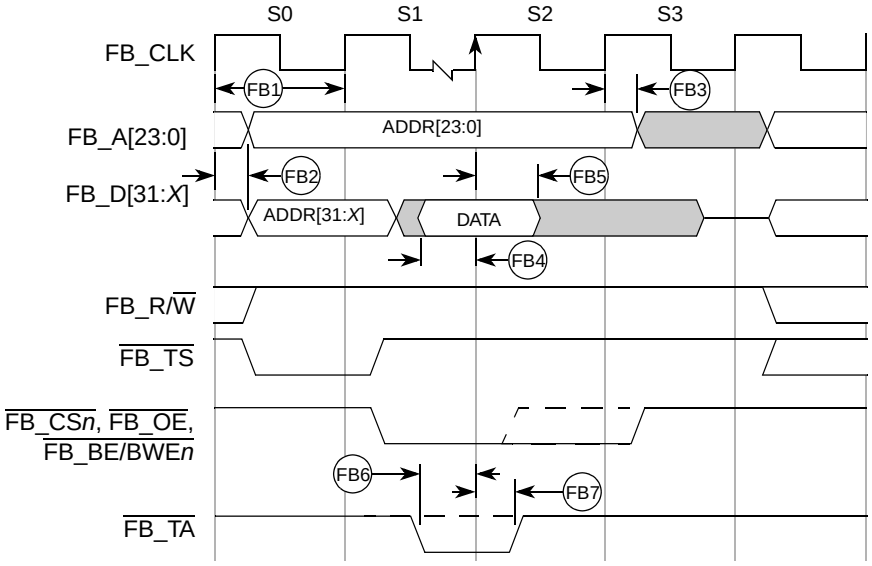


Figure 7. FlexBus Read Timing

Table 11. DDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)[6]	t_{DQDMI}	1.0	—	ns
DD9	Input Data Skew Relative to DQS (Input Setup)[7]	t_{DVDQ}	—	1	ns
DD10	Input Data Hold Relative to DQS[8]	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK
DD14	DQS output write preamble width	t_{DQWPRE}	0.25		SD_CLK
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK

1 SD_CLK is one SDRAM clock in (ns).

2 Pulse width high plus pulse width low cannot exceed min and max clock period.

3 Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

4 This specification relates to the required input setup time of today's DDR memories. The processor's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

5 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

6 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

7 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

8 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

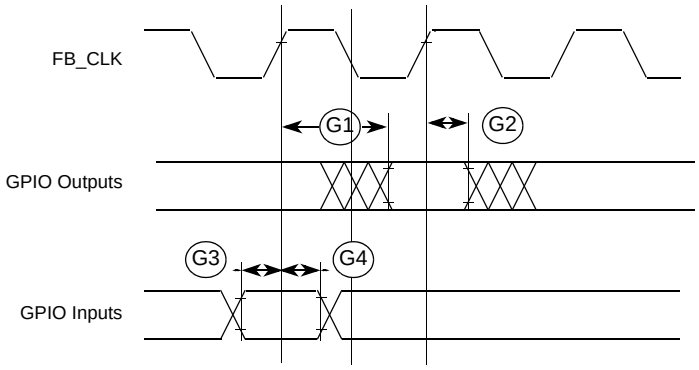


Figure 13. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 13. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

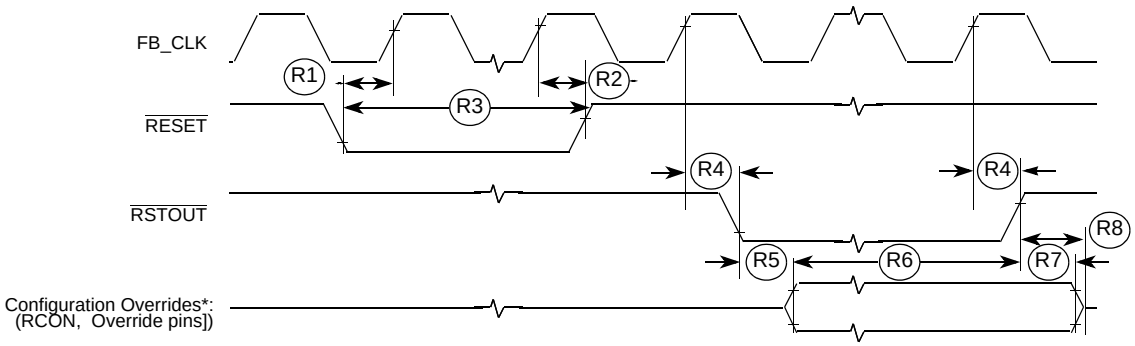


Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF5329 Reference Manual* for more information.

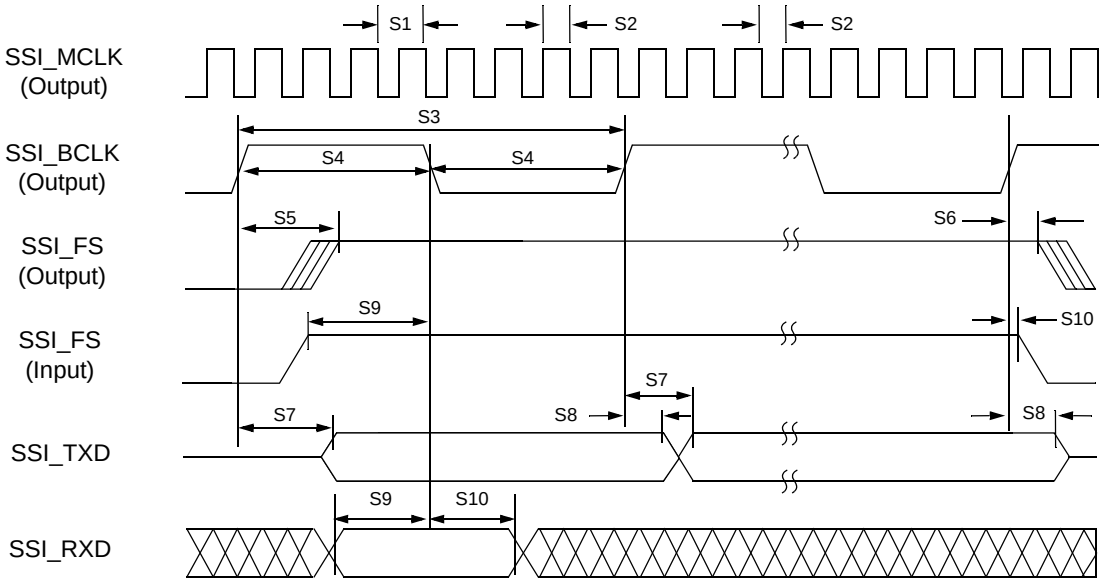


Figure 20. SSI Timing – Master Modes

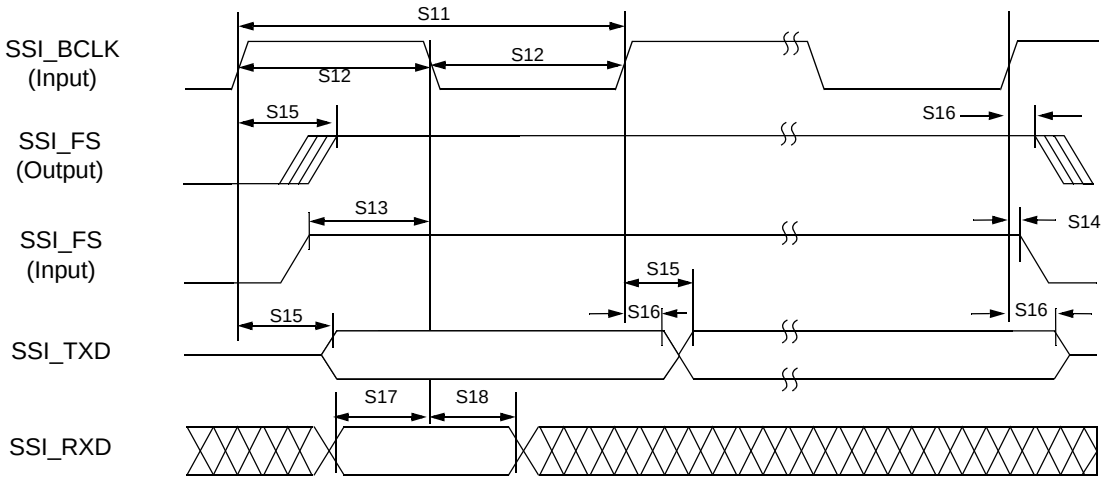


Figure 21. SSI Timing – Slave Modes

5.14 I²C Input/Output Timing Specifications

Table 21 lists specifications for the I²C input timing parameters shown in Figure 22.

Table 21. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

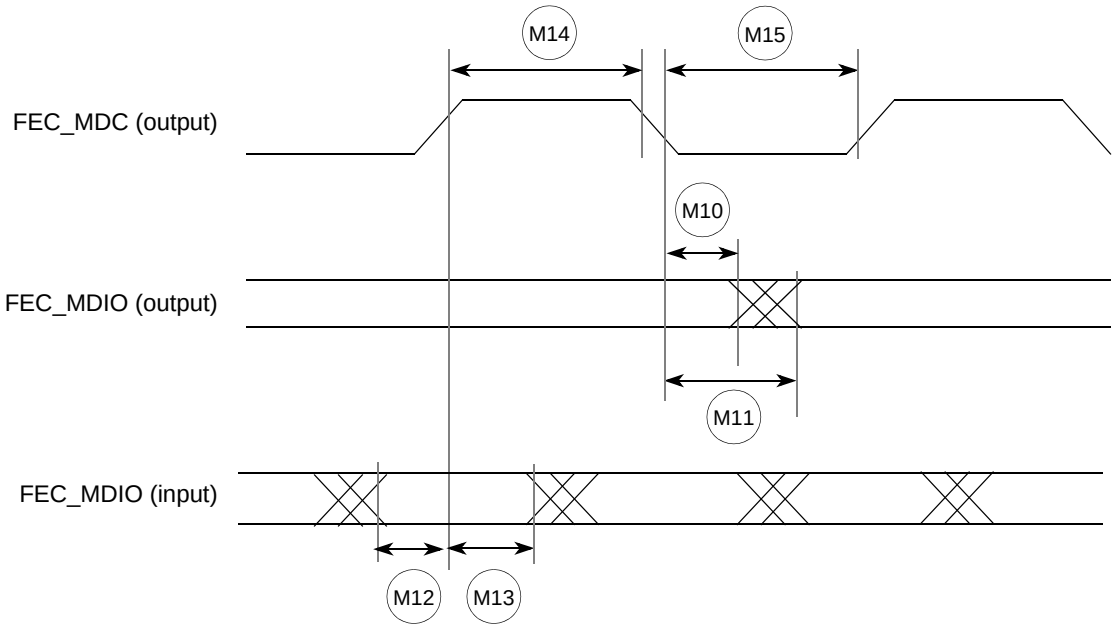


Figure 26. MII Serial Management Channel Timing Diagram

5.16 32-Bit Timer Module Timing Specifications

Table 27 lists timer module AC timings.

Table 27. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.17 QSPI Electrical Specifications

Table 28 lists QSPI timings.

Table 28. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

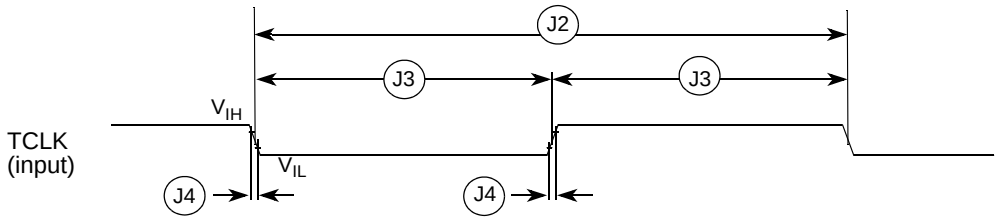


Figure 28. Test Clock Input Timing

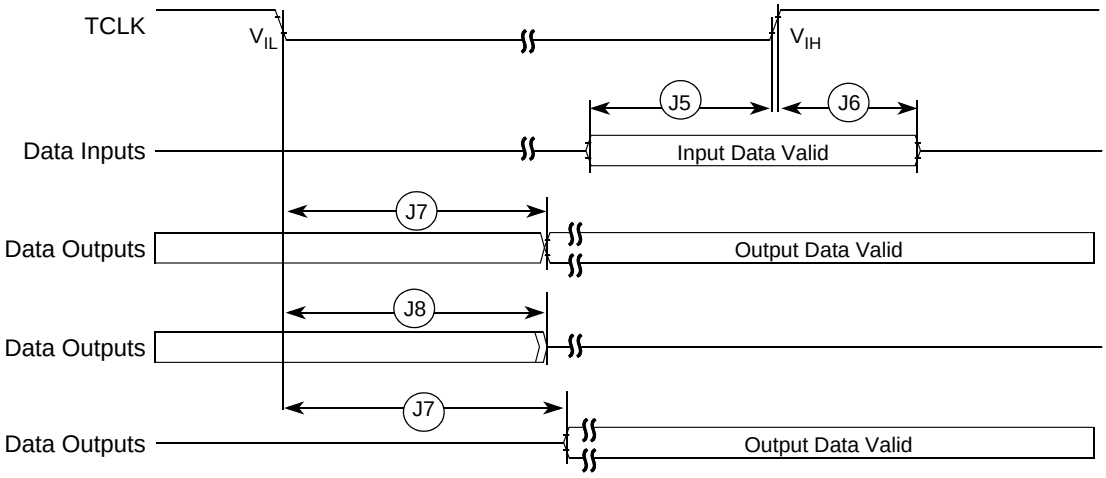


Figure 29. Boundary Scan (JTAG) Timing

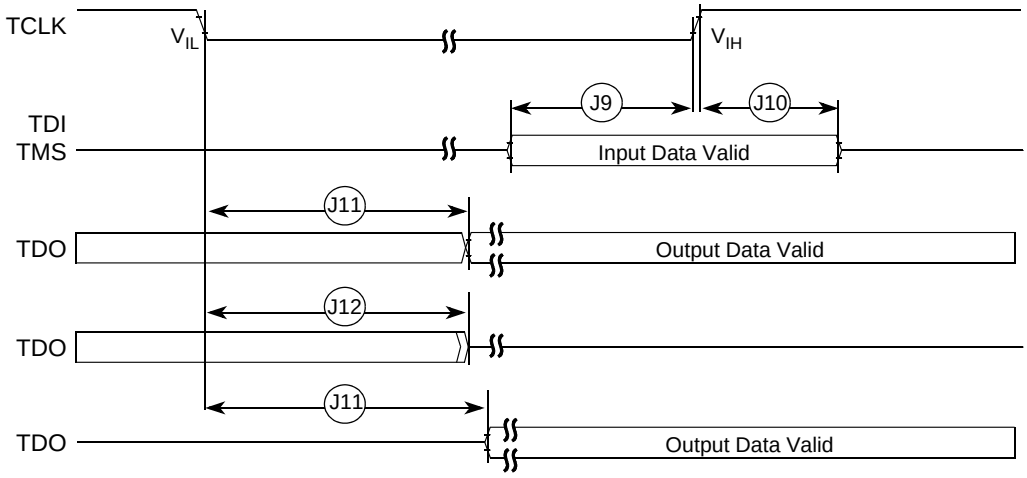


Figure 30. Test Access Port Timing

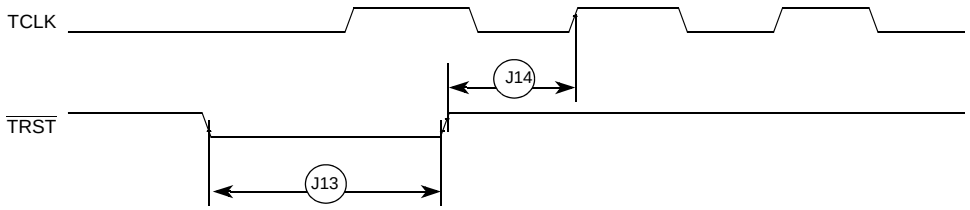


Figure 31. TRST Timing

Table 31. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage	58 MHz (Typ)[3]	64 MHz (Typ)[3]	72 MHz (Typ)[3]	80 MHz (Typ)[3]	80 MHz (Peak)[4]	Units
Stop Mode 3 (Stop 11)[5]	3.3 V	3.9	3.92	4.0	4.0	4.0	mA
	1.5 V	1.04	1.04	1.04	1.04	1.08	
Stop Mode 2 (Stop 10)[4]	3.3 V	4.69	4.72	4.8	4.8	4.8	
	1.5 V	2.69	2.69	2.70	2.70	2.75	
Stop Mode 1(Stop 01)[4]	3.3 V	4.72	4.73	4.81	4.81	4.81	
	1.5 V	15.28	16.44	17.85	19.91	20.42	
Stop Mode 0 (Stop 00)[4]	3.3 V	21.65	21.68	24.33	26.13	26.16	
	1.5 V	15.47	16.63	18.06	20.12	20.67	
Wait/Doze	3.3 V	22.49	22.52	25.21	27.03	39.8	
	1.5 V	26.79	28.85	30.81	34.47	97.4	
Run	3.3 V	33.61	33.61	42.3	50.5	62.6	
	1.5 V	56.3	60.7	65.4	73.4	132.3	

1 All values are measured with a 3.30V EV_{DD}, 3.30V SDV_{DD} and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.

2 Refer to the Power Management chapter in the *MCF532x Reference Manual* for more information on low-power modes.

3 All peripheral clocks except UART0, FlexBus, INTC0, reset controller, PLL, and edge port off before entering low power mode. All code executed from flash.

4 All peripheral clocks on before entering low power mode. All code is executed from flash.

5 See the description of the low-power control register (LCPR) in the *MCF532x Reference Manual* for more information on stop modes 0–3.

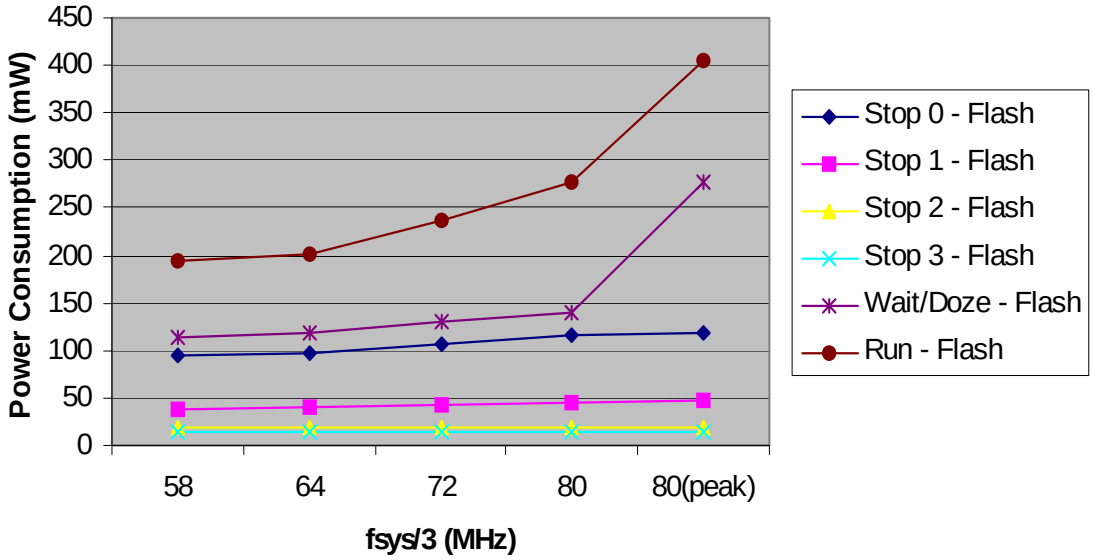


Figure 34. Current Consumption in Low-Power Modes

7 Package Information

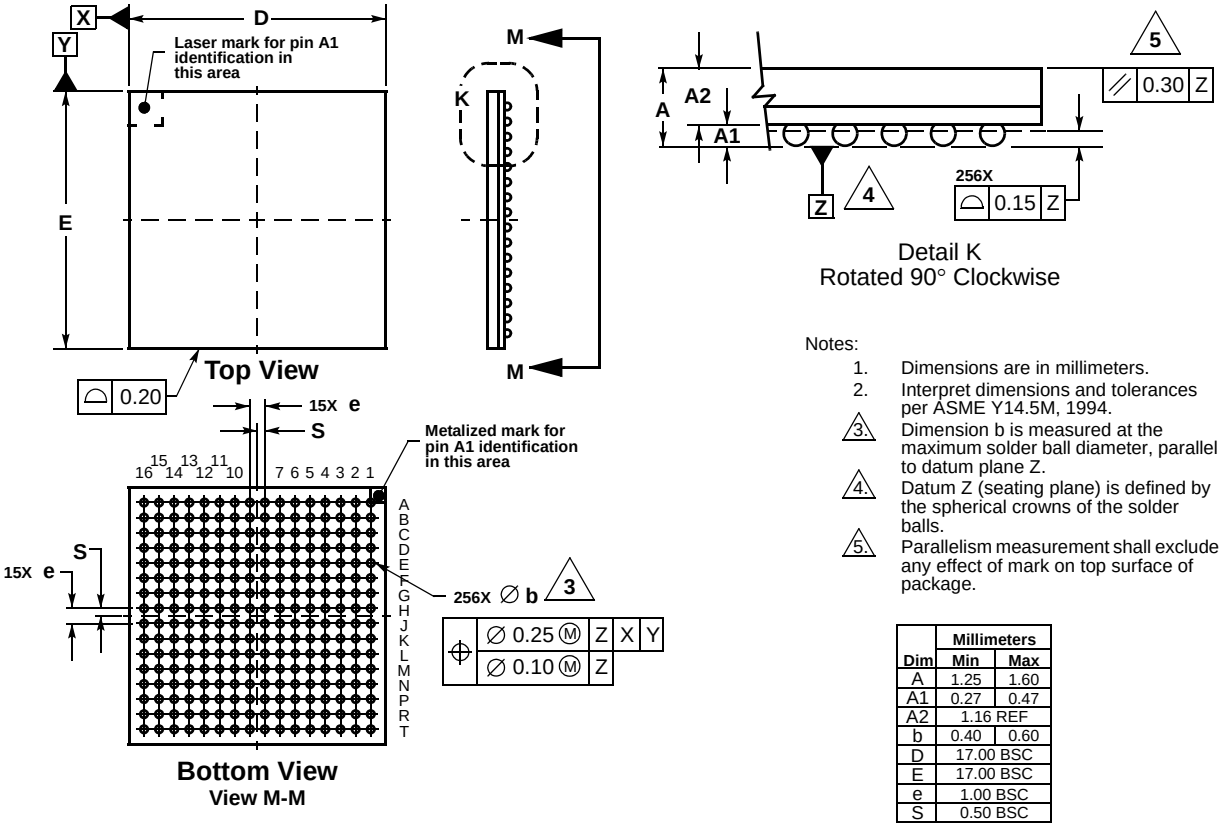
This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF532*x* devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

7.1 Package Dimensions—256 MAPBGA

Figure 36 shows MCF5328CVM240, MCF53281CVM240, and MCF5329CVM240 package dimensions.



Dim	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 36. 256 MAPBGA Package Outline

7.2 Package Dimensions—196 MAPBGA

Figure 37 shows the MCF5327CVM240 package dimensions.

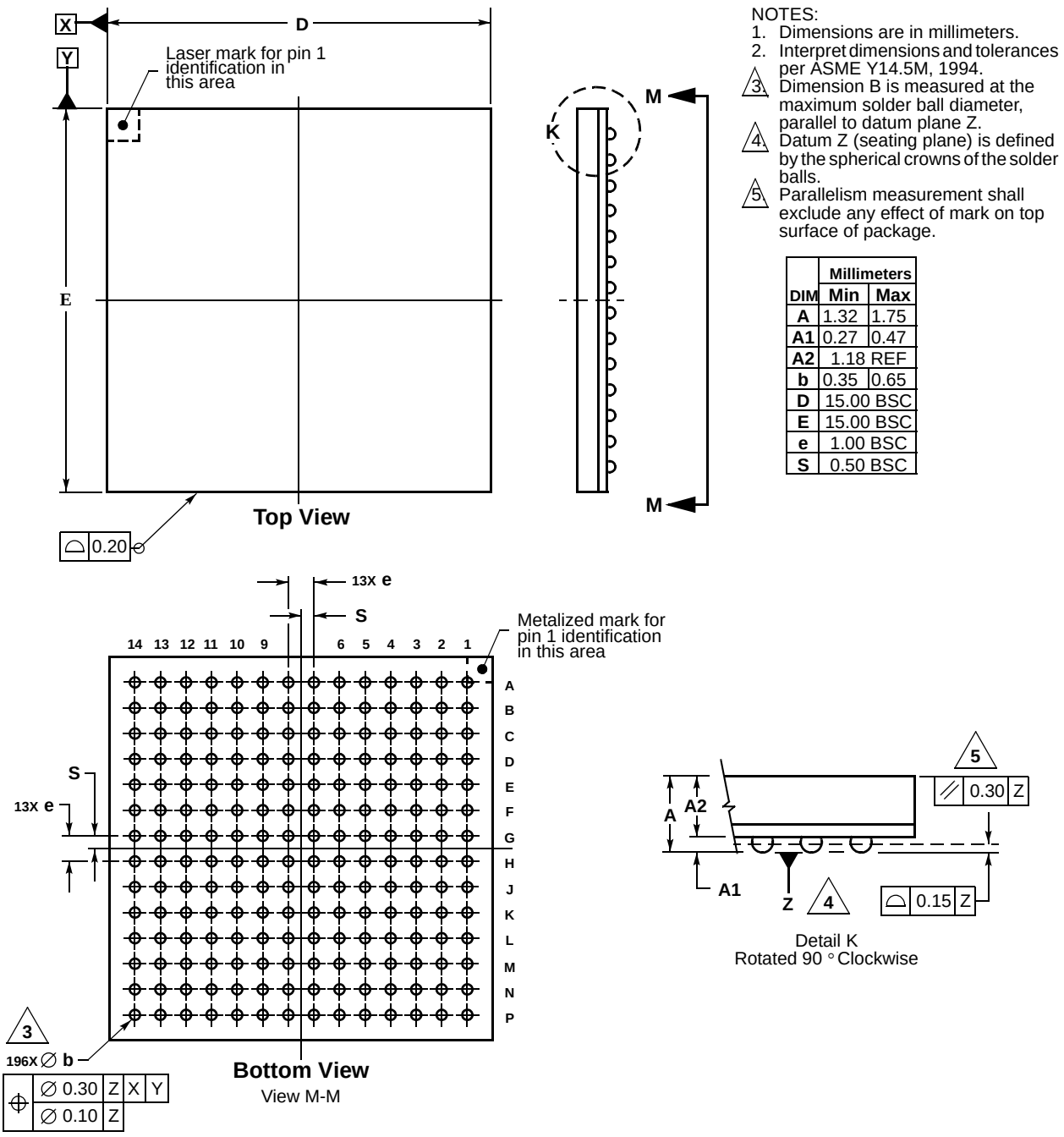


Figure 37. 196 MAPBGA Package Dimensions (Case No. 1128A-01)