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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	227MHz, 1GHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.15V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SNVS, System JTAG, TVDECODE
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6x1evo10ac

Table 2. i.MX 6SoloX Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
MLB	MediaLB	Connectivity/ Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (MOST25, MOST 50).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller supports 16/32-bit LPDDR2-800, DDR3-800 and DDR3L-800.
MU	Messaging Unit	Interprocessor Communication & Synchronization	The MU module supports interprocessor communication between the Cortex-A9 and Cortex-M4 cores.
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable (eFUSE) polyfuses. The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module.
OCRAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
OCRAM_S 16KB	Secure/nonsecure RAM	Secured Internal Memory	Secure/nonsecure internal RAM, interfaced through the CAAM. OCRAM_S can be used by software for state retention of the CPU and other hardware blocks.
OSC32KHz	OSC32KHz	Clocking	Generates 32.768 KHz clock from external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4 PWM-5 PWM-6 PWM-7 PWM-8	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximum Supply Currents

The data shown in Table 13 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

Table 13. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	996 MHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	996 MHz ARM clock	1260	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	400[2]	µA
USB_OTG1_VBUS/USB_OTG2_VBUS (LDO_USB)	—	50[3]	mA
VDDA_ADC_3P3	—	1.5	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(See Note[4])	—
NVCC_DRAM_2P5	—	Use Maximum IO equation [5]	—
NVCC_ENET	N=10	Use Maximum IO equation [5]	—
NVCC_LCD1	N=29	Use Maximum IO equation [5]	—
NVCC_GPIO	N=14	Use Maximum IO equation [5]	—
NVCC_CSI	N=12	Use Maximum IO equation [5]	—
NVCC_QSPI	N=16	Use Maximum IO equation [5]	—
NVCC_JTAG	N=6	Use Maximum IO equation [5]	—

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

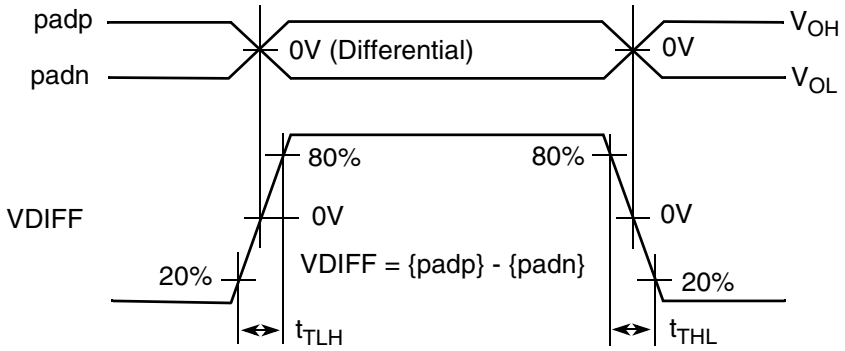

Figure 6. Differential LVDS Driver Transition Time Waveform

Table 34 shows the AC parameters for LVDS I/O.

Table 34. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SoloX processors for the following I/O types:

- Dual Voltage General Purpose I/O (DVGPIO)
- Single Voltage General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

Table 39 shows DDR I/O output buffer impedance of i.MX 6SoloX processors.

Table 39. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.4 USB HSIC I/O Output Buffer Impedance

Table 40 shows the USB HSIC I/O (USB_H_DATA and USB_H_STROBE) output buffer impedance.

Table 40. USB HSIC I/O Output Buffer Impedance

Parameter	Symbol	Drive Strength (DSE)	Typical				Unit
			NVCC_USB_H=1.2V DDR_SEL=10	NVCC_USB_H=1.5V DDR_SEL=11	NVCC_USB_H=1.8V DDR_SEL=11	NVCC_USB_H=2.5V DDR_SEL=11	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Hi-Z 247 113 73 55 43 36 30	Hi-Z 287 121 76 57 45 37 31	Ω

4.8.5 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloX processor.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 44 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

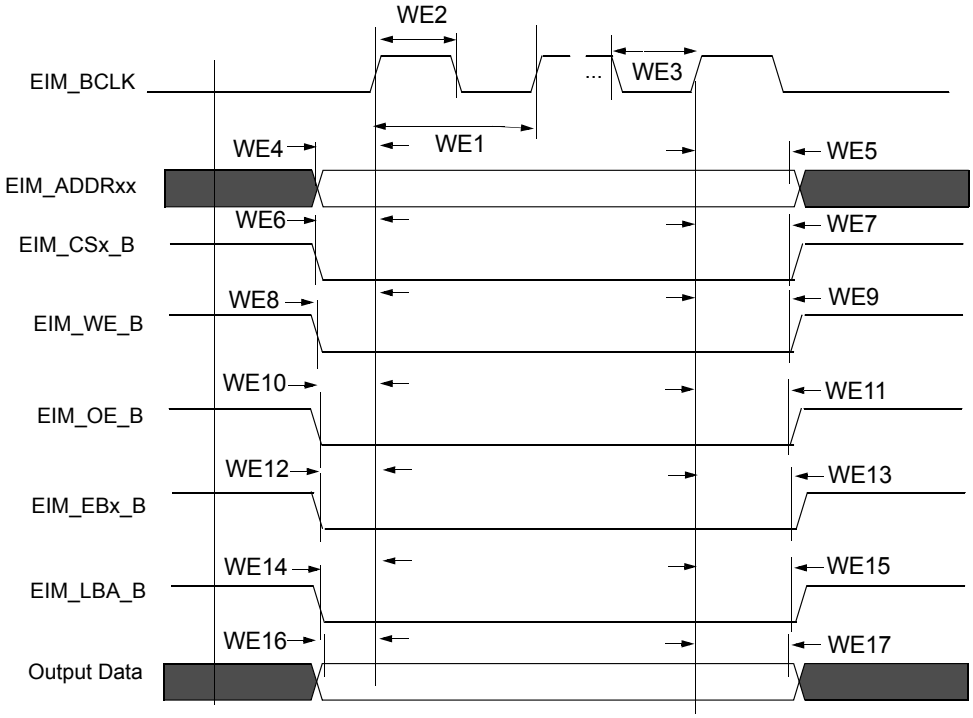

Figure 10. EIM Outputs Timing Diagram

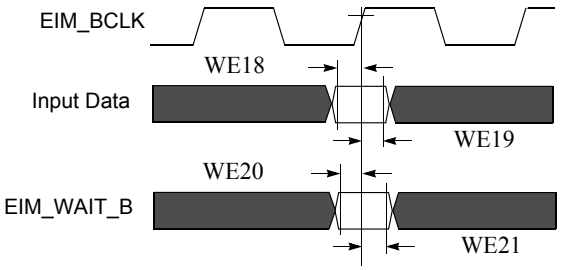

Figure 11. EIM Inputs Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 44. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2 x t	—	3 x t	—	4 x t	—
WE2	EIM_BCLK Low Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE3	EIM_BCLK High Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

Table 64. RGMII Signal Switching Specifications [1] (continued)

Symbol	Description	Min	Max	Unit
T_{skewR}[4]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[5]	Duty cycle for Gigabit	45	55	%
Duty_T[6]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 For all signals, the maximum load is as follows:
CL = 5 pF at 1.8 V
CL = 10 pF at 2.5 V
See Figure 4 for the test circuit.

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

5 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

6 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

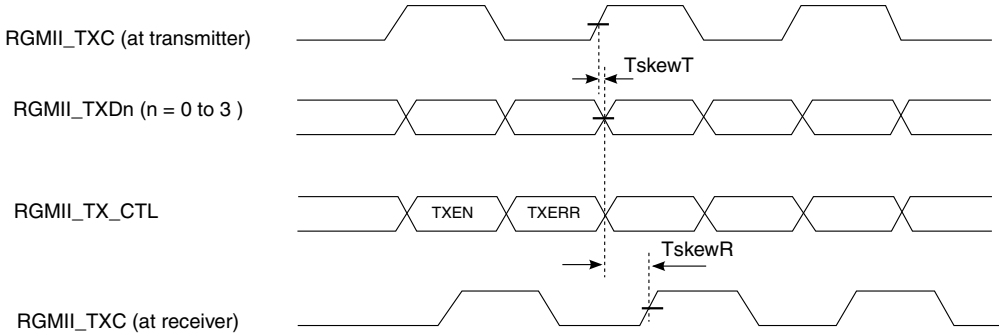

Figure 49. RGMII Transmit Signal Timing Diagram Original

4.12.9 LCD Controller (LCDIF) Timing Parameters

Figure 53 shows the LCDIF timing and Table 66 lists the timing parameters.

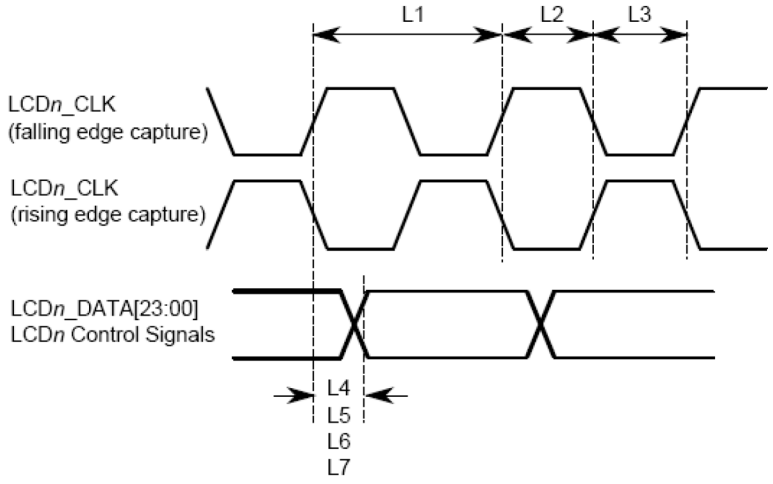

Figure 53. LCD Timing

Table 66. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	-	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	-	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	-	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signals valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signals valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.12.9.1 LCDIF Display Interface Signal Mapping

Table 67. LCDIF Display Interface Signal Mapping

Pin Name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	X	X	X	X	CCIR_CLK
LCD_CS	X	X	X	X	X
LCD_WR_RWn	X	X	X	X	X
LCD_RD_E	X	X	X	X	X
LCD_VSYNC* (two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	X
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	X

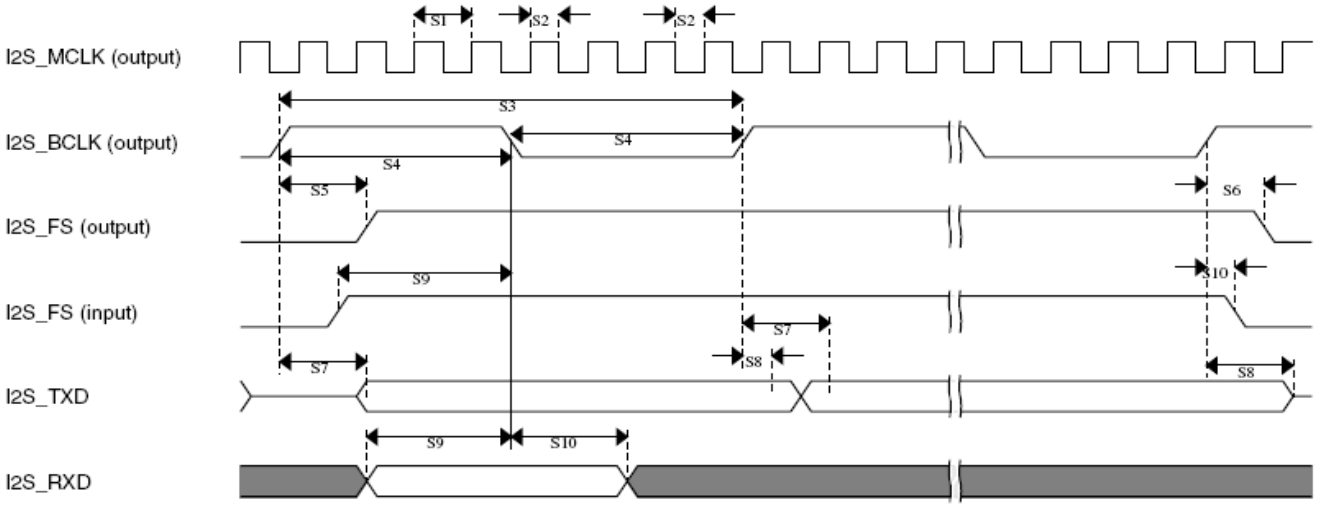

Figure 61. SAI Timing—Master Modes

Table 76. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	2 x S1	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

Table 81. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDxRXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDxRXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDxRXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.18.1.1 UART Transmitter

Figure 73 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 85 lists the UART RS-232 serial mode transmit timing characteristics.

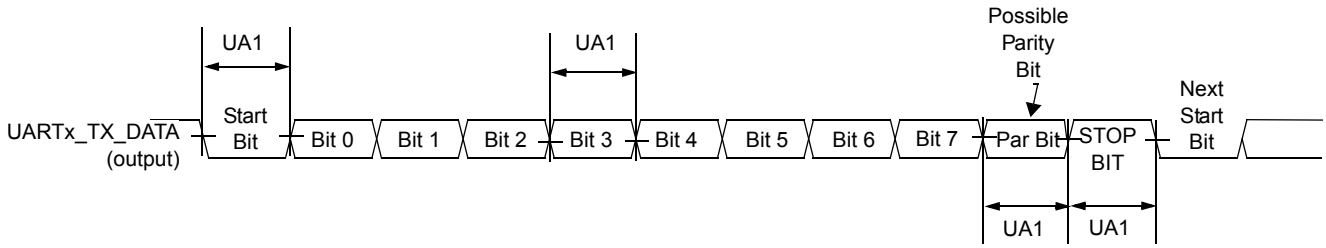

Figure 73. UART RS-232 Serial Mode Transmit Timing Diagram

Table 85. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.18.1.2 UART Receiver

Figure 74 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 86 lists serial mode receive timing characteristics.

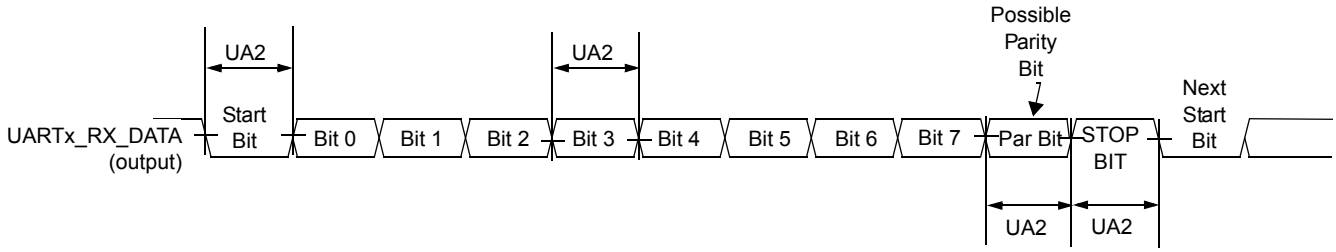

Figure 74. UART RS-232 Serial Mode Receive Timing Diagram

Table 86. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - 1/(16 x F_{baud_rate})	$1/F_{baud\_rate}$ + 1/(16 x F_{baud_rate})	—

1 The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	State during reset (POR_B asserted)	State after reset (POR_B deasserted)	Details
LCD1_DATA00	Input	BT_CFG1[0]	100K Pull Down	Keeper	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL='0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD1_DATA01	Input	BT_CFG1[1]	100K Pull Down	Keeper	
LCD1_DATA02	Input	BT_CFG1[2]	100K Pull Down	Keeper	
LCD1_DATA03	Input	BT_CFG1[3]	100K Pull Down	Keeper	
LCD1_DATA04	Input	BT_CFG1[4]	100K Pull Down	Keeper	
LCD1_DATA05	Input	BT_CFG1[5]	100K Pull Down	Keeper	
LCD1_DATA06	Input	BT_CFG1[6]	100K Pull Down	Keeper	
LCD1_DATA07	Input	BT_CFG1[7]	100K Pull Down	Keeper	
LCD1_DATA08	Input	BT_CFG2[0]	100K Pull Down	Keeper	
LCD1_DATA09	Input	BT_CFG2[1]	100K Pull Down	Keeper	
LCD1_DATA10	Input	BT_CFG2[2]	100K Pull Down	Keeper	
LCD1_DATA11	Input	BT_CFG2[3]	100K Pull Down	Keeper	
LCD1_DATA12	Input	BT_CFG2[4]	100K Pull Down	Keeper	
LCD1_DATA13	Input	BT_CFG2[5]	100K Pull Down	Keeper	
LCD1_DATA14	Input	BT_CFG2[6]	100K Pull Down	Keeper	
LCD1_DATA15	Input	BT_CFG2[7]	100K Pull Down	Keeper	
LCD1_DATA16	Input	BT_CFG4[0]	100K Pull Down	Keeper	
LCD1_DATA17	Input	BT_CFG4[1]	100K Pull Down	Keeper	
LCD1_DATA18	Input	BT_CFG4[2]	100K Pull Down	Keeper	
LCD1_DATA19	Input	BT_CFG4[3]	100K Pull Down	Keeper	
LCD1_DATA20	Input	BT_CFG4[4]	100K Pull Down	Keeper	
LCD1_DATA21	Input	BT_CFG4[5]	100K Pull Down	Keeper	
LCD1_DATA22	Input	BT_CFG4[6]	100K Pull Down	Keeper	
LCD1_DATA23	Input	BT_CFG4[7]	100K Pull Down	Keeper	

Table 107. i.MX 6SoloX Signal Availability by Package (continued)

Affected Module	Package				SoC Capability Implication
	19x19 mm [VM]	17x17 mm NP (no PCIe) [VO]	17x17 mm WP (with PCIe) [VN]	14x14 mm [VK]	
GPIO	GPIO1_IO[21]	—	—	—	—
	GPIO1_IO[20]	—	—	—	—
	GPIO1_IO[19]	—	—	—	—
	GPIO1_IO[18]	—	—	—	—
	GPIO1_IO[17]	—	—	—	—
	GPIO1_IO[16]	—	—	—	—
	GPIO1_IO[15]	—	—	—	—
	GPIO1_IO[14]	—	—	—	—
	GPIO1_IO[25]	—	—	—	—
	GPIO1_IO[22]	—	—	—	—
	GPIO1_IO[23]	—	—	—	—
	GPIO1_IO[24]	—	—	—	—
	GPIO6_IO[2]	—	—	—	—
	GPIO6_IO[3]	—	—	—	—
	GPIO6_IO[1]	—	—	—	—
	GPIO6_IO[0]	—	—	—	—
	GPIO6_IO[4]	—	—	—	—
	GPIO6_IO[5]	—	—	—	—
GPT	GPT_CAPTURE1	—	—	—	—
	GPT_CAPTURE2	—	—	—	—
	GPT_COMPARE1	—	—	—	—
	GPT_CLK	—	—	—	—
	GPT_COMPARE2	—	—	—	—
	GPT_COMPARE3	—	—	—	—
	GPT_CAPTURE1	—	—	—	—
LVDS I/F	LVDS_CLK_N	—	—	—	—
	LVDS_CLK_P	—	—	—	—
	LVDS_DATA0_N	—	—	—	—
	LVDS_DATA0_P	—	—	—	—
	LVDS_DATA1_N	—	—	—	—
	LVDS_DATA1_P	—	—	—	—
	LVDS_DATA2_N	—	—	—	—
	LVDS_DATA2_P	—	—	—	—
	LVDS_DATA3_N	—	—	—	—
	LVDS_DATA3_P	—	—	—	—
	LVDS_CLK_N	—	—	—	—

Table 110. 19x19 mm Functional Contact Assignments (continued)

Ball Name	19x19 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
LCD1_DATA09	H20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO10	Input	Keeper
LCD1_DATA10	H19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO11	Input	Keeper
LCD1_DATA11	H18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO12	Input	Keeper
LCD1_DATA12	G23	NVCC_LCD1	GPIO	ALT5	GPIO3_IO13	Input	Keeper
LCD1_DATA13	G22	NVCC_LCD1	GPIO	ALT5	GPIO3_IO14	Input	Keeper
LCD1_DATA14	G21	NVCC_LCD1	GPIO	ALT5	GPIO3_IO15	Input	Keeper
LCD1_DATA15	G19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO16	Input	Keeper
LCD1_DATA16	G18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO17	Input	Keeper
LCD1_DATA17	F23	NVCC_LCD1	GPIO	ALT5	GPIO3_IO18	Input	Keeper
LCD1_DATA18	F22	NVCC_LCD1	GPIO	ALT5	GPIO3_IO19	Input	Keeper
LCD1_DATA19	F21	NVCC_LCD1	GPIO	ALT5	GPIO3_IO20	Input	Keeper
LCD1_DATA20	G20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO21	Input	Keeper
LCD1_DATA21	F19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO22	Input	Keeper
LCD1_DATA22	F18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO23	Input	Keeper
LCD1_DATA23	E20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO24	Input	Keeper
LCD1_ENABLE	E21	NVCC_LCD1	GPIO	ALT5	GPIO3_IO25	Input	Keeper
LCD1_HSYNC	D23	NVCC_LCD1	GPIO	ALT5	GPIO3_IO26	Input	Keeper
LCD1_RESET	E22	NVCC_LCD1	GPIO	ALT5	GPIO3_IO27	Input	Keeper
LCD1_VSYNC	E23	NVCC_LCD1	GPIO	ALT5	GPIO3_IO28	Input	Keeper
LVDS_CLK_N	T20	NVCC_LVDS	LVDS	—	LVDS_CLK_N	—	—
LVDS_CLK_P	T21	NVCC_LVDS	LVDS	ALT0	LVDS_CLK_P	Input	—
LVDS_DATA0_N	V22	NVCC_LVDS	LVDS	—	LVDS_DATA0_N	—	—
LVDS_DATA0_P	V23	NVCC_LVDS	LVDS	ALT0	LVDS_DATA0_P	Input	—
LVDS_DATA1_N	V20	NVCC_LVDS	LVDS	—	LVDS_DATA1_N	—	—
LVDS_DATA1_P	V21	NVCC_LVDS	LVDS	ALT0	LVDS_DATA1_P	Input	—
LVDS_DATA2_N	U22	NVCC_LVDS	LVDS	—	LVDS_DATA2_N	—	—
LVDS_DATA2_P	U23	NVCC_LVDS	LVDS	ALT0	LVDS_DATA2_P	Input	—
LVDS_DATA3_N	T22	NVCC_LVDS	LVDS	—	LVDS_DATA3_N	—	—
LVDS_DATA3_P	T23	NVCC_LVDS	LVDS	ALT0	LVDS_DATA3_P	Input	—
NAND_ALE	AB7	NVCC_NAND	GPIO	ALT5	GPIO4_IO00	Input	Keeper
NAND_CE0_B	AB8	NVCC_NAND	GPIO	ALT5	GPIO4_IO01	Input	Keeper
NAND_CE1_B	AC9	NVCC_NAND	GPIO	ALT5	GPIO4_IO02	Input	Keeper
NAND_CLE	AB9	NVCC_NAND	GPIO	ALT5	GPIO4_IO03	Input	Keeper

6.4.3 17x17 mm NP (No PCIe) Supplies Contact Assignments and Functional Contact Assignments

Table 113 shows supplies contact assignments for the 17x17 mm NP (No PCIe) package.

Table 113. 17x17 mm NP (no PCIe) Supplies Contact Assignments

Supply Rail Name	17x17 NP [No PCIe] Ball(s) Position(s)	Remark
ADC_VREFH	V16	ADC high reference voltage
ADC_VREFL	R14	ADC low reference voltage
DRAM_VREF	J3	DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM.
DRAM_ZQPAD	C5	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss.
GPANAIO	T15	Analog output for NXP use only. This output must always be left unconnected.
NGND_KEL0	P13	Connect to Vss
NVCC_DRAM	G6, H6, J6, K6, L6, M6, N6, P6	Supply input for the DDR I/O interface
NVCC_DRAM_2P5	K7	Supply input for the DDR interface
NVCC_ENET	F6	Supply input for the ENET interfaces
NVCC_GPIO	F15	Supply input for the GPIO interface
NVCC_HIGH	R12	3.3 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_JTAG	R11	Supply input for the JTAG interface
NVCC_KEY	G15	Supply input for the Key Pad Port (KPP) interface
NVCC_LCD1	H15	Supply input for the LCD interface
NVCC_LOW	V13	1.8 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_NAND	R6	Supply input for the Raw NAND flash memories interface
NVCC_PLL	U18	Supply input for the PLLs
NVCC_QSPI	F14	Supply input for the QSPI interface
NVCC_RGMII1	F8	Supply input for the RGMII1 interface
NVCC_RGMII2	F9	Supply input for the RGMII2 interface
NVCC_SD2	F13	Supply input for the SD2 interface
NVCC_SD4	V10	Supply input for the SD4 interface
NVCC_USB_H	V5	Supply input for the USB HSIC interface
PCIE_VP_CAP	L18	PCIe LDO output
USB_OTG1_VBUS	T17	VBUS input for USB_OTG1

Table 114. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)

Ball Name	17x17 NP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
DRAM_DATA31	A4	NVCC_DRAM	DDR	—	DRAM_DATA31	Input	100 kΩ pull-up
DRAM_DQM0	N2	NVCC_DRAM	DDR	—	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	G2	NVCC_DRAM	DDR	—	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_DQM2	Y3	NVCC_DRAM	DDR	—	DRAM_DQM2	Output	100 kΩ pull-up
DRAM_DQM3	A3	NVCC_DRAM	DDR	—	DRAM_DQM3	Output	100 kΩ pull-up
DRAM_ODT0	U3	NVCC_DRAM	DDR	—	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_RAS_B	H5	NVCC_DRAM	DDR	—	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	D4	NVCC_DRAM	DDR	—	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	G3	NVCC_DRAM	DDR	—	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	P3	NVCC_DRAM	DDR	—	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K4	NVCC_DRAM	DDR	—	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	P5	NVCC_DRAM	DDR	—	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	E4	NVCC_DRAM	DDR	—	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	L1	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK0_N	—	—
DRAM_SDCLK0_P	K1	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK0_P	Output	Low
DRAM_SDQS0_N	P2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_N	—	—
DRAM_SDQS0_P	P1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS0_P	Input	—
DRAM_SDQS1_N	H2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_N	—	—
DRAM_SDQS1_P	G1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS1_P	Input	—
DRAM_SDQS2_N	W1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_N	—	—
DRAM_SDQS2_P	W2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS2_P	Input	—
DRAM_SDQS3_N	B2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_N	—	—
DRAM_SDQS3_P	B1	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_P	Input	—

Table 117. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

Ball Name	17x17 WP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
RGMII2_RX_CTL	B9	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO16	Input	Keeper
RGMII2_RXC	A9	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO17	Input	Keeper
RGMII2_TD0	A11	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO18	Input	Keeper
RGMII2_TD1	B11	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO19	Input	Keeper
RGMII2_TD2	A12	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO20	Input	Keeper
RGMII2_TD3	B12	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO21	Input	Keeper
RGMII2_TX_CTL	B10	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO22	Input	Keeper
RGMII2_TXC	A10	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO23	Input	Keeper
RTC_XTALI	W19	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	Y19	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD2_CLK	E12	NVCC_SD2	GPIO	ALT5	GPIO6_IO06	Input	Keeper
SD2_CMD	F12	NVCC_SD2	GPIO	ALT5	GPIO6_IO07	Input	Keeper
SD2_DATA0	E13	NVCC_SD2	GPIO	ALT5	GPIO6_IO08	Input	Keeper
SD2_DATA1	E14	NVCC_SD2	GPIO	ALT5	GPIO6_IO09	Input	Keeper
SD2_DATA2	F10	NVCC_SD2	GPIO	ALT5	GPIO6_IO10	Input	Keeper
SD2_DATA3	F11	NVCC_SD2	GPIO	ALT5	GPIO6_IO11	Input	Keeper
SD3_CLK	V11	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-down
SD3_CMD	T13	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-down
SD3_DATA0	U10	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-down
SD3_DATA1	T11	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-down
SD3_DATA2	U14	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-down
SD3_DATA3	V14	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-down
SD3_DATA4	T14	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-down
SD3_DATA5	U13	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-down
SD3_DATA6	V12	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-down

Table 118. 17x17 mm WP (with PCIe), 0.8 mm Pitch, 20x20 Ball Map (continued)

	Y	W	V	U	T	R	P	
1	VSS	DRAM_SDQS2_N	DRAM_DATA16	DRAM_DATA22	DRAM_DATA02	DRAM_DATA00	DRAM_SDQS0_P	1
2	DRAM_DATA21	DRAM_SDQS2_P	DRAM_DATA23	DRAM_DATA19	DRAM_DATA01	DRAM_DATA03	DRAM_SDQS0_N	2
3	DRAM_DQM2	DRAM_DATA20	VSS	DRAM_ODT0	VSS	VSS	DRAM_SDBA1	3
4	DRAM_DATA18	DRAM_DATA17	VSS	DRAM_ADDR01	DRAM_ADDR06	DRAM_ADDR14	DRAM_ADDR12	4
5	USB_H_DATA	USB_H_STROBE	NVCC_USB_H	NAND_DATA03	NAND_DATA05	VSS	DRAM_SDCKE0	5
6	NAND_READY_B	NAND_ALE	NAND_DATA00	VSS	NAND_DATA07	NVCC_NAND	NVCC_DRAM	6
7	NAND_DATA02	NAND_DATA04	NAND_WP_B	NAND_CE0_B	NAND_WE_B	JTAG_MOD	VSS	7
8	NAND_DATA06	NAND_DATA01	VDD_SOC_CAP	NAND_RE_B	NAND_CLE	JTAG_TDO	VSS	8
9	SD4_DATA0	SD4_DATA1	NAND_CE1_B	VSS	JTAG_TRST_B	JTAG_TCK	VSS	9
10	SD4_DATA6	SD4_DATA7	NVCC_SD4	SD3_DATA0	JTAG_TMS	JTAG_TDI	VSS	10
11	SD4_DATA5	SD4_CLK	SD3_CLK	SD3_DATA7	SD3_DATA1	NVCC_JTAG	VSS	11
12	SD4_DATA4	SD4_CMD	SD3_DATA6	VSS	SD4_RESET_B	NVCC_HIGH	VSS	12
13	SD4_DATA2	SD4_DATA3	NVCC_LOW	SD3_DATA5	SD3_CMD	VDDA_ADC_3P3	NGND_KEL0	13
14	ADC1_IN0	ADC1_IN1	SD3_DATA3	SD3_DATA2	SD3_DATA4	SNVS_TAMPER	POR_B	14
15	USB_OTG2_DP	USB_OTG2_DN	VDD_USB_CAP	VSS	USB_OTG2_VBUS	CCM_CLK2	CCM_PMIC_STBY_REQ	15
16	VSS	VSS	VDD_SNVS_CAP	GPANAIO	USB_OTG1_VBUS	CCM_CLK1_P	CCM_CLK1_N	16
17	USB_OTG1_DP	USB_OTG1_DN	VDD_HIGH_CAP	VDD_HIGH_IN	USB_OTG1_CHD_B	VSS	PCIE_VPTX	17
18	VSS	VSS	VDD_HIGH_CAP	VDD_HIGH_IN	VDD_SNVS_IN	PCIE_VPH	PCIE_VP	18
19	RTC_XTALO	RTC_XTALI	XTALI	BOOT_MODE1	VSS	PCIE_TX_N	PCIE_RX_N	19
20	VSS	NVCC_PLL	XTALO	BOOT_MODE0	VSS	PCIE_TX_P	PCIE_RX_P	20
	Y	W	V	U	T	R	P	

6.5 14x14 mm Package Information

6.5.1 14x14 mm, 0.65 mm Pitch, 20x20 Ball Matrix

Figure 87 shows the top, bottom, and side views of the 14×14 mm BGA package.

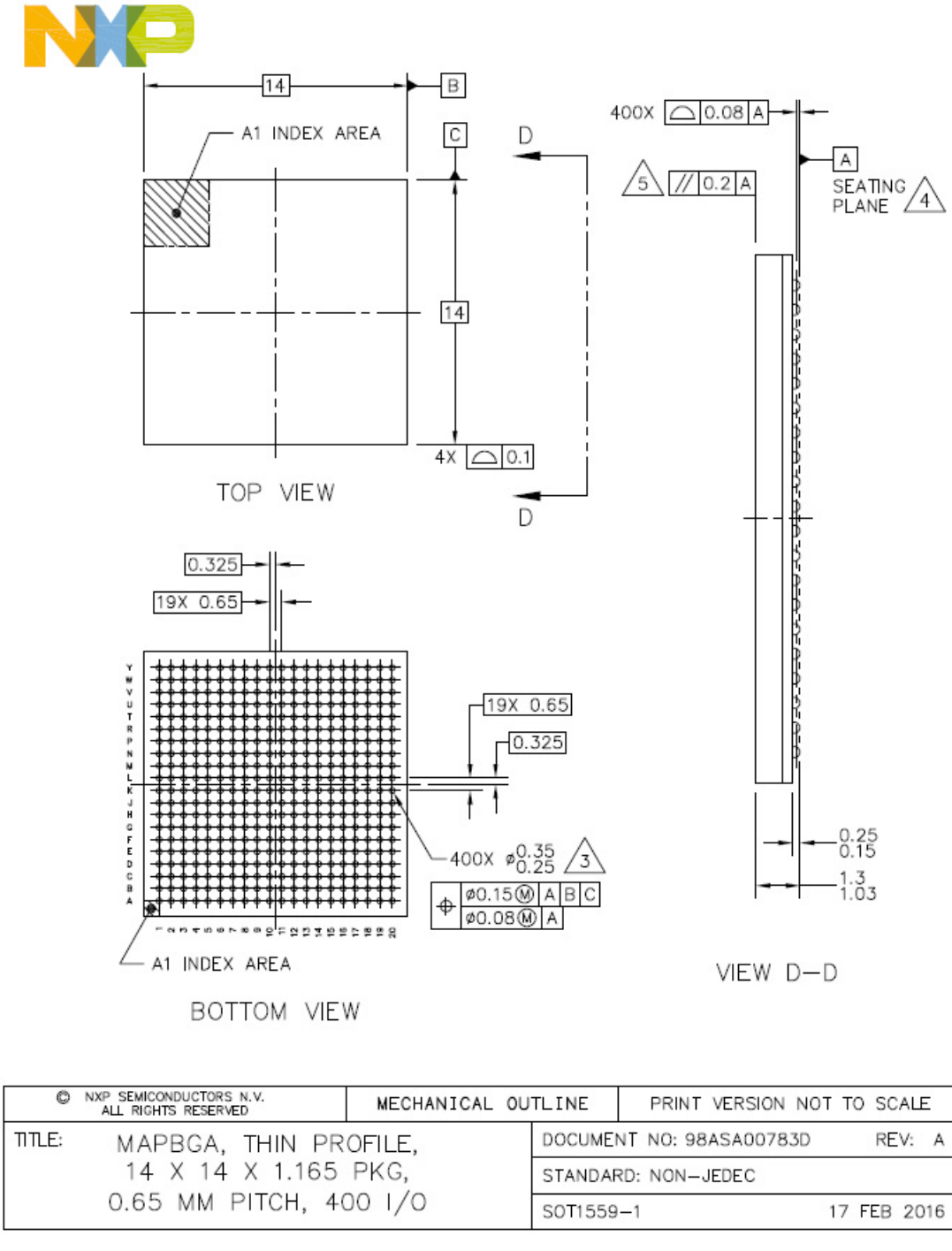

Figure 87. 14x14 mm BGA Package—Top, Bottom, and Side Views

Table 120. 14 x 14 Functional Contact Assignments (continued)

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
LCD1_DATA19	J20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO20	Input	Keeper
LCD1_DATA20	H17	NVCC_LCD1	GPIO	ALT5	GPIO3_IO21	Input	Keeper
LCD1_DATA21	G18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO22	Input	Keeper
LCD1_DATA22	G19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO23	Input	Keeper
LCD1_DATA23	G16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO24	Input	Keeper
LCD1_ENABLE	K20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO25	Input	Keeper
LCD1_HSYNC	J15	NVCC_LCD1	GPIO	ALT5	GPIO3_IO26	Input	Keeper
LCD1_RESET	J18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO27	Input	Keeper
LCD1_VSYNC	J16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO28	Input	Keeper
NAND_ALE	W6	NVCC_NAND	GPIO	ALT5	GPIO4_IO00	Input	Keeper
NAND_CE0_B	U7	NVCC_NAND	GPIO	ALT5	GPIO4_IO01	Input	Keeper
NAND_CE1_B	T8	NVCC_NAND	GPIO	ALT5	GPIO4_IO02	Input	Keeper
NAND_CLE	R7	NVCC_NAND	GPIO	ALT5	GPIO4_IO03	Input	Keeper
NAND_DATA00	V6	NVCC_NAND	GPIO	ALT5	GPIO4_IO04	Input	Keeper
NAND_DATA01	W8	NVCC_NAND	GPIO	ALT5	GPIO4_IO05	Input	Keeper
NAND_DATA02	Y7	NVCC_NAND	GPIO	ALT5	GPIO4_IO06	Input	Keeper
NAND_DATA03	U5	NVCC_NAND	GPIO	ALT5	GPIO4_IO07	Input	Keeper
NAND_DATA04	W7	NVCC_NAND	GPIO	ALT5	GPIO4_IO08	Input	Keeper
NAND_DATA05	T5	NVCC_NAND	GPIO	ALT5	GPIO4_IO09	Input	Keeper
NAND_DATA06	Y8	NVCC_NAND	GPIO	ALT5	GPIO4_IO10	Input	Keeper
NAND_DATA07	T6	NVCC_NAND	GPIO	ALT5	GPIO4_IO11	Input	Keeper
NAND_RE_B	U8	NVCC_NAND	GPIO	ALT5	GPIO4_IO12	Input	Keeper
NAND_READY_B	Y6	NVCC_NAND	GPIO	ALT5	GPIO4_IO13	Input	Keeper
NAND_WE_B	T7	NVCC_NAND	GPIO	ALT5	GPIO4_IO14	Input	Keeper
NAND_WP_B	V7	NVCC_NAND	GPIO	ALT5	GPIO4_IO15	Input	Keeper
ONOFF	U16	VDD_SNVS_IN	GPIO	—	ONOFF	Input	100 kΩ pull-up
POR_B	R16	VDD_SNVS_IN	GPIO	—	POR_B	Input	100 kΩ pull-up
QSPI1A_DATA0	E15	NVCC_QSPI	GPIO	ALT5	GPIO4_IO16	Input	Keeper
QSPI1A_DATA1	C15	NVCC_QSPI	GPIO	ALT5	GPIO4_IO17	Input	Keeper
QSPI1A_DATA2	D14	NVCC_QSPI	GPIO	ALT5	GPIO4_IO18	Input	Keeper
QSPI1A_DATA3	A18	NVCC_QSPI	GPIO	ALT5	GPIO4_IO19	Input	Keeper