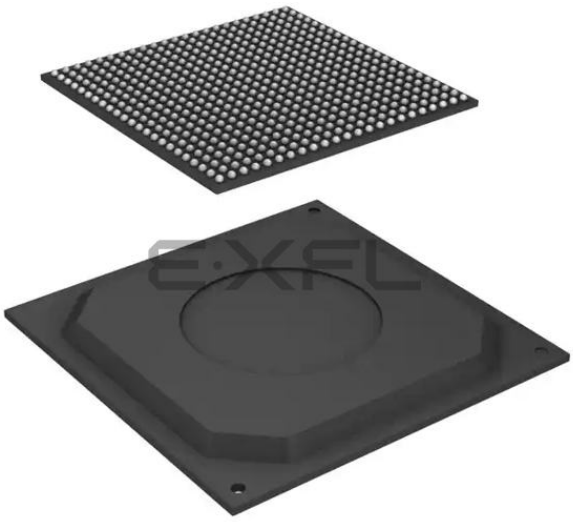

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	227MHz, 1GHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, LVDS
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.15V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SNVS, System JTAG, TVDECODE
Package / Case	529-LFBGA
Supplier Device Package	529-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6x4evm10ac

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 10 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, LVDS Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6XHDG).

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 10 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the DDR IOs, USB Phy, LVDS Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloX Applications Processors (IMX6XHDG).

For additional information, see the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM).

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG1_VBUS and USB_OTG2_VBUS voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either

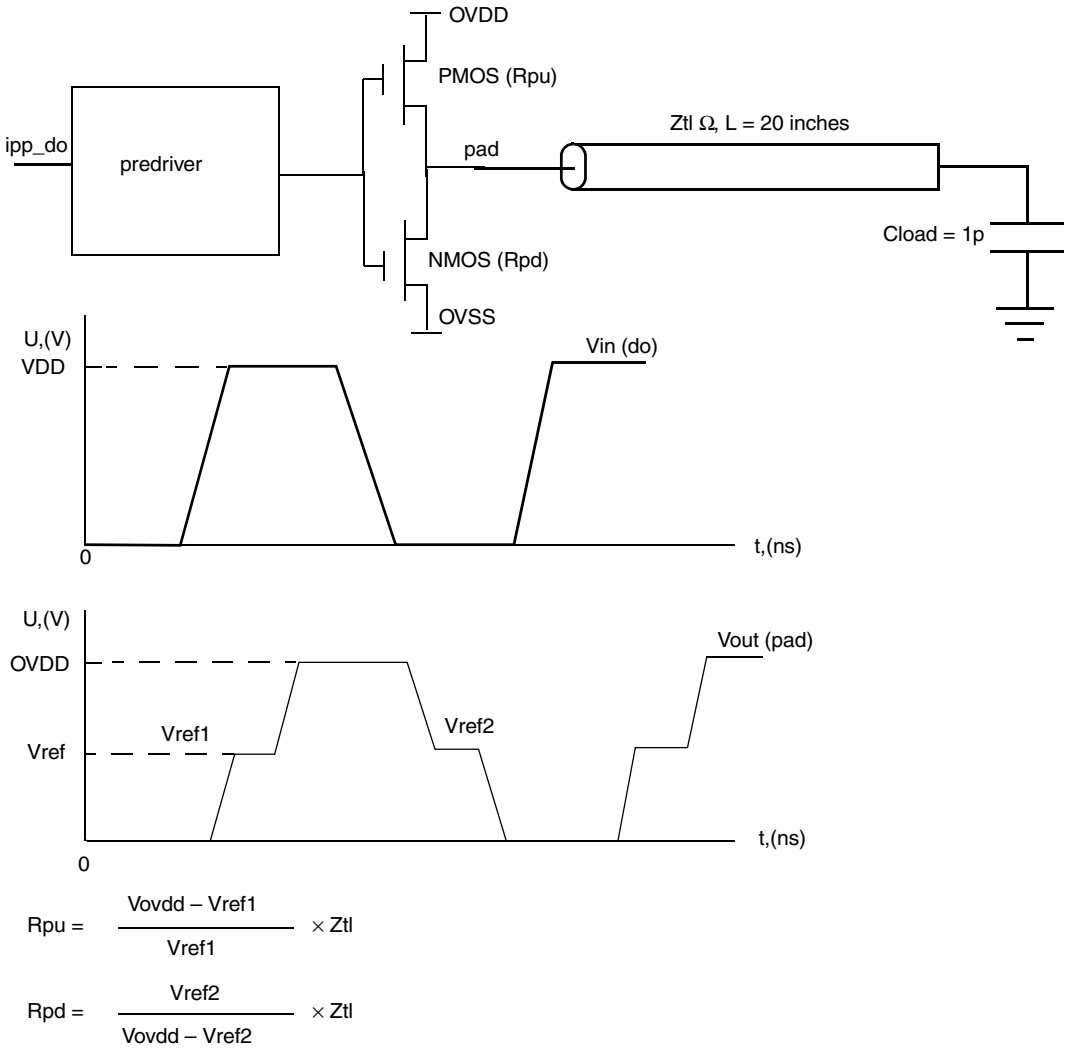

Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typical ADD_DS=1	Typical ADD_DS=0	Unit
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 262 134 88 62 51 43 37	Hi-Z 235 117 78 52 43 36 31	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typical	Unit
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 247 126 84 57 47 40 34	Ω

4.8.2 Single Voltage GPIO Output Buffer Impedance

Table 37 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 37. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 88 65 52 43 37	Ω

Table 38 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 38. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	157 78 53 39 32 26 23	Ω

4.8.3 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.10, “Multi-mode DDR Controller (MMDC).

Table 39 shows DDR I/O output buffer impedance of i.MX 6SoloX processors.

Table 39. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.4 USB HSIC I/O Output Buffer Impedance

Table 40 shows the USB HSIC I/O (USB_H_DATA and USB_H_STROBE) output buffer impedance.

Table 40. USB HSIC I/O Output Buffer Impedance

Parameter	Symbol	Drive Strength (DSE)	Typical				Unit
			NVCC_USB_H=1.2V DDR_SEL=10	NVCC_USB_H=1.5V DDR_SEL=11	NVCC_USB_H=1.8V DDR_SEL=11	NVCC_USB_H=2.5V DDR_SEL=11	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Hi-Z 247 113 73 55 43 36 30	Hi-Z 287 121 76 57 45 37 31	Ω

4.8.5 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloX processor.

- ACLK_EXSC is also used when the EIM is in synchronous mode.
  The maximum frequency for ACLK_EXSC is 132 MHz.

Timing parameters in this section that are given as a function of register settings.

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 43 provides EIM interface pads allocation in different modes.

Table 43. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

[1] For more information on configuration ports mentioned in this table, see the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM).

4.9.3.3 Examples of EIM Synchronous Accesses

Table 44. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2 x t	—	3 x t	—	4 x t	—
WE2	EIM_BCLK Low Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE3	EIM_BCLK High Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

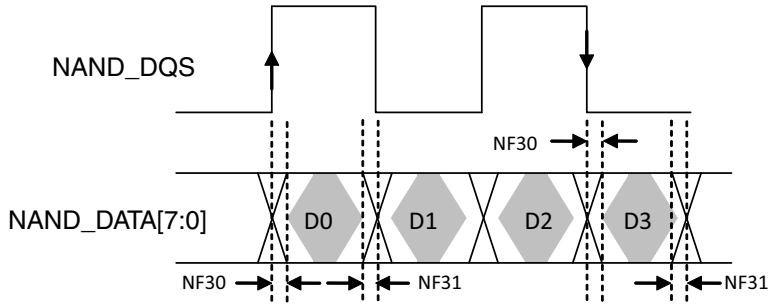

Figure 30. NAND_DQS/NAND_DQ Read Valid Window

Table 48. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		—
NF29	Data write hold	—	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	—

1 GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 30 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM)). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.12.2.0.1 Gated Clock Mode Timing

Figure 33 and Figure 34 shows the gated clock mode timings for CSI, and Table 50 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC (VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

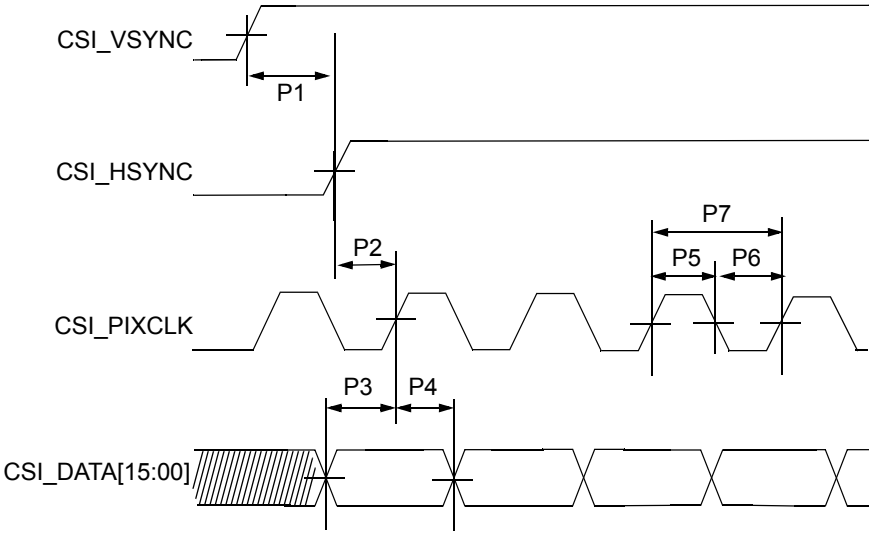

Figure 33. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

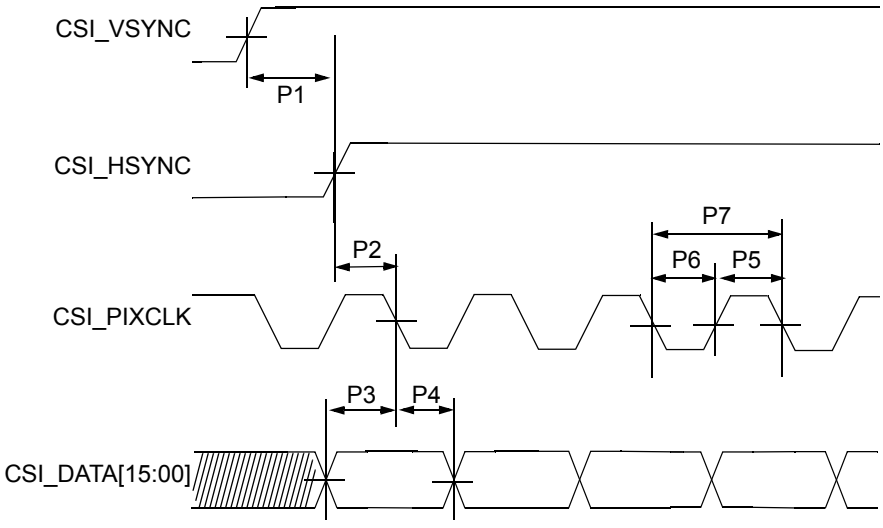

Figure 34. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

4.12.4 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 54 shows the interface timing values. The number field in the table refers to timing signals found in Figure 38 and Figure 39.

Table 54. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

4.12.5.3 SDR50/SDR104 AC Timing

Figure 42 depicts the timing of SDR50/SDR104, and Table 57 lists the SDR50/SDR104 timing characteristics.

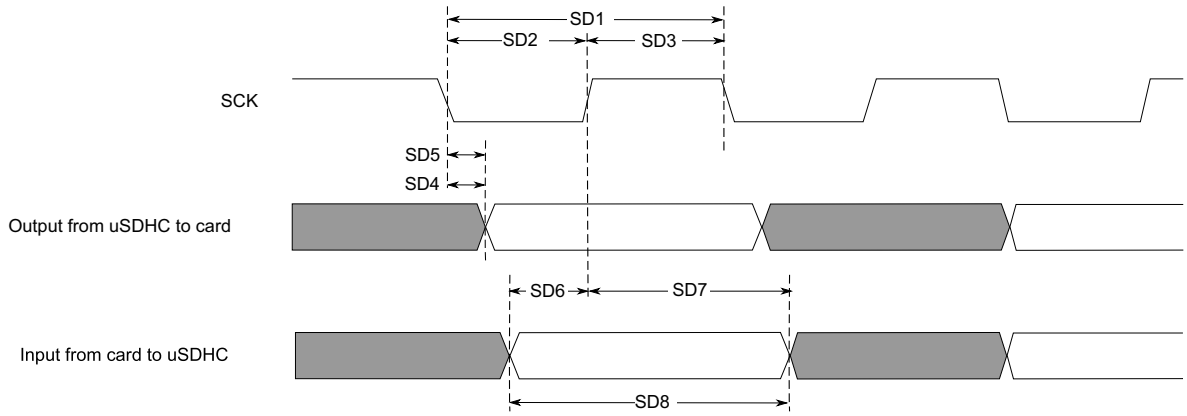

Figure 42. SDR50/SDR104 Timing

Table 57. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times$ tCLK	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times$ tCLK	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times$ tCLK	—	ns

[1] Data window in SDR100 mode is variable.

4.12.5.4 HS200 Mode Timing

Figure 43 depicts the timing of HS200 mode, and Table 58 lists the HS200 timing characteristics.

4.12.17.2 SSI Receiver Timing with Internal Clock

Figure 70 depicts the SSI receiver internal clock timing and Table 82 lists the timing parameters for the receiver timing with the internal clock.

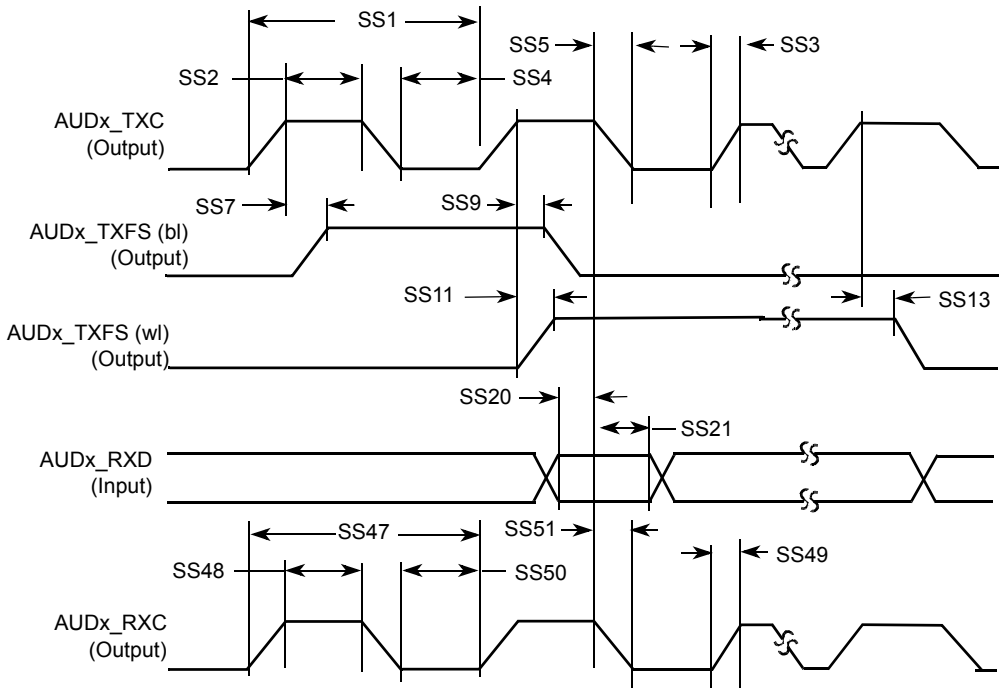

Figure 70. SSI Receiver Internal Clock Timing Diagram

Table 82. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

4.12.18.1.1 UART Transmitter

Figure 73 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 85 lists the UART RS-232 serial mode transmit timing characteristics.

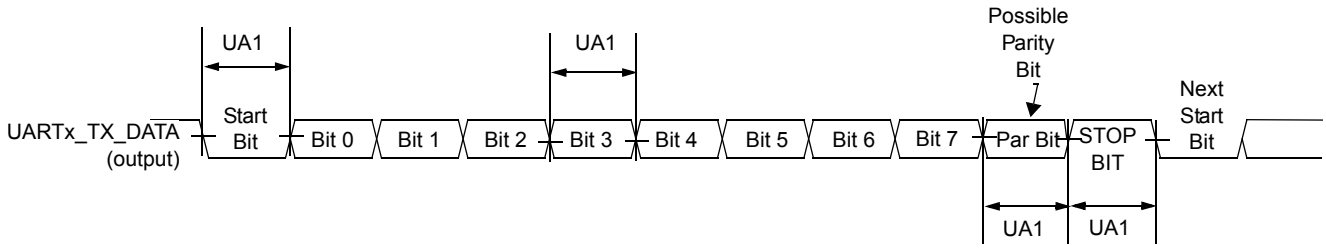

Figure 73. UART RS-232 Serial Mode Transmit Timing Diagram

Table 85. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.18.1.2 UART Receiver

Figure 74 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 86 lists serial mode receive timing characteristics.

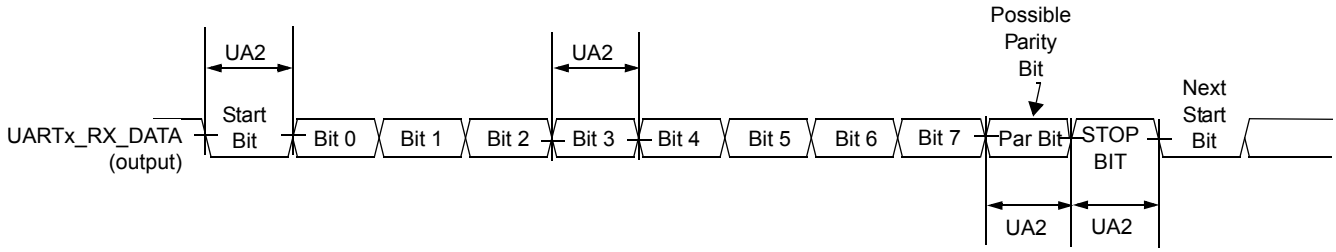

Figure 74. UART RS-232 Serial Mode Receive Timing Diagram

Table 86. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - 1/(16 x F_{baud_rate})	$1/F_{baud\_rate}$ + 1/(16 x F_{baud_rate})	—

1 The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 107. i.MX 6SoloX Signal Availability by Package (continued)

Affected Module	Package				SoC Capability Implication
	19x19 mm [VM]	17x17 mm NP (no PCIe) [VO]	17x17 mm WP (with PCIe) [VN]	14x14 mm [VK]	
MMDC	DRAM_ADDR15	—	—	—	Address space is limited to 2GB on the smaller packages vs.4 GB on the 19x19 package.
PCIe	PCIE_REXT	—	PCIE_REXT	—	—
	PCIE_RX_N	—	PCIE_RX_N	—	—
	PCIE_RX_P	—	PCIE_RX_P	—	—
	PCIE_TX_N	—	PCIE_TX_N	—	—
	PCIE_TX_P	—	PCIE_TX_P	—	—
	PCIE_VP	—	PCIE_VP	—	—
	—	PCIE_VP_CAP	—	PCIE_VP_CAP	—
	PCIE_VPH	—	PCIE_VPH	—	—
	PCIE_VPTX	—	PCIE_VPTX	—	—
UART6	UART6_DCD_B	—	—	—	—
	UART6_DTR_B	—	—	—	—
	UART6_DSR_B	—	—	—	—
	UART6_RI_B	—	—	—	—
uSDHC1	SD1_DATA0	—	—	—	Entire interface not available on the smaller packages
	SD1_DATA1	—	—	—	—
	SD1_CMD	—	—	—	—
	SD1_CLK	—	—	—	—
	SD1_DATA2	—	—	—	—
	SD1_DATA3	—	—	—	—

6.2 Signals with Different States During Reset and After Reset

For most of the signals, the state during reset is the same as the state after reset as listed in the "Out of Reset Condition" column of the Functional Contact Assignment tables for the various packages (Table 110, Table 114, Table 117, and Table 120). However, there are a few signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in Table 108.

Table 108. Signals with Different States During Reset and After Reset

Ball Name	State During Reset (POR_B Asserted)	
	Input/Output	Value
GPIO1_IO06	Output	Drive state unknown. This signal should not be used for system functions that will require it to be an input or stable output during reset.
GPIO1_IO09	Output	Drive state unknown. This signal should not be used for system functions that will require it to be an input or stable output during reset.

Table 110 shows an alpha-sorted list of functional contact assignments for the 19x19 mm package.

Table 110. 19x19 mm Functional Contact Assignments

Ball Name	19x19 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
ADC1_IN0	AC15	VDDA_ADC_3P3	—	—	ADC1_IN0	Input	—
ADC1_IN1	AB15	VDDA_ADC_3P3	—	—	ADC1_IN1	Input	—
ADC1_IN2	AC16	VDDA_ADC_3P3	—	—	ADC1_IN2	Input	—
ADC1_IN3	AB16	VDDA_ADC_3P3	—	—	ADC1_IN3	Input	—
ADC2_IN0	AC17	VDDA_ADC_3P3	—	—	ADC2_IN0	Input	—
ADC2_IN1	AB17	VDDA_ADC_3P3	—	—	ADC2_IN1	Input	—
ADC2_IN2	AC18	VDDA_ADC_3P3	—	—	ADC2_IN2	Input	—
ADC2_IN3	AB18	VDDA_ADC_3P3	—	—	ADC2_IN3	Input	—
BOOT_MODE0	W14	VDD_SNVS_IN	GPIO	—	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	W15	VDD_SNVS_IN	GPIO	—	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	AA22	VDD_HIGH_CAP	—	—	CCM_CLK1_N	—	—
CCM_CLK1_P	AA23	VDD_HIGH_CAP	—	—	CCM_CLK1_P	—	—
CCM_CLK2	W18	VDD_HIGH_CAP	—	—	CCM_CLK2	—	—
CCM_PMIC_STBY_REQ	V16	VDD_SNVS_IN	GPIO	—	CCM_PMIC_STBY_REQ	Output	0
CSI_DATA00	P21	NVCC_CSI	GPIO	ALT5	GPIO1_IO14	Input	Keeper
CSI_DATA01	P20	NVCC_CSI	GPIO	ALT5	GPIO1_IO15	Input	Keeper
CSI_DATA02	P19	NVCC_CSI	GPIO	ALT5	GPIO1_IO16	Input	Keeper
CSI_DATA03	N21	NVCC_CSI	GPIO	ALT5	GPIO1_IO17	Input	Keeper
CSI_DATA04	N19	NVCC_CSI	GPIO	ALT5	GPIO1_IO18	Input	Keeper
CSI_DATA05	N20	NVCC_CSI	GPIO	ALT5	GPIO1_IO19	Input	Keeper
CSI_DATA06	M19	NVCC_CSI	GPIO	ALT5	GPIO1_IO20	Input	Keeper
CSI_DATA07	L19	NVCC_CSI	GPIO	ALT5	GPIO1_IO21	Input	Keeper
CSI_HSYNC	L20	NVCC_CSI	GPIO	ALT5	GPIO1_IO22	Input	Keeper
CSI_MCLK	R19	NVCC_CSI	GPIO	ALT5	GPIO1_IO23	Input	Keeper
CSI_PIXCLK	T19	NVCC_CSI	GPIO	ALT5	GPIO1_IO24	Input	Keeper
CSI_VSYNC	U19	NVCC_CSI	GPIO	ALT5	GPIO1_IO25	Input	Keeper
DRAM_ADDR00	N4	NVCC_DRAM	DDR	—	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	Y4	NVCC_DRAM	DDR	—	DRAM_ADDR01	Output	100 kΩ pull-up

Table 111. 19x19 mm, 0.8 mm Pitch, 23x23 Ball Map (continued)

	H	J	K	L	M	N	P
1	DRAM_SDQS1_P	DRAM_DATA08	DRAM_DATA12	DRAM_DATA09	DRAM_SDCLK0_N	DRAM_DATA05	DRAM_DATA04
2	DRAM_SDQS1_N	VSS	DRAM_DATA10	VSS	DRAM_SDCLK0_P	VSS	DRAM_DATA07
3	DRAM_ADDR03	VSS	DRAM_SDWE_B	VSS	DRAM_VREF	VSS	DRAM_ADDR09
4	DRAM_SDBA0	DRAM_CS0_B	DRAM_CAS_B	DRAM_RAS_B	DRAM_SDBA2	DRAM_ADDR00	DRAM_ADDR13
5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
6	VSS	VSS	VSS	VSS	NVCC_DRAM_2P5	VSS	VSS
7	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
9	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
10	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
11	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
12	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
13	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
14	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
15	VSS	VDD_ARM_CAP	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_SOC_IN	VDD_SOC_IN
16	VSS	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_SOC_CAP	VDD_SOC_CAP
17	VSS	VSS	VSS	VSS	VSS	VSS	VSS
18	LCD1_DATA11	LCD1_DATA06	LCD1_DATA04	PCIE_VP	PCIE_VPTX	RSVD	NVCC_CSI
19	LCD1_DATA10	LCD1_DATA05	LCD1_DATA03	CSI_DATA07	CSI_DATA06	CSI_DATA04	CSI_DATA02
20	LCD1_DATA09	VSS	LCD1_DATA02	CSI_HSYNC	VSS	CSI_DATA05	CSI_DATA01
21	LCD1_CLK	VDD_ARM_IN	RSVD	RSVD	PCIE_REXT	CSI_DATA03	CSI_DATA00
22	LCD1_DATA08	LCD1_DATA01	RSVD	RSVD	VSS	PCIE_RX_N	PCIE_TX_N
23	LCD1_DATA07	LCD1_DATA00	RSVD	RSVD	VSS	PCIE_RX_P	PCIE_TX_P
	H	J	K	L	M	N	P

Table 113. 17x17 mm NP (no PCIe) Supplies Contact Assignments (continued)

Supply Rail Name	17x17 NP [No PCIe] Ball(s) Position(s)	Remark
USB_OTG2_VBUS	U17	VBUS input for USB_OTG2
VDD_ARM_CAP	C16, D16, H10, H11, H12, H13, J13, K13, L13	Supply voltage output from internal LDO_ARM. Requires external capacitor(s).
VDD_ARM_IN	H18, J10, J11, J12, K12, L12	Supply voltage input for internal LDO_ARM.
VDD_HIGH_CAP	N17, N18	Supply voltage output from internal LDO_2P5. Requires external capacitor(s).
VDD_HIGH_IN	P17, P18	Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS.
VDD_SNVS_CAP	T18	Supply voltage output from internal LDO_SNVS. Requires external capacitor(s).
VDD_SNVS_IN	R18	Supply voltage input to the SNVS voltage domain
VDD_SOC_CAP	H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V8	Supply voltage output from internal LDO_SOC. Requires external capacitor(s).
VDD_SOC_IN	C7, C8, J9, K9, L9, M9, M10, M11, M12	Supply voltage input to internal LDO_SOC and LDO_PCIE
VDD_USB_CAP	V17	Supply voltage output from internal LDO_USB. Requires external capacitor(s).
VDDA_ADC_3P3	R13	Supply voltage input to the ADC. This supply must be provided even if the ADC is not used.
VSS	A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, P7, P8, P9, P10, P11, P12, R3, R5, R17, R19, R20, T3, U6, U9, U12, U15, U19, U20, V3, V4, V18, W18, Y1, Y18, Y20	Ground

Table 114 shows an alpha-sorted list of functional contact assignments for the 17x17 mm NP (No PCIe) package.

Table 114. 17x17 mm NP (No PCIe) Functional Contact Assignments

Ball Name	17x17 NP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
ADC1_IN0	Y14	VDDA_ADC_3P3	—	—	ADC1_IN0	Input	—
ADC1_IN1	W14	VDDA_ADC_3P3	—	—	ADC1_IN1	Input	—
ADC1_IN2	Y15	VDDA_ADC_3P3	—	—	ADC1_IN2	Input	—

6.4.5 17x17 mm WP (with PCIe) Supplies Contact Assignments and Functional Contact Assignments

Table 116 shows supplies contact assignments for the 17x17 mm WP (with PCIe) package.

Table 116. 17x17 mm WP (with PCIe) Supplies Contact Assignments

Supply Rail Name	17x17 WP [with PCIe] Ball(s) Position(s)	Remark
DRAM_VREF	J3	DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM.
DRAM_ZQPAD	C5	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss.
GPANAIO	U16	Analog output for NXP use only. This output must always be left unconnected.
NGND_KEL0	P13	Connect to Vss
NVCC_DRAM	G6, H6, J6, K6, L6, M6, N6, P6	Supply input for the DDR I/O interface
NVCC_DRAM_2P5	K7	Supply input for the DDR interface
NVCC_ENET	F6	Supply input for the ENET interfaces
NVCC_GPIO	F15	Supply input for the GPIO interface
NVCC_HIGH	R12	3.3 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_JTAG	R11	Supply input for the JTAG interface
NVCC_KEY	G15	Supply input for the Key Pad Port (KPP) interface
NVCC_LCD1	H15	Supply input for the LCD interface
NVCC_LOW	V13	1.8 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_NAND	R6	Supply input for the Raw NAND flash memories interface
NVCC_PLL	W20	Supply input for the PLLs
NVCC_QSPI	F14	Supply input for the QSPI interface
NVCC_RGMII1	F8	Supply input for the RGMII1 interface
NVCC_RGMII2	F9	Supply input for the RGMII2 interface
NVCC_SD2	F13	Supply input for the SD2 interface
NVCC_SD4	V10	Supply input for the SD4 interface
NVCC_USB_H	V5	Supply input for the USB HSIC interface
PCIE_REXT	N18	PCIe impedance calibration resistor. Connect PCIE_REXT to an external 200 ohm 1% resistor to Vss.
PCIE_VP	P18	Supply input for the PCIe PHY
PCIE_VPH	R18	Supply input for the PCIe PHY
PCIE_VPTX	P17	Supply input for the PCIe PHY

Table 116. 17x17 mm WP (with PCIe) Supplies Contact Assignments (continued)

Supply Rail Name	17x17 WP [with PCIe] Ball(s) Position(s)	Remark
USB_OTG1_VBUS	T16	VBUS input for USB_OTG1
USB_OTG2_VBUS	T15	VBUS input for USB_OTG2
VDD_ARM_CAP	C16, D16, H10, H11, H12, H13, J13, K13, L13	Supply voltage output from internal LDO_ARM. Requires external capacitor(s).
VDD_ARM_IN	H18, J10, J11, J12, K12, L12	Supply voltage input for internal LDO_ARM.
VDD_HIGH_CAP	V17, V18	Supply voltage output from internal LDO_2P5. Requires external capacitor(s).
VDD_HIGH_IN	U17, U18	Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS.
VDD_SNVS_CAP	V16	Supply voltage output from internal LDO_SNVS. Requires external capacitor(s).
VDD_SNVS_IN	T18	Supply voltage input to the SNVS voltage domain
VDD_SOC_CAP	H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V8	Supply voltage output from internal LDO_SOC. Requires external capacitor(s).
VDD_SOC_IN	C7, C8, J9, K9, L9, M9, M10, M11, M12	Supply voltage input to internal LDO_SOC and LDO_PCIE
VDD_USB_CAP	V15	Supply voltage output from internal LDO_USB. Requires external capacitor(s).
VDDA_ADC_3P3	R13	Supply voltage input to the ADC. This supply must be provided even if the ADC is not used.
VSS	A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, N19, N20, P7, P8, P9, P10, P11, P12, R3, R5, R17, T3, T19, T20, U6, U9, U12, U15, V3, V4, W16, W18, Y1, Y16, Y18, Y20	Ground

Table 117 shows an alpha-sorted list of functional contact assignments for the 17x17 mm WP (with PCIe) package.

Table 117. 17x17 WP (with PCIe) Functional Contact Assignments

Ball Name	17x17 WP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
ADC1_IN0	Y14	VDDA_ADC_3P3	—	—	ADC1_IN0	Input	—
ADC1_IN1	W14	VDDA_ADC_3P3	—	—	ADC1_IN1	Input	—

Table 119. 14x14 mm Supplies Contact Assignments (continued)

Supply Rail Name	14x14 mm Ball Position(s)	Comments
VDD_ARM_CAP	C16, D16, H10, H11, H12, H13, J13, K13, L13	Supply voltage output from internal LDO_ARM. Requires external capacitor(s).
VDD_ARM_IN	H18, J10, J11, J12, K12, L12	Supply voltage input for internal LDO_ARM.
VDD_HIGH_CAP	N17, N18	Supply voltage output from internal LDO_2P5. Requires external capacitor(s).
VDD_HIGH_IN	P17, P18	Supply voltage input to internal LDO_2P5, LDO_1P1 and LDO_SNVS.
VDD_SNVS_CAP	T18	Supply voltage output from internal LDO_SNVS. Requires external capacitor(s).
VDD_SNVS_IN	R18	Supply voltage input to the SNVS voltage domain
VDD_SOC_CAP	H8, H9, J8, K8, L8, M8, M13, N8, N9, N10, N11, N12, V9	Supply voltage output from internal LDO_SOC. Requires external capacitor(s).
VDD_SOC_IN	D7, D8, J9, K9, L9, M9, M10, M11, M12	Supply voltage input to internal LDO_SOC and LDO_PCIE
VDD_USB_CAP	V17	Supply voltage output from internal LDO_USB. Requires external capacitor(s).
VDDA_ADC_3P3	R13	Supply voltage input to the ADC. This supply must be provided even if the ADC is not used.
VSS	A1, A20, C3, C4, C18, D6, D9, D12, D15, E3, F3, F5, F17, G7, G8, G9, G10, G11, G12, G13, G14, H3, H7, H14, J7, J14, J17, K3, K10, K11, K14, L3, L7, L10, L11, L14, M7, M14, M17, N3, N7, N13, P7, P8, P9, P10, P11, P12, R3, R5, R17, R19, R20, T3, U6, U9, U12, U15, U19, U20, V3, V4, V18, W18, Y1, Y18, Y20	Ground

Table 121. 14 x 14 mm Ball Map (continued)

	N	M	L	K	J	H
1	DRAM_DQM0	DRAM_SDWE_B	DRAM_SDCLK0_N	DRAM_SDCLK0_P	DRAM_RAS_B	DRAM_SDQS1_N
2	DRAM_CAS_B	DRAM_SDBA1	DRAM_ADDR09	DRAM_CS1_B	DRAM_SDBA2	DRAM_ZQPAD
3	VSS	DRAM_ADDR11	VSS	VSS	DRAM_ADDR13	VSS
4	DRAM_ADDR06	DRAM_ADDR02	DRAM_CS0_B	DRAM_VREF	DRAM_ADDR08	DRAM_ADDR10
5	DRAM_ADDR00	DRAM_ADDR12	DRAM_SDCKE0	DRAM_ADDR03	DRAM_SDCKE1	DRAM_ADDR04
6	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
7	VSS	VSS	VSS	NVCC_DRAM_2P5	VSS	VSS
8	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
9	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_CAP
10	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VDD_ARM_IN	VDD_ARM_CAP
11	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VDD_ARM_IN	VDD_ARM_CAP
12	VDD_SOC_CAP	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_CAP
13	VSS	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP
14	ADC1_IN0	VSS	VSS	VSS	VSS	VSS
15	ADC2_IN2	LCD1_DATA05	LCD1_DATA09	LCD1_DATA12	LCD1_HSYNC	NVCC_CSI_LCD1
16	CCM_PMIC_STBY_REQ	LCD1_DATA06	LCD1_DATA11	LCD1_DATA13	LCD1_VSYNC	LCD1_DATA15
17	VDD_HIGH_CAP	VSS	LCD1_DATA01	LCD1_DATA14	VSS	LCD1_DATA20
18	VDD_HIGH_CAP	LCD1_DATA02	PCIE_VP_CAP	LCD1_DATA08	LCD1_RESET	VDD_ARM_IN
19	LCD1_DATA04	LCD1_DATA00	LCD1_CLK	LCD1_DATA10	LCD1_DATA07	KEY_ROW4
20	LCD1_DATA03	LCD1_DATA17	LCD1_DATA18	LCD1_ENABLE	LCD1_DATA19	LCD1_DATA16