



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

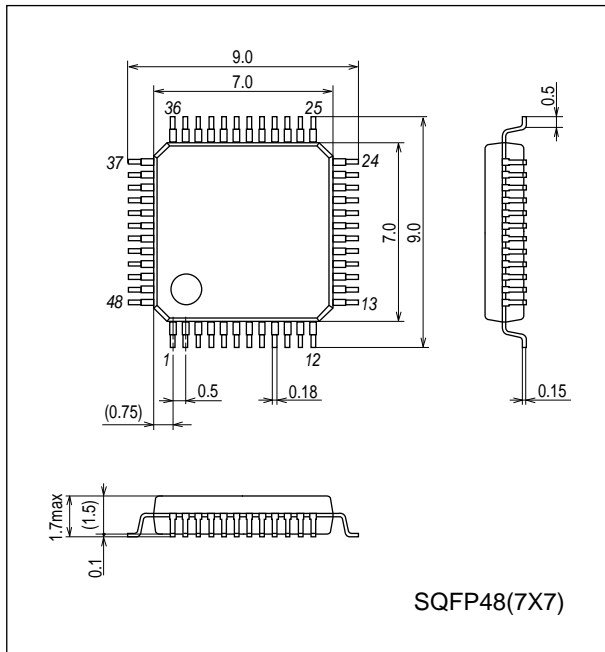
#### Details

Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BQFP
Supplier Device Package	48-QIPE (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/onsemi/lc87f2j32au-qip-e">https://www.e-xfl.com/product-detail/onsemi/lc87f2j32au-qip-e</a>

## Package Dimensions

unit : mm (typ)

3163B



### ■ Minimum Bus Cycle

- 83.3ns (12MHz)  $V_{DD}=2.7$  to 5.5V
- 100ns (10MHz)  $V_{DD}=2.2$  to 5.5V
- 250ns (4MHz)  $V_{DD}=1.8$  to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

### ■ Minimum Instruction Cycle Time

- 250ns (12MHz)  $V_{DD}=2.7$  to 5.5V
- 300ns (10MHz)  $V_{DD}=2.2$  to 5.5V
- 750ns (4MHz)  $V_{DD}=1.8$  to 5.5V

### ■ Ports

- Normal withstand voltage I/O ports  
Ports I/O direction can be designated in 1-bit units
  - Dedicated oscillator ports/input ports
  - Reset pin
  - Power pins
- 39 (P0n, P1n, P2n, P30 to P36, P70 to P73, PWM0, PWM1, XT2, CF2)  
2 (CF1, XT1)  
1 (RES)  
6 ( $V_{SS1}$  to 3,  $V_{DD1}$  to 3)

### ■ Timers

- Timer 0: 16-bit timer/counter with a capture register.  
Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)  $\times$  2 channels  
Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)  
+ 8-bit counter (with an 8-bit capture register)  
Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)  
Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs  
Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs)  
+ 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)  
Mode 1: 8-bit PWM with an 8-bit prescaler  $\times$  2 channels  
Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)  
(toggle outputs also possible from the lower-order 8 bits)  
Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)  
(The lower-order 8 bits can be used as PWM.)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer
  - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  - 2) Interrupts are programmable in 5 different time schemes

### ■High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz)
- 2) Can generate output real-time

### ■SIO

- SIO0: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8-data bits, 1-stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8-data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8-data bits, stop detect)

### ■UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

### ■AD Converter: 12 bits/8 bits × 14 channels

- 12/8 bits AD converter resolution selectable

### ■PWM: Multifrequency 12-bit PWM × 2 channels

### ■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- 1) Noise rejection function  
(Units of noise rejection filter : about 120μs, when selecting a 32.768kHz crystal oscillator as a clock.)
- 2) Supporting reception formats with a guide-pulse of halt-clock/clock/none.
- 3) Determines a end of reception by detecting a no-signal periods (No carrier).  
(Supports same reception format with a different bit length.)
- 4) X'tal HOLD mode release function

### ■Clock Output Function

- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock.

### ■Watchdog timer

- External RC watchdog timer
- Interrupt and reset signals selectable

**■Interrupts**

- 24 sources, 10 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/REMOREC2
4	0001BH	H or L	INT3/INT5/ BT0/BT1
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority levels  $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

- IFLG (List of interrupt source flag function)

- 1) Shows a list of interrupt source flags that caused a branching to a particular vector address (shown in the table above).

**■Subroutine Stack Levels: 512 levels (the stack is allocated in RAM)****■High-speed Multiplication/Division Instructions**

- 16 bits  $\times$  8 bits (5 tCYC execution time)
- 24 bits  $\times$  16 bits (12 tCYC execution time)
- 16 bits  $\div$  8 bits (8 tCYC execution time)
- 24 bits  $\div$  16 bits (12 tCYC execution time)

**■Oscillation Circuits**

- Internal oscillation circuits

- 1) Low-speed RC oscillation circuit : For system clock(100kHz)
- 2) Medium-speed RC oscillation circuit : For system clock(1MHz)
- 3) Frequency variable RC oscillation circuit: For system clock(8MHz)
  - (1) Adjustable in 0.5% (typ) step from a selected center frequency.
  - (2) Measures oscillation clock using a input signal from XT1 as a reference.

- External oscillation circuits

- 1) Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf
- 2) Hi-speed CF oscillation circuit: For system clock, with internal Rf
  - (1) Both the CF and crystal oscillator circuits stop operation on a system reset.

**■System Clock Divider Function**

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2 $\mu$ s, 2.4 $\mu$ s, 4.8 $\mu$ s, 9.6 $\mu$ s, 19.2 $\mu$ s, 38.4 $\mu$ s, and 76.8 $\mu$ s (at a main clock rate of 10MHz).

## ■ Internal Reset Function

- Power-on reset (POR) function
  - 1) POR reset is generated only at power-on time.
  - 2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  - 2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

## ■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) There are three ways of resetting the HALT mode.
    - (1) Setting the reset pin to the low level
    - (2) System resetting by watchdog timer or low-voltage detection
    - (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The CF, RC, and crystal oscillators automatically stop operation.
  - 2) There are four ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the low level.
    - (2) System resetting by watchdog timer or low-voltage detection
    - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4, or INT5
      - \* INT0 and INT1 HOLD mode reset is available only when level detection is set.
    - (4) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The CF and RC oscillators automatically stop operation.
  - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  - 3) There are six ways of resetting the X'tal HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) System resetting by watchdog timer or low-voltage detection
    - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4, or INT5
      - \* INT0 and INT1 HOLD mode reset is available only when level detection is set.
    - (4) Having an interrupt source established at port 0
    - (5) Having an interrupt source established in the base timer circuit
    - (6) Having an interrupt source established in the infrared remote controller receiver circuit

## ■ On-chip Debugger

- Supports software debugging with the IC mounted on the target board (LC87D2J32A).  
LC87F2J32A has an On-chip debugger but its function is limited.

## ■ Data Security Function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.  
Note: This data security function does not necessarily provide absolute data security.

## LC87F2J32A

### ■Development Tools

- On-chip debugger: TCB87- TypeB + LC87D2J32A

### ■Programming Board

Package	Programming boards
SQFP48 (7×7)	W87F55256SQ
QIP48E (14×14)	W87F55256Q

### ■Flash ROM Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single programmer	AF9708 AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 03.07 or later	LC87F2J32A
	Gang programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	
Flash Support Group, Inc. (FSG) + Our company (Note 1)	In-circuit programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	LC87F2J32A
		SIB87(Inter Face Driver) (Our company model)		
Our company	Single/Gang programmer	SKK/SKK Type B (SANYO FWS)	Application Version 1.04 or later	LC87F2J32A
	In-circuit/ Gang programmer	SKK-DBG Type B (SANYO FWS)	Chip Data Version 2.16 or later	

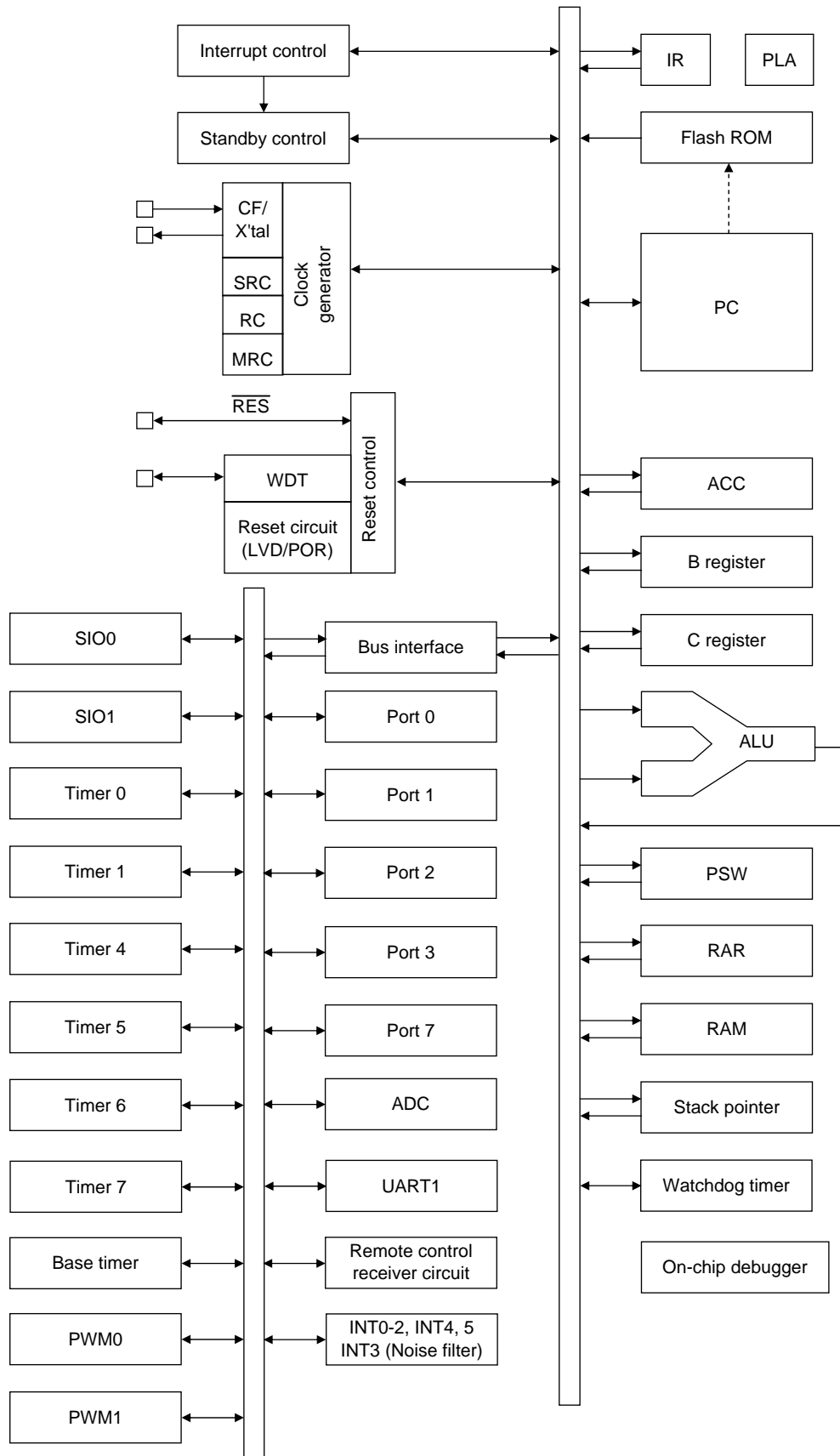
Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together

can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment.

Please ask FSG or Our company for the information.

# System Block Diagram



## Pin Description

Pin Description

Pin Name	I/O	Description	Option																		
V <sub>SS</sub> 1 to V <sub>SS</sub> 3	-	- power supply pins	No																		
V <sub>DD</sub> 1 to V <sub>DD</sub> 3	-	+ power supply pin	No																		
Port 0	I/O	<ul style="list-style-type: none"><li>• 8-bit I/O port</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• HOLD reset input</li><li>• Port 0 interrupt input</li><li>• Pin functions<ul style="list-style-type: none"><li>P05: System clock output</li><li>P06: Timer 6 toggle output</li><li>P07: Timer 7 toggle output</li><li>P00(AN0) to P07(AN7): AD converter input</li></ul></li></ul>	Yes																		
P00 to P07																					
Port 1	I/O	<ul style="list-style-type: none"><li>• 8-bit I/O port</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions<ul style="list-style-type: none"><li>P10: SIO0 data output</li><li>P11: SIO0 data input/bus I/O</li><li>P12: SIO0 clock I/O</li><li>P13: SIO1 data output</li><li>P14: SIO1 data input / bus I/O</li><li>P15: SIO1 clock I/O</li><li>P16: Timer 1PWM output</li><li>P17: Timer 1PWMH output/beeper output</li></ul></li></ul>	Yes																		
P10 to P17																					
Port 2	I/O	<ul style="list-style-type: none"><li>• 8-bit I/O port</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions<ul style="list-style-type: none"><li>P20: UART transmit</li><li>P21: UART receive</li><li>P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/timer 0H capture input</li><li>P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/timer 0H capture input</li></ul></li></ul> <p>Interrupt acknowledge type</p> <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising &amp; Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising & Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	Yes
			Rising	Falling	Rising & Falling	H level	L level														
INT4	enable	enable	enable	disable	disable																
INT5	enable	enable	enable	disable	disable																
P20 to P27																					
Port 3	I/O	<ul style="list-style-type: none"><li>• 7-bit I/O port</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Shared pins<ul style="list-style-type: none"><li>On-chip debugger pins: DBGP0 to DBGP2 (P30 to P32)</li></ul></li></ul>	Yes																		
P30 to P36																					

Continued on next page.



## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.  
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	Programmable (Note 1)
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P36	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No
CF1	-	No	Input for ceramic resonator oscillator (Input only)	No
CF2	-	No	Output for ceramic resonator oscillator (Nch-open drain when in general-purpose output mode)	No

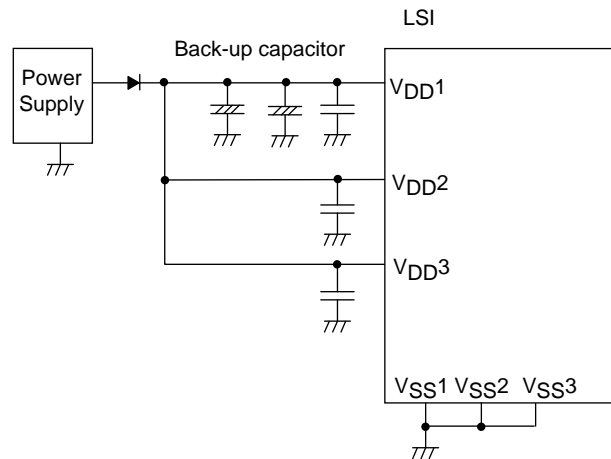
Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low- and high-impedance pull-up connection is exercised in 1-bit units.

User Option Table

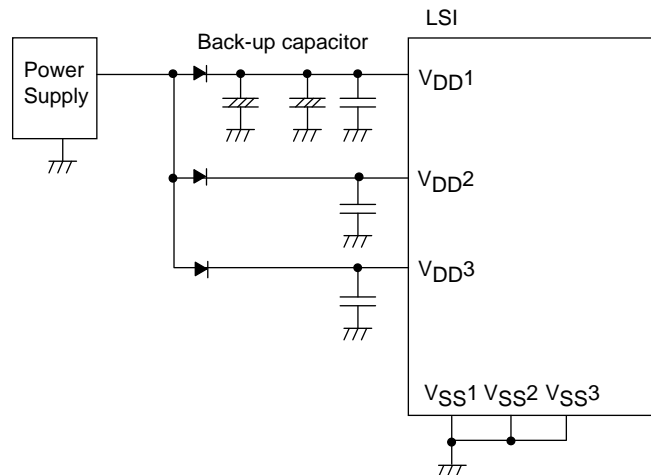
Option name	Option to be applied on	Flash-ROM version	Option selected in units of	Option selection
Port output type	P00 to P07	○	1 bit	CMOS
				Nch-open drain
	P10 to P17	○	1 bit	CMOS
				Nch-open drain
	P20 to P27	○	1 bit	CMOS
				Nch-open drain
	P30 to P36	○	1 bit	CMOS
				Nch-open drain
Program start address	-	○	-	00000h
				07E00h
Low-voltage detection reset function	Detect function	○	-	Enable: Use
	Detect level	○	-	Disable: Not Used
Power-on reset function	Power-On reset level	○	-	7-level
				8-level

Note: To reduce  $V_{DD}$  signal noise and to increase the duration of the backup battery supply,  $V_{SS1}$ ,  $V_{SS2}$ , and  $V_{SS3}$  should connect to each other and they should also be grounded.

Example 1: During backup in hold mode, port output 'H' level is supplied from the back-up capacitor.



Example 2: During backup in hold mode, output is not held high and its value is unsettled.



# LC87F2J32A

## Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

Parameter		Symbol	Pin/Remarks	Conditions	Specification			
					VDD[V]	min	typ	max
Maximum supply voltage		VDD max	VDD1, VDD2, VDD3	VDD1=VDD2=VDD3		-0.3		+6.5
Input voltage		VI	XT1, CF1			-0.3		VDD+0.3
Input/output voltage		VI/O	Ports 0, 1, 2, 3, Port 7, PWM0, PWM1, XT2, CF2			-0.3		VDD+0.3
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-10		
		IOPH(2)	PWM0, PWM1			-20		
		IOPH(3)	P71 to P73	Per 1 applicable pin		-5		
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-7.5		
		IOMH(2)	PWM0, PWM1			-15		
		IOMH(3)	P71 to P73	Per 1 applicable pin		-3		
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-10		
		ΣIOAH(2)	Port 0	Total of all applicable pins		-25		
		ΣIOAH(3)	Port 1, PWM0, PWM1	Total of all applicable pins		-25		
		ΣIOAH(4)	Ports 0, 1, PWM0, PWM1	Total of all applicable pins		-45		
		ΣIOAH(5)	Ports 2, P35, P36	Total of all applicable pins		-25		
		ΣIOAH(6)	P30 to P34	Total of all applicable pins		-25		
		ΣIOAH(7)	Pots 2, 3	Total of all applicable pins		-45		
Low level output current	Peak output current	IOPL(1)	P02 to P07, Ports 1, 2, 3, PWM0, PWM1	Per 1 applicable pin				20
		IOPL(2)	P00, P01	Per 1 applicable pin				30
		IOPL(3)	Port 7, XT2, CF2	Per 1 applicable pin				10
	Mean output current (Note 1-1)	IOML(1)	P02 to P07, Ports 1, 2, 3, PWM0, PWM1	Per 1 applicable pin				15
		IOML(2)	P00, P01	Per 1 applicable pin				20
		IOML(3)	Port 7, XT2, CF2	Per 1 applicable pin				7.5
	Total output current	ΣIOAL(1)	Port 7, XT2, CF2	Total of all applicable pins				15
		ΣIOAL(2)	Port 0	Total of all applicable pins				45
		ΣIOAL(3)	Port 1, PWM0, PWM1	Total of all applicable pins				45
		ΣIOAL(4)	Port 0, 1, PWM0, PWM1	Total of all applicable pins				80
		ΣIOAL(5)	Ports 2, P35, P36	Total of all applicable pins				45
		ΣIOAL(6)	P30 to P34	Total of all applicable pins				45
		ΣIOAL(7)	Ports 2, 3	Total of all applicable pins				60
Power dissipation	Pd max(1)	SQFP48 (7×7)		Ta=-40 to +85°C Package only				139
				Ta=-40 to +85°C Package with thermal resistance board (Note 1-2)				356
	Pd max(3)	QIP48E (14×14)		Ta=-40 to +85°C Package only				281
				Ta=-40 to +85°C Package with thermal resistance board (Note 1-2)				489
Operating ambient temperature	Topr					-40		+85
Storage ambient temperature	Tstg					-55		+125

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6mm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# LC87F2J32A

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmMRC(1)		Frequency variable RC oscillation. 1/2 frequency division ratio. (RCCTD=0) (Note 2-4)	2.4 to 5.5	7.44	8.0	8.56	MHz
	FmMRC(2)		Frequency variable RC oscillation. 1/2 frequency division ratio. (RCCTD=0) Ta=-10 to +50°C (Note 2-4)	2.4 to 5.5	7.6	8.0	8.4	
	FmRC		Internal Medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal Low-speed RC oscillation	1.8 to 5.5	50	100	200	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 3.	1.8 to 5.5		32.768		
Frequency variable RC oscillation usable range	OpVMRC		Frequency variable RC oscillation. 1/2 frequency division ratio. (RCCTD=0)	2.4 to 5.5	6	8	10	MHz
Frequency variable RC oscillation adjustment range	VmADJ(1)		Each step of VMRCHBn	2.4 to 5.5	3.6	7.0	11	%
	VmADJ(2)		Each step of VMFCHBn	2.4 to 5.5	0.7	1.5	2.3	
	VmADJ(3)		Each step of VMDCHn	2.4 to 5.5	0.2	0.5	1.1	

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When switching the system clock, allow an oscillation stabilization time of 100μs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

## LC87F2J32A

**Serial Input/Output Characteristics** at  $T_a = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	$V_{DD}[\text{V}]$	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6	1.8 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SB0(P11), SIO(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	1.8 to 5.5	0.05			
	Data hold time		thDI(1)				0.05			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-2)	1.8 to 5.5			(1/3)tCYC +0.08	$\mu\text{s}$
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-2)				1tCYC +0.08	
	Output clock		tdD0(3)		(Note 4-1-2)				(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	$V_{DD}[\text{V}]$	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 6.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	1.8 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	1.8 to 5.5	0.05			
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	1.8 to 5.5			(1/3)tCYC +0.08	$\mu\text{s}$

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

## LC87F2J32A

### Pulse Input Conditions at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
					min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23) INT5(P24 to P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	1.8 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	256			
	tPIL(5)	$\overline{\text{RES}}$	• Resetting is enabled.	1.8 to 5.5	200			μs

### AD Converter Characteristics at V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

#### <12bits AD Converter Mode at Ta = -40 to +85°C>

Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	Specification			
					min	typ	max	unit
Resolution	N	AN0(P00) to		2.4 to 5.5		12		bit
Absolute accuracy	ET	AN7(P07)	(Note 6-1)	3.0 to 5.5			±16	LSB
		AN8(P70)	(Note 6-1)	2.4 to 3.6			±20	
Conversion time	TCAD	AN9(P71)	• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	μs
		AN10(XT1)		3.0 to 5.5	64		115	
		AN11(XT2)	• See Conversion time calculation formulas. (Note 6-2)	2.4 to 3.6	410		425	
Analog input voltage range	VAIN	AN12(CF1) AN13(CF2)		2.4 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	V
Analog port input current	I <sub>AINH</sub> (1)	analog channel except AN12	V <sub>AIN</sub> =V <sub>DD</sub>	2.4 to 5.5			1	μA
	I <sub>AINL</sub> (1)		V <sub>AIN</sub> =V <sub>SS</sub>	2.4 to 5.5	-1			
	I <sub>AINH</sub> (2)	AN12	V <sub>AIN</sub> =V <sub>DD</sub>	2.4 to 5.5			15	
	I <sub>AINL</sub> (2)		V <sub>AIN</sub> =V <sub>SS</sub>	2.4 to 5.5	-15			

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

## LC87F2J32A

### <8bits AD Converter Mode at Ta = -40 to +85°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Resolution	N	AN0(P00) to		2.4 to 5.5		8		bit
Absolute accuracy	ET	AN7(P07) AN8(P70)	(Note 6-1)	2.4 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71)	• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	μs
		AN10(XT1) AN11(XT2)		3.0 to 5.5	40		90	
		AN12(CF1) AN13(CF2)	• See Conversion time calculation formulas. (Note 6-2)	2.4 to 3.6	250		265	
Analog input voltage range	VAIN			2.4 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	V
Analog port input current	IAINH(1)	analog channel except AN12	VAIN=V <sub>DD</sub>	2.4 to 5.5			1	μA
	IAINL(1)		VAIN=V <sub>SS</sub>	2.4 to 5.5	-1			
	IAINH(2)	AN12	VAIN=V <sub>DD</sub>	2.4 to 5.5			15	
	IAINL(2)		VAIN=V <sub>SS</sub>	2.4 to 5.5	-15			

Conversion time calculation formulas:

12bits AD Converter Mode: TCAD(Conversion time)= ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time)= ((32/(AD division ratio))+2)×(1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (V <sub>DD</sub> )	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-12MHz	4.0V to 5.5V	1/1	250ns	1/8	34.8μs	21.5μs
	3.0V to 5.5V	1/1	250ns	1/16	69.5μs	42.8μs
CF-10MHz	4.0V to 5.5V	1/1	300ns	1/8	41.8μs	25.8μs
	3.0V to 5.5V	1/1	300ns	1/16	83.4μs	51.4μs
CF-4MHz	3.0V to 5.5V	1/1	750ns	1/8	104.5μs	64.5μs
	2.4V to 3.6V	1/1	750ns	1/32	416.5μs	256.5μs

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

### Power-on reset (POR) Characteristics at Ta = -40 to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification			
					min	typ	max	unit
POR release voltage	PORRL		• Select from option. (Note 7-1)	1.67V	1.55	1.67	1.79	V
				1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		• See Fig. 8. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.				100	ms

Note7-1: The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

## LC87F2J32A

### Low voltage detection reset (LVD) Characteristics at Ta = -40 to +85°C, V<sub>SS1</sub>=V<sub>SS2</sub>=V<sub>SS3</sub>=0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				Option selected voltage	min	typ	max	unit
LVD reset Voltage (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3) • See Fig. 9.	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD hysteresis width	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		• See Fig. 9. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Replv sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 10.		0.2			ms

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.



# LC87F2J32A

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(10)	V <sub>DD</sub> 1	• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		27	120	μA
				1.8 to 3.6		13	59	
	IDDOP(11)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	5.0		27	84	
				3.3		13	33	
				2.5		8.1	22	
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(1)	V <sub>DD</sub> 1	• HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		2.6	4.7	mA
				2.7 to 3.6		1.4	2.5	
	IDDHALT(2)		• HALT mode • CF1=24MHz external clock • System clock set to CF1 side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		4.0	6.9	
				3.0 to 3.6		2.0	3.4	
	IDDHALT(3)		• HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		2.2	4.4	
				2.2 to 3.6		1.2	2.3	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		1.2	3.0	
				1.8 to 3.6		0.6	1.4	
	IDDHALT(5)		• HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.2 to 5.5		0.6	1.5	
				2.2 to 3.6		0.3	0.7	
	IDDHALT(6)		• HALT mode • FsX'tal=32.768 kHz crystal oscillation mode • Internal Low speed RC oscillation stopped. • System clock set to internal Medium speed RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.3	0.9	
				1.8 to 3.6		0.2	0.5	

Note 9-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified

Continued on next page.

# LC87F2J32A

Continued from preceding page

Parameter	Symbol	Pin/ remarks	Conditions	Specification				
				V <sub>DD</sub> [V]	min.	typ.	max.	unit
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(7)	V <sub>DD</sub> 1	<ul style="list-style-type: none"><li>• HALT mode</li><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• Internal Low speed and Medium speed RC oscillation stopped.</li><li>• System clock set to 8MHz with Frequency variable RC oscillation</li><li>• 1/1 frequency division ratio</li></ul>	2.7 to 5.5		2.5	5.0	μA
				2.7 to 3.6		1.4	2.6	
	IDDHALT(8)		<ul style="list-style-type: none"><li>• HALT mode</li><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal Low speed RC oscillation.</li><li>• Internal Medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li></ul>	1.8 to 5.5		26	91	
				1.8 to 3.6		15	48	
	IDDHALT(9)		<ul style="list-style-type: none"><li>• HALT mode</li><li>• External FsX'tal and FmCF oscillation stopped.</li><li>• System clock set to internal Low speed RC oscillation.</li><li>• Internal Medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/1 frequency division ratio</li><li>• Ta=-10 to +50°C</li></ul>	5.0		26	52	
				3.3		15	26	
				2.5		10	18	
	IDDHALT(10)		<ul style="list-style-type: none"><li>• HALT mode</li><li>• FsX'tal=32.768 kHz crystal oscillation mode</li><li>• System clock set to 32.768kHz side</li><li>• Internal Low speed and Medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/2 frequency division ratio</li></ul>	1.8 to 5.5		16	96	
				1.8 to 3.6		6.2	43	
	IDDHALT(11)		<ul style="list-style-type: none"><li>• HALT mode</li><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• System clock set to 32.768kHz side</li><li>• Internal Low speed and Medium speed RC oscillation stopped.</li><li>• Frequency variable RC oscillation stopped.</li><li>• 1/2 frequency division ratio</li><li>• Ta=-10 to +50°C</li></ul>	5.0		16	56	
				3.3		6.2	18	
				2.5		3.4	11	
HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(1)	V <sub>DD</sub> 1	<div>HOLD mode</div> <ul style="list-style-type: none"><li>• CF1=V<sub>DD</sub> or open (External clock mode)</li></ul>	1.8 to 5.5		0.04	30	μA
				1.8 to 3.6		0.02	14	
	IDDHOLD(2)		<div>HOLD mode</div> <ul style="list-style-type: none"><li>• CF1=V<sub>DD</sub> or open (External clock mode)</li><li>• Ta=-10 to +50°C</li></ul>	5.0		0.04	2.8	
				3.3		0.02	1.2	
				2.5		0.015	0.9	
	IDDHOLD(3)		<div>HOLD mode</div> <ul style="list-style-type: none"><li>• CF1=V<sub>DD</sub> or open (External clock mode)</li><li>• LVD option selected</li></ul>	1.8 to 5.5		2.9	35	
				1.8 to 3.6		2.2	18	
	IDDHOLD(4)		<div>HOLD mode</div> <ul style="list-style-type: none"><li>• CF1=V<sub>DD</sub> or open (External clock mode)</li><li>• Ta=-10 to +50°C</li><li>• LVD option selected</li></ul>	5.0		2.9	7.2	
3.3				2.2	4.1			
2.5				1.9	3.4			
Timer HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(5)	V <sub>DD</sub> 1	<div>Timer HOLD mode</div> <ul style="list-style-type: none"><li>• FsX'tal=32.768kHz crystal oscillation mode</li></ul>	1.8 to 5.5		14	89	
				1.8 to 3.6		4.8	38	
	IDDHOLD(6)		<div>Timer HOLD mode</div> <ul style="list-style-type: none"><li>• FsX'tal=32.768kHz crystal oscillation mode</li><li>• Ta=-10 to +50°C</li></ul>	5.0		14	40	
				3.3		4.8	15	
				2.5		2.4	7.6	

Note 9-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	Open	330k	1.8 to 5.5	1.4	4.0	Applicable CL value= 7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

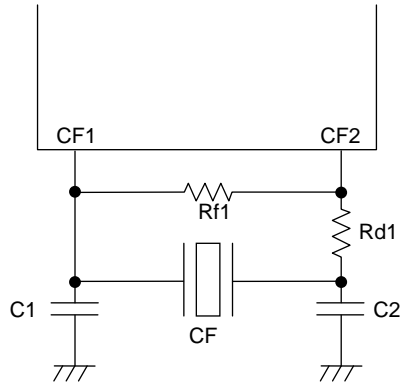


Figure 1 CF Oscillator Circuit

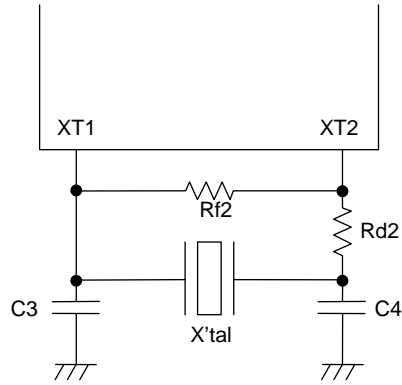


Figure 2 XT Oscillator Circuit

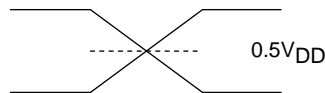
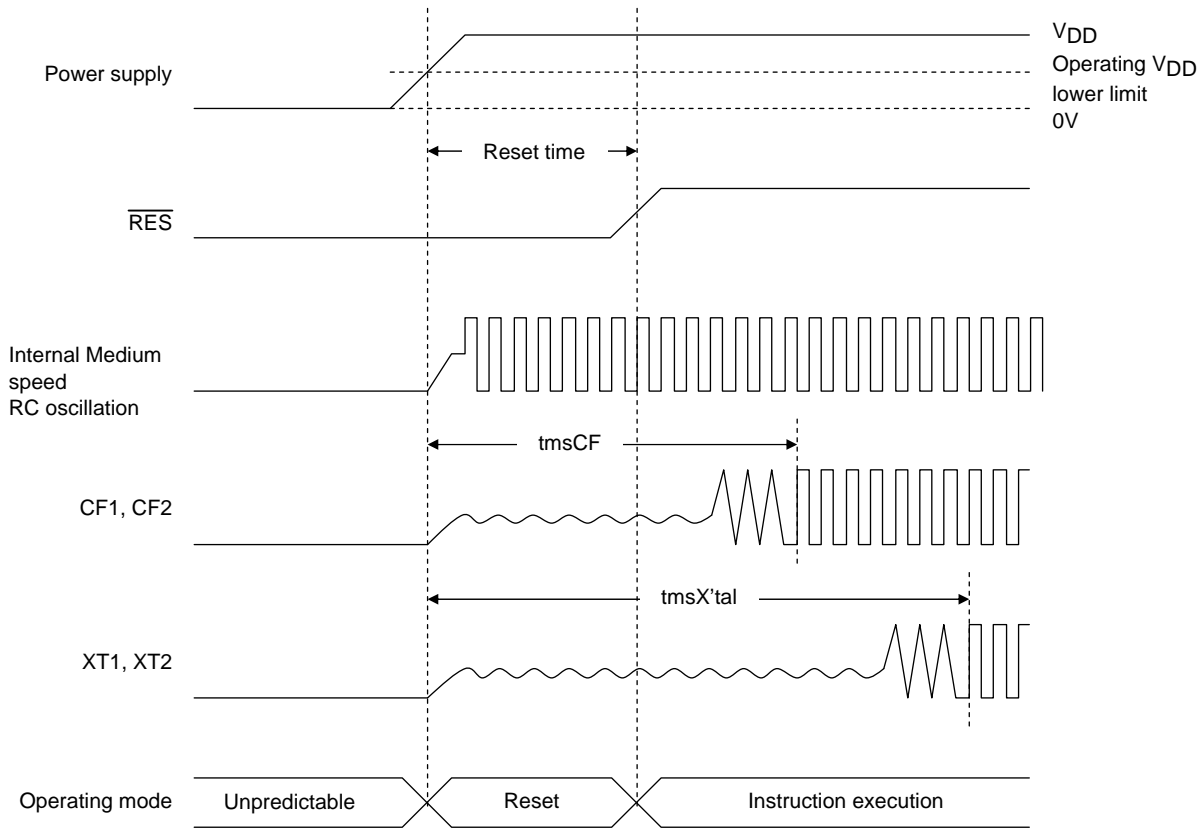
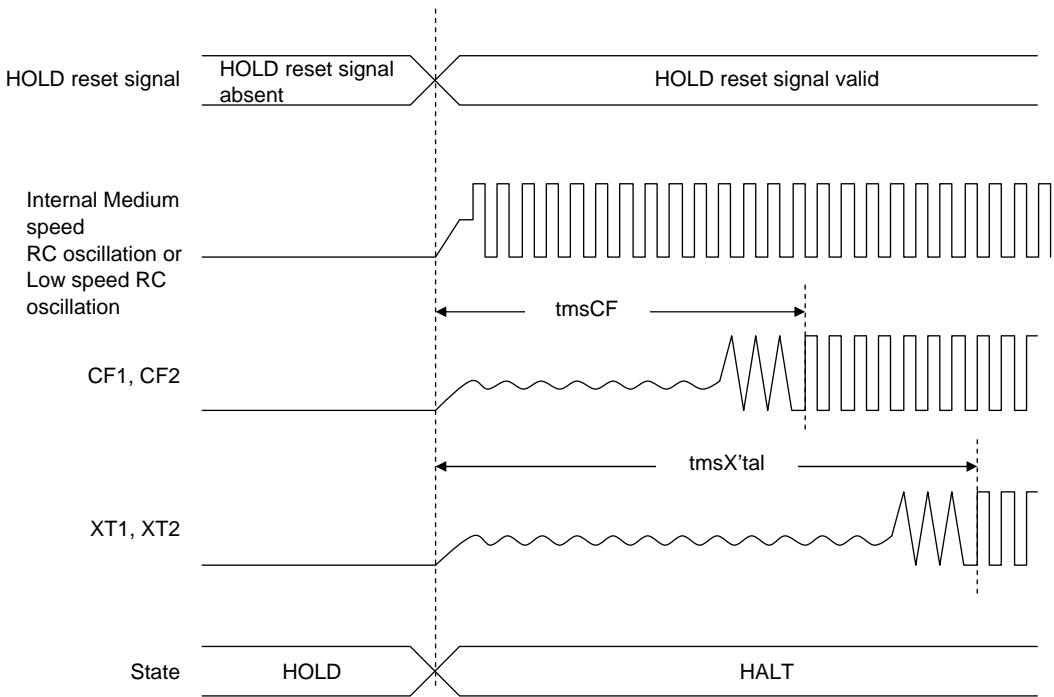


Figure 3 AC Timing Measurement Point



Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 4 Oscillation Stabilization Times

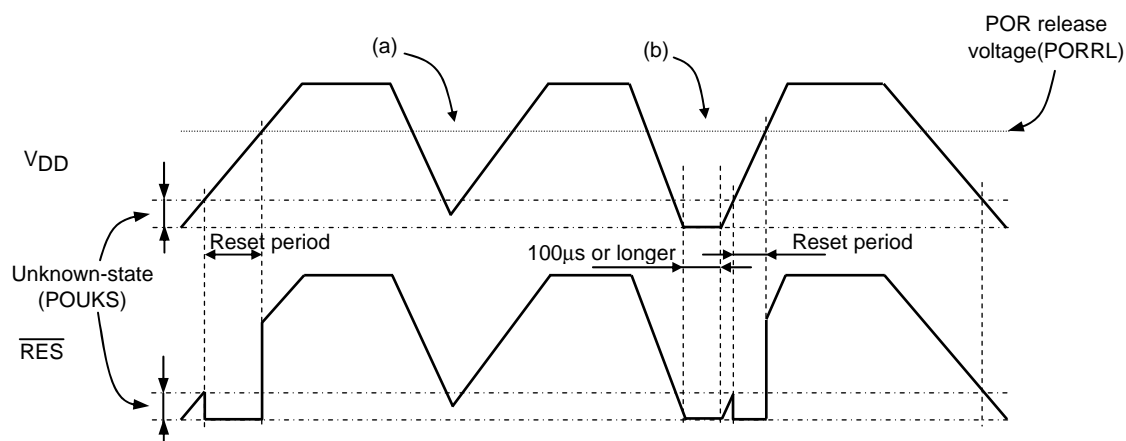


Figure 8 Waveform observed when only POR is used (LVD not used)  
(RESET pin: Pull-up resistor  $R_{RES}$  only)

- The POR function generates a reset only when power is turned on starting at the  $V_{SS}$  level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the  $V_{SS}$  level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the  $V_{SS}$  level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

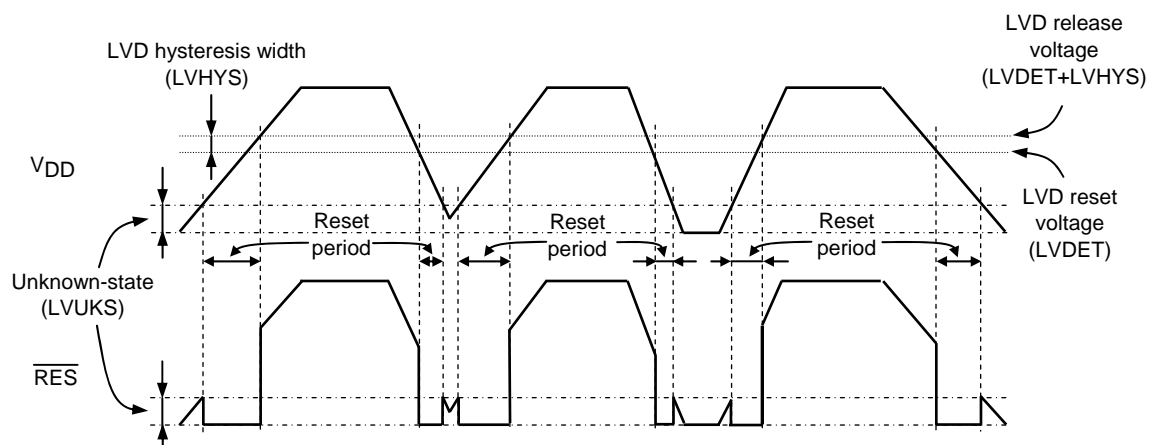


Figure 9 Waveform observed when both POR and LVD functions are used  
(RESET pin: Pull-up resistor  $R_{RES}$  only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.