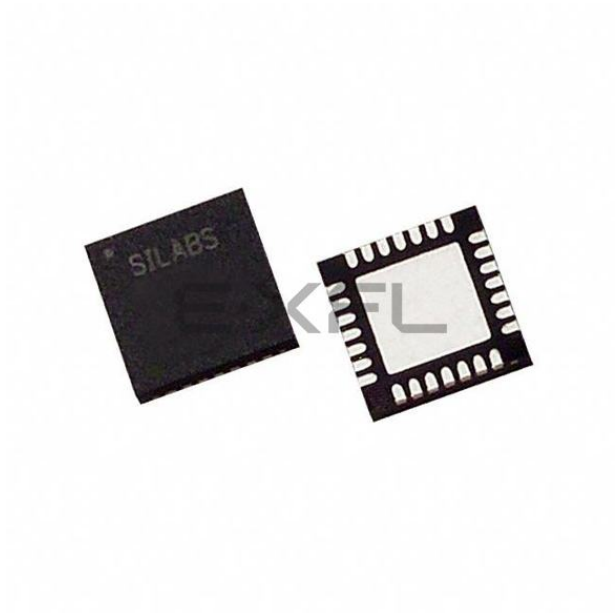

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	UART/USART, USB
Peripherals	POR
Number of I/O	15
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f326-gmr

Figure 1.3. Typical Connections for the C8051F326

Figure 1.4. Typical Connections for the C8051F327

3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
I/O Supply Voltage (VIO)[1,2]		1.8	3.3	3.6	V
Core Supply Voltage (VDD)[3]		2.7	3.3	3.6	V
Core Supply Current with CPU Active	VDD = 3.3 V, Clock = 24 MHz VDD = 3.3 V, Clock = 3 MHz VDD = 3.3 V, Clock = 32 kHz	— — —	11 1.9 20	— — —	mA mA µA
Core Supply Current with CPU Inactive (not accessing Flash)	VDD = 3.3 V, Clock = 24 MHz VDD = 3.3 V, Clock = 3 MHz VDD = 3.3 V, Clock = 32 kHz	— — —	4.4 0.83 13	— — —	mA mA µA
Digital Supply Current (suspend mode or shutdown mode)	Oscillator not running	—	< 0.1	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[4]		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C

Notes:
1. The I/O Supply Voltage (VIO) must be less than or equal to the Core Supply Voltage (VDD).
2. For C8051F327 devices, VIO is internally connected to VDD.
3. USB Requires 3.0 V Minimum Core Supply Voltage (VDD).
4. SYSCLK must be at least 32 kHz to enable debugging.

Notes on Registers, Operands and Addressing Modes:
Rn - Register R0-R7 of the currently selected register bank. @Ri - Data RAM location addressed indirectly through R0 or R1. **rel** - 8-bit, signed (2s complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps. **direct** - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00-0x7F) or an SFR (0x80-0xFF). **#data** - 8-bit constant **#data16** - 16-bit constant **bit** - Direct-accessed bit in Data RAM or SFR **addr11** - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction. **addr16** - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space. There is one unused opcode (0xA5) that performs the same function as NOP. All mnemonics copyrighted © Intel Corporation 1980.

SFR Definition 6.7. IE: Interrupt Enable

R/W	R	R	R/W	R/W	R/W	R/W	R/W	Reset Value
EA	—	—	ES0	ET1	EX1	ET0	EX0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xA8

Bit7: EA: Enable All Interrupts.
This bit globally enables/disables all interrupts. It overrides the individual interrupt mask settings.
0: Disable all interrupt sources.
1: Enable each interrupt according to its individual mask setting.

Bit6–5: Unused. Read = 00b. Write = don't care.

Bit4: ES0: Enable UART0 Interrupt.
This bit sets the masking of the UART0 interrupt.
0: Disable UART0 interrupt.
1: Enable UART0 interrupt.

Bit3: ET1: Enable Timer 1 Interrupt.
This bit sets the masking of the Timer 1 interrupt.
0: Disable all Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag.

Bit2: EX1: Enable External Interrupt 1.
This bit sets the masking of External Interrupt 1.
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the /INT1 input.

Bit1: ET0: Enable Timer 0 Interrupt.
This bit sets the masking of the Timer 0 interrupt.
0: Disable all Timer 0 interrupt.
1: Enable interrupt requests generated by the TF0 flag.

Bit0: EX0: Enable External Interrupt 0.
This bit sets the masking of External Interrupt 0.
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the /INT0 input.

SFR Definition 7.2. RSTSRC: Reset Source

R/W	R	R	R/W	R	R/W	R/W	R	Reset Value
USBRSF	FERROR	—	SWRSF	—	MCDRSF	PORSF	PINRSF	Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xEF

Bit7: USBRSF: USB Reset Flag
0: **Read:** Last reset was not a USB reset; **Write:** USB resets disabled.
1: **Read:** Last reset was a USB reset; **Write:** USB resets enabled.

Bit6: FERROR: Flash Error Indicator.
0: Source of last reset was not a Flash read/write/erase error.
1: Source of last reset was a Flash read/write/erase error.

Bit5: Unused. Read = 0. Write = don't care.

Bit4: SWRSF: Software Reset Force and Flag.
0: **Read:** Source of last reset was not a write to the SWRSF bit; **Write:** No Effect.
1: **Read:** Source of last was a write to the SWRSF bit; **Write:** Forces a system reset.

Bit3: Unused. Read = 0. Write = don't care.

Bit2: MCDRSF: Missing Clock Detector Flag.
0: **Read:** Source of last reset was not a Missing Clock Detector timeout; **Write:** Missing Clock Detector disabled.
1: **Read:** Source of last reset was a Missing Clock Detector timeout; **Write:** Missing Clock Detector enabled; triggers a reset if a missing clock condition is detected.

Bit1: PORSF: Power-On / VDD Monitor Reset Flag.
This bit is set anytime a power-on reset occurs. Writing this bit selects/deselects the VDD monitor as a reset source. **Note: writing '1' to this bit before the VDD monitor is enabled and stabilized can cause a system reset.** See register VDM0CN (Figure 7.1).
0: **Read:** Last reset was not a power-on or VDD monitor reset; **Write:** VDD monitor is not a reset source.
1: **Read:** Last reset was a power-on or VDD monitor reset; all other reset flags indeterminate; **Write:** VDD monitor is a reset source.

Bit0: PINRSF: HW Pin Reset Flag.
0: Source of last reset was not $\overline{\text{RST}}$ pin.
1: Source of last reset was $\overline{\text{RST}}$ pin.

Note: Do not use read-modify-write instructions on this register.

8. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system, a single byte at a time, through the C2 interface or by software using the MOVX instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operation is not required. Code execution is stalled during a Flash write/erase operation. Refer to Table 8.1 for complete Flash memory electrical characteristics.

8.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Laboratories or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section “15. C2 Interface” on page 135.

To ensure the integrity of Flash contents, it is strongly recommended that the on-chip VDD Monitor be enabled in any system that includes code that writes and/or erases Flash memory from software.

8.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in Figure 8.2.

8.1.2. Flash Erase Procedure

The Flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before writing to Flash memory using MOVX, Flash write operations must be enabled by: (1) Writing the Flash key codes in sequence to the Flash Lock register (FLKEY); and (2) Setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 (this directs the MOVX writes to target Flash memory). The PSWE bit remains set until cleared by software.

A write to Flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in Flash. **A byte location to be programmed must be erased before a new value is written.** The Flash memory is organized in 512-byte pages. The erase operation applies to an entire page (setting all bytes in the page to 0xFF). To erase an entire 512-byte page, perform the following steps:

Step 1. Disable interrupts (recommended).
Step 2. Write the first key code to FLKEY: 0xA5.
Step 3. Write the second key code to FLKEY: 0xF1.
Step 4. Set the PSEE bit (register PSCTL).
Step 5. Set the PSWE bit (register PSCTL).
Step 6. Using the MOVX instruction, write a data byte to any location within the 512-byte page to be erased.
Step 7. Clear the PSWE bit (register PSCTL).
Step 8. Clear the PSEE bit (register PSCTI).

SFR Definition 8.2. FLKEY: Flash Lock and Key

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xB7

Bits7–0: FLKEY: Flash Lock and Key Register
Write:
This register must be written to before Flash writes or erases can be performed. Flash remains locked until this register is written to with the following key codes: 0xA5, 0xF1. The timing of the writes does not matter, as long as the codes are written in order. The key codes must be written for each Flash write or erase operation. Flash will be locked until the next system reset if the wrong codes are written or if a Flash operation is attempted before the codes have been written correctly.
Read:
When read, bits 1-0 indicate the current Flash lock state.
00: Flash is write/erase locked.
01: The first key code has been written (0xA5).
10: Flash is unlocked (writes/erases allowed).
11: Flash writes/erases disabled until the next reset.

SFR Definition 8.3. FLSCL: Flash Scale

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
FOSE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xB6

Bits7: FOSE: Flash One-shot Enable
This bit enables the Flash read one-shot. When the Flash one-shot disabled, the Flash sense amps are enabled for a full clock cycle during Flash reads. At system clock frequencies below 10 MHz, disabling the Flash one-shot will increase system power consumption.
0: Flash one-shot disabled.
1: Flash one-shot enabled.
Bits6–0: Reserved. Read = 0. Must Write 0.

9.2. Accessing USB FIFO Space

The upper 256 bytes of XRAM functions as USB FIFO space. Figure 9.2 shows an expanded view of the FIFO space and user XRAM. FIFO space is accessed via USB FIFO registers; see Section “12.5. FIFO Management” on page 95 for more information on accessing these FIFOs. The FIFO block operates on the USB clock domain; thus the USB clock must be active when accessing FIFO space.

Important Note: The USB clock must be active when accessing FIFO space.

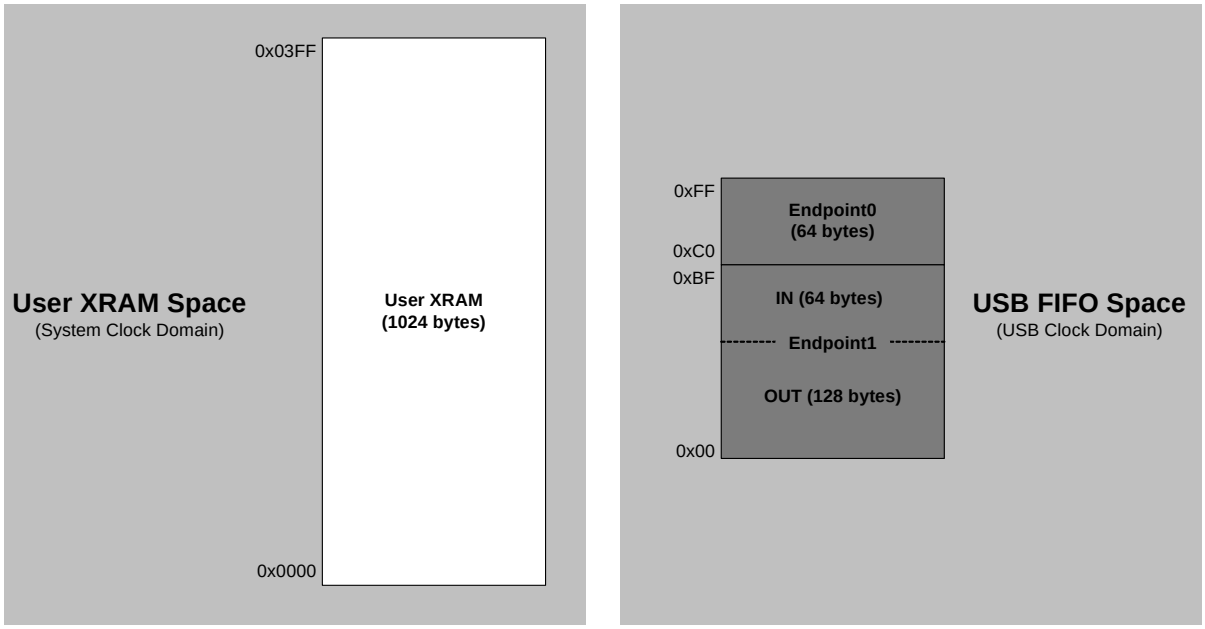

Figure 9.2. XRAM Memory Map Expanded View

SFR Definition 9.1. EMI0CN: External Memory Interface Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	PGSEL1	PGSEL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xAA

Bits7–3: Unused. Read = 000000b. Write = don’t care.
Bits2–0: PGSEL[1:0]: XRAM Page Select Bits.
The XRAM Page Select Bits provide the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. The upper 6-bits are "don't cares", so the 1k address block is repeated modulo over the entire 64k external data memory address space.

10.1.1. Adjusting the Internal Oscillator on C8051F326/7 Devices

The OSCICL reset value is factory calibrated to result in a 12 MHz internal oscillator with a ±1.5% accuracy; this frequency is suitable for use as the USB clock (see Section “10.5. System and USB Clock Selection” on page 76). Software may adjust the frequency of the internal oscillator using the OSCICL register.

Important Note: Once the internal oscillator frequency has been modified, the internal oscillator may not be used as the USB clock as described in Section “10.5. System and USB Clock Selection” on page 76. The internal oscillator frequency will reset to its original factory-calibrated frequency following any device reset, at which point the oscillator is suitable for use as the USB clock.

10.1.2. Internal Oscillator Suspend Mode

The internal oscillator may be placed in Suspend mode by writing ‘1’ to the SUSPEND bit in register OSCICN. In Suspend mode, the internal oscillator is stopped until a non-idle USB event is detected (Section “12. Universal Serial Bus Controller (USB0)” on page 87) or VBUS matches the polarity selected by the VBPOL bit in register REG0CN (Section “5.2. VBUS Detection” on page 31). Note that the USB transceiver must be enabled or in Suspend mode for a USB event to be detected.

SFR Definition 10.1. OSCICN: Internal Oscillator Control

R/W	R	R/W	R	R/W	R/W	R/W	R/W	Reset Value
IOSCEN	IFRDY	SUSPEND	—	—	—	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB2

Bit7: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled.
1: Internal Oscillator Enabled.

Bit6: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.

Bit5: SUSPEND: Force Suspend
Writing a ‘1’ to this bit will force the internal oscillator to be stopped. The oscillator will be restarted on the next non-idle USB event (i.e., RESUME signaling) or VBUS interrupt event (see SFR Definition 5.1).

Bits4–2: Unused. Read = 000b. Write = don't care.

Bits1–0: IFCN1–0: Internal Oscillator Frequency Control Bits.
00: SYSCLK derived from Internal Oscillator divided by 8.
01: SYSCLK derived from Internal Oscillator divided by 4.
10: SYSCLK derived from Internal Oscillator divided by 2.
11: SYSCLK derived from Internal Oscillator divided by 1.

10.5. System and USB Clock Selection

The internal oscillator requires little start-up time and may be selected as the system or USB clock immediately following the OSCICN write that enables the internal oscillator. If the external clock is selected as the system or USB clock, then startup times may vary based on the specifications of the external clock.

10.5.1. System Clock Selection

The CLKSL[2:0] bits in register CLKSEL select which oscillator source is used as the system clock. CLKSL[2:0] must be set to 001b for the system clock to run from the external clock; however the external clock may still clock certain peripherals (timers, UART, USB) when the internal oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillator, external clock, low frequency oscillator, and 4x Clock Multiplier so long as the selected oscillator is enabled and can provide a stable clock.

10.5.2. USB Clock Selection

The USBCLK[1:0] bits in register CLKSEL select which oscillator source is used as the USB clock. The USB clock may be derived from the 4x Clock Multiplier output, internal oscillator divided by 2, or an external clock. The USB clock source may also be turned off. The USB clock must be 48 MHz when operating USB0 as a Full Speed Function; the USB clock must be 6 MHz when operating USB0 as a Low Speed Function. See Figure 10.5 for USB clock selection options.

Some example USB clock configurations for Full and Low Speed mode are given below:

Table 10.1. Typical USB Full Speed Clock Settings

Internal Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Clock Multiplier	USBCLK = 00b
Clock Multiplier Input	Internal Oscillator*	MULSEL = 0b
Internal Oscillator	Divide by 1	IFCN = 11b
External Clock		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Clock Multiplier	USBCLK = 10b
Clock Multiplier Input	External Clock	MULSEL = 1b
Port I/O	12 MHz CMOS Clock	INPUTEN = 1b (GPIOCN.6)
***Note:** Clock Recovery must be enabled for this configuration.		

Table 10.2. Typical USB Low Speed Clock Settings

Internal Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Internal Oscillator / 2	USBCLK = 01b
Internal Oscillator	Divide by 1	IFCN = 11b
External Clock		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	External Clock	USBCLK = 10b
Port I/O	6 MHz CMOS Clock	INPUTEN = 1b (GPIOCN.6)

SFR Definition 11.4. P2: Port2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xA0

Bits7–6: Unused. Read = 00b. Write = don't care.
Bits5–0: P2.[5:0]
Write - Output appears on I/O pins.
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding P2MDOUT.n bit = 0).
Read - Always reads '0' if INPUTEN = '0'. Otherwise, directly reads Port pin.
0: P2.n pin is logic low.
1: P2.n pin is logic high.

SFR Definition 11.5. P2MDOUT: Port2 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—							00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xA6

Bits7–6: Unused. Read = 00b. Write = don't care.
Bits5–0: Output Configuration Bit for P2.5–2.0:
0: P2.0 Output is open-drain.
1: P2.0 Output is push-pull.

SFR Definition 11.6. P3: Port3

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—	—	—	—	—	—	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xB0

Bits7–1: Unused. Read = 0000000b. Write = don't care.
Bit0: P3.0
Write - Output appears on I/O pins.
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding P3MDOUT.n bit = 0).
Read - Always reads '0' if INPUTEN = '0'. Otherwise, directly reads Port pin.
0: P3.n pin is logic low.
1: P3.n pin is logic high.

12.1. Endpoint Addressing

A total of three endpoint pipes are available. The control endpoint (Endpoint0) always functions as a bi-directional IN/OUT endpoint. Endpoint 1 is implemented as a 64 byte IN pipe and a 128 byte OUT pipe:

Table 12.1. Endpoint Addressing Scheme

Endpoint	Associated Pipes	USB Protocol Address
Endpoint0	Endpoint0 IN	0x00
	Endpoint0 OUT	0x00
Endpoint1	Endpoint1 IN	0x81
	Endpoint1 OUT	0x01

12.2. USB Transceiver

The USB Transceiver is configured via the USB0XCN register shown in Figure 12.1. This configuration includes Transceiver enable/disable, pullup resistor enable/disable, and device speed selection (Full or Low Speed). When bit SPEED = ‘1’, USB0 operates as a Full Speed USB function, and the on-chip pullup resistor (if enabled) appears on the D+ pin. When bit SPEED = ‘0’, USB0 operates as a Low Speed USB function, and the on-chip pullup resistor (if enabled) appears on the D- pin. Bits4-0 of register USB0XCN can be used for Transceiver testing as described in Figure 12.1. The pullup resistor is enabled only when VBUS is present (see Section “5.2. VBUS Detection” on page 31 for details on VBUS detection).

Important Note: The USB clock should be active before the Transceiver is enabled.

12.11. Configuring Endpoint1

Endpoint1 is configured and controlled through a set of control/status registers: IN registers EINCSRL and EINCSRH, and OUT registers EOUTCSRL and EOUTCSRH. The endpoint control/status registers are mapped into the USB register address space based on the contents of the INDEX register (Figure 12.4).

12.12. Controlling Endpoint1 IN

Endpoint1 IN is managed via USB registers EINCSRL and EINCSRH. The IN endpoint can be used for Interrupt, Bulk, or Isochronous transfers. Isochronous (ISO) mode is enabled by writing '1' to the ISO bit in register EINCSRH. Bulk and Interrupt transfers are handled identically by hardware.

An Endpoint1 IN interrupt is generated by any of the following conditions:

1. An IN packet is successfully transferred to the host.
2. Software writes '1' to the FLUSH bit (EINCSRL.3) when the target FIFO is not empty.
3. Hardware generates a STALL condition.

12.12.1.Endpoint1 IN Interrupt or Bulk Mode

When the ISO bit (EINCSRH.6) is logic 0, Endpoint1 operates in Bulk or Interrupt Mode. Once it has been configured to operate in Bulk/Interrupt IN mode (typically following an Endpoint0 SET_INTERFACE command), firmware should load an IN packet into the endpoint IN FIFO and set the INPRDY bit (EINCSRL.0). Upon reception of an IN token, hardware will transmit the data, clear the INPRDY bit, and generate an interrupt.

Writing '1' to INPRDY without writing any data to the endpoint FIFO will cause a zero-length packet to be transmitted upon reception of the next IN token.

A Bulk or Interrupt pipe can be shut down (or Halted) by writing '1' to the SDSTL bit (EINCSRL.4). While SDSTL = '1', hardware will respond to all IN requests with a STALL condition. Each time hardware generates a STALL condition, an interrupt will be generated and the STSTL bit (EINCSRL.5) set to '1'. The STSTL bit must be reset to '0' by firmware.

Hardware will automatically reset INPRDY to '0' when a packet slot is open in the endpoint FIFO. If double buffering is enabled for the target endpoint, it is possible for firmware to load two packets into the IN FIFO at a time. In this case, hardware will reset INPRDY to '0' immediately after firmware loads the first packet into the FIFO and sets INPRDY to '1'. An interrupt will not be generated in this case; an interrupt will only be generated when a data packet is transmitted.

When firmware writes '1' to the FCDT bit (EINCSRH.3), the data toggle for each IN packet will be toggled continuously, regardless of the handshake received from the host. This feature is typically used by Interrupt endpoints functioning as rate feedback communication for Isochronous endpoints. When FCDT = '0', the data toggle bit will only be toggled when an ACK is sent from the host in response to an IN packet.

12.12.2.Endpoint1 IN Isochronous Mode

When the ISO bit (EINCSRH.6) is set to '1', the target endpoint operates in Isochronous (ISO) mode. Once an endpoint has been configured for ISO IN mode, the host will send one IN token (data request) per frame; the location of data within each frame may vary. Therefore, it is recommended that double buffering be enabled when using Endpoint1 IN as an Isochronous endpoint.

12.13. Controlling Endpoint1 OUT

Endpoint1 OUT is managed via USB registers EOUTCSRL and EOUTCSRH. It can be used for Interrupt, Bulk, or Isochronous transfers. Isochronous (ISO) mode is enabled by writing ‘1’ to the ISO bit in register EOUTCSRH. Bulk and Interrupt transfers are handled identically by hardware.

An Endpoint1 OUT interrupt may be generated by the following:

1. Hardware sets the OPRDY bit (EINCSRL.0) to ‘1’.
2. Hardware generates a STALL condition.

12.13.1.Endpoint1 OUT Interrupt or Bulk Mode

When the ISO bit (EOUTCSRH.6) is logic 0, Endpoint1 operates in Bulk or Interrupt mode. Once it has been configured to operate in Bulk/Interrupt OUT mode (typically following an Endpoint0 SET_INTERFACE command), hardware will set the OPRDY bit (EOUTCSRL.0) to ‘1’ and generate an interrupt upon reception of an OUT token and data packet. The number of bytes in the current OUT data packet (the packet ready to be unloaded from the FIFO) is given in the EOUTCNTH and EOUTCNTL registers. In response to this interrupt, firmware should unload the data packet from the OUT FIFO and reset the OPRDY bit to ‘0’.

A Bulk or Interrupt pipe can be shut down (or Halted) by writing ‘1’ to the SDSTL bit (EOUTCSRL.5). While SDSTL = ‘1’, hardware will respond to all OUT requests with a STALL condition. Each time hardware generates a STALL condition, an interrupt will be generated and the STSTL bit (EOUTCSRL.6) set to ‘1’. The STSTL bit must be reset to ‘0’ by firmware.

Hardware will automatically set OPRDY when a packet is ready in the OUT FIFO. Note that if double buffering is enabled for Endpoint1, it is possible for two packets to be ready in the OUT FIFO at a time. In this case, hardware will set OPRDY to ‘1’ immediately after firmware unloads the first packet and resets OPRDY to ‘0’. A second interrupt will be generated in this case.

12.13.2.Endpoint1 OUT Isochronous Mode

When the ISO bit (EOUTCSRH.6) is set to ‘1’, Endpoint1 operates in Isochronous (ISO) mode. Once it has been configured for ISO OUT mode, the host will send exactly one data per USB frame; the location of the data packet within each frame may vary, however. Because of this, it is recommended that double buffering be enabled when Endpoint1 is used in Isochronous mode.

Each time a data packet is received, hardware will load the received data packet into the endpoint FIFO, set the OPRDY bit (EOUTCSRL.0) to ‘1’, and generate an interrupt (if enabled). Firmware would typically use this interrupt to unload the data packet from the endpoint FIFO and reset the OPRDY bit to ‘0’.

If a data packet is received when there is no room in the endpoint FIFO, an interrupt will be generated and the OVRUN bit (EOUTCSRL.2) set to ‘1’. If USB0 receives an ISO data packet with a CRC error, the data packet will be loaded into the endpoint FIFO, OPRDY will be set to ‘1’, an interrupt (if enabled) will be generated, and the DATAERR bit (EOUTCSRL.3) will be set to ‘1’. Software should check the DATAERR bit each time a data packet is unloaded from an ISO OUT endpoint FIFO.

Table 12.4. USB Transceiver Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
USB Operating Current		Full Speed Low Speed	— —	5.7 1.5	— —	mA
Transmitter						
Output High Voltage	V_{OH}		2.8	—		V
Output Low Voltage	V_{OL}		—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High Driving Low	— —	38 38	— —	W
Pullup Resistance	R_{PU}	Full Speed (D+ Pullup) Low Speed (D– Pullup)	1.425 —	1.5 —	1.575 —	kW
Output Rise Time	T_R	Low Speed Full Speed	75 4	— —	300 20	ns
Output Fall Time	T_F	Low Speed Full Speed	75 4	— —	300 20	ns
Receiver						
Differential Input Sensitivity	V_{DI}	| (D+) – (D–) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Note: Refer to the USB Specification for timing diagrams and symbol definitions.						

Table 13.1. Baud Rate Generator Settings for Standard Baud Rates

	Target Baud Rate (bps)	Actual Baud Rate (bps)	Baud Rate Error	Oscillator Divide Factor	SB1PS[1:0] (Prescaler Bits)	Reload Value in SBRLH1:SBRLL1
BRG Clock = 12 MHz	230400	230769	0.16%	52	11	0xFFE6
	115200	115385	0.16%	104	11	0xFFCC
	57600	57692	0.16%	208	11	0xFF98
	28800	28846	0.16%	416	11	0xFF30
	14400	14388	0.08%	834	11	0xFE5F
	9600	9600	0.0%	1250	11	0xFD8F
	2400	2400	0.0%	5000	11	0xF63C
	1200	1200	0.0%	10000	11	0xEC78
BRG Clock = 24 MHz	230400	230769	0.16%	104	11	0xFFCC
	115200	115385	0.16%	208	11	0xFF98
	57600	57692	0.16%	416	11	0xFF30
	28800	28777	0.08%	834	11	0xFE5F
	14400	14406	0.04%	1666	11	0xFCBF
	9600	9600	0.0%	2500	11	0xFB1E
	2400	2400	0.0%	10000	11	0xEC78
	1200	1200	0.0%	20000	11	0xD8F0
BRG Clock = 48 MHz	230400	230769	0.16%	208	11	0xFF98
	115200	115385	0.16%	416	11	0xFF30
	57600	57554	0.08%	834	11	0xFE5F
	28800	28812	0.04%	1666	11	0xFCBF
	14400	14397	0.02%	3334	11	0xF97D
	9600	9600	0.0%	5000	11	0xF63C
	2400	2400	0.0%	20000	11	0xD8F0
	1200	1200	0.0%	40000	11	0xB1E0

SFR Definition 13.5. SBRLH0: UART0 Baud Rate Generator High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x94

Bits7-0: SBRLH0[7:0]: High Byte of reload value for UART0 Baud Rate Generator.

SFR Definition 13.6. SBRLL0: UART0 Baud Rate Generator Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x93

Bits7-0: SBRLL0[7:0]: Low Byte of reload value for UART0 Baud Rate Generator.

14.1.1. Mode 0: 13-bit Timer

Timer 0 and Timer 1 operate as 13-bit timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit timer. TL0 holds the five LSBs in bit positions TL0.4-TL0.0. The three upper bits of TL0 (TL0.7-TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or GATE0 is logic 1 and the input signal /INT0 is active. Setting GATE0 to logic 1 allows the timer to be controlled by the external input signal /INT0, facilitating pulse width measurements. When GATE0 is set to logic 1, the /INT0 input pin is P0.2.

Table 14.2. Timer 0 Operation

TR0	GATE0	/INT0	Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0 (P0.2 High)	Disabled
1	1	1 (P0.2 Low)	Enabled

X = Don't Care

See Table 6.4 on page 49 for detailed information on how GATE0 affects /INT0 functionality.

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled. TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal /INT1 is used with Timer 1. See Section “6.3.2. External Interrupts” on page 49 for a complete description of /INT0 and /INT1.

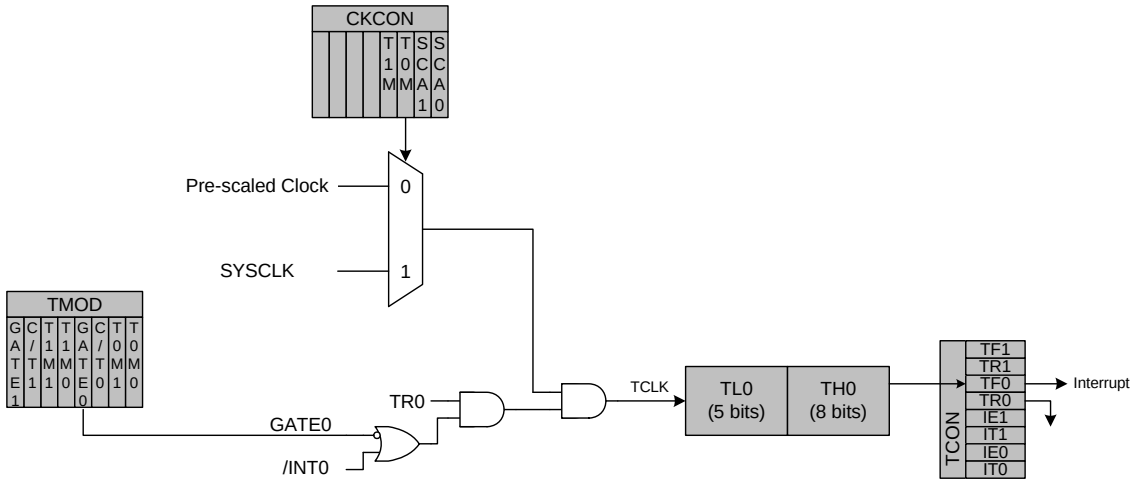

Figure 14.1. T0 Mode 0 Block Diagram

14.1.2. Mode 1: 16-bit Timer

Mode 1 operation is the same as Mode 0, except that the timer registers use all 16 bits. The timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

14.1.3. Mode 2: 8-bit Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when GATE0 (TMOD.3) is logic 0 or when GATE0 is logic 1 and the input signal /INT0 is active (see Section “6.3.2. External Interrupts” on page 49 for details on the external input signals /INT0 and /INT1).

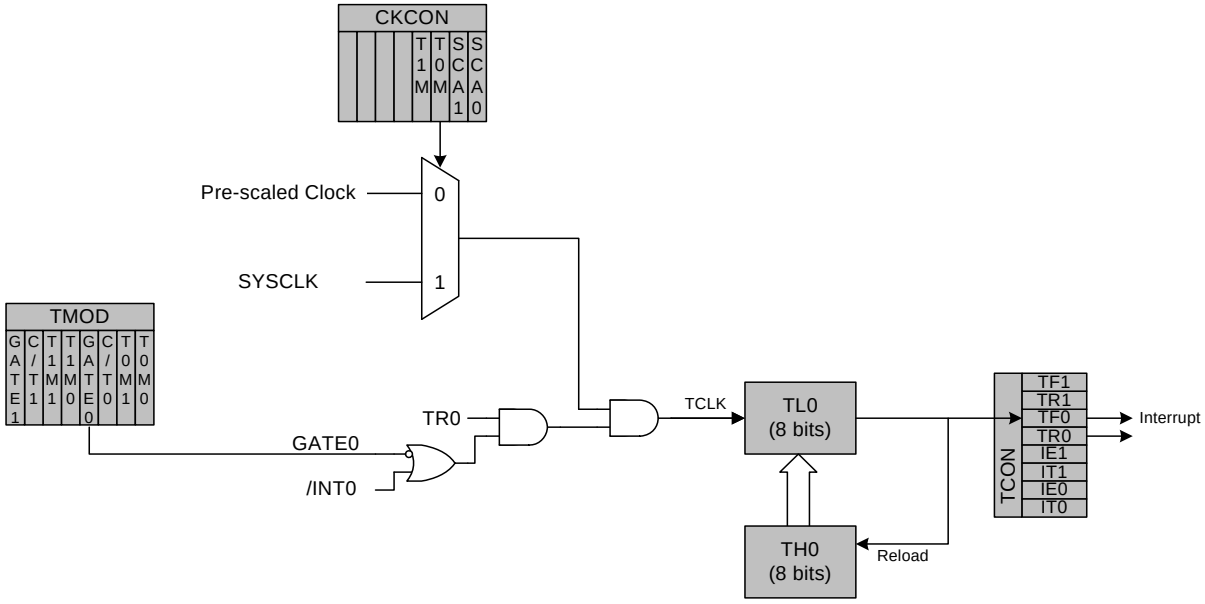

Figure 14.2. T0 Mode 2 Block Diagram

NOTES: