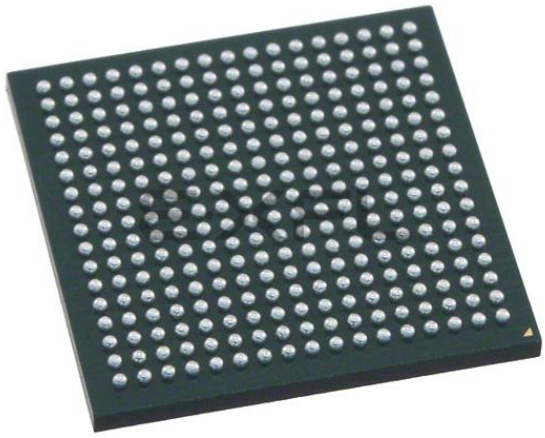

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; C3
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	Cryptography
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spear300-2

List of tables

List of figures

- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes
  - CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bit general purpose timers with programmable prescaler.
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1
- Boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x15 mm, pitch 0.8 mm)

DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.

- **DOZE mode**: In this mode the system clocks, HCLK and CPU_CLK, and the System Controller clock are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

2.3 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

2.4 General purpose timers

SPEAr300 provides three general purpose timers (GPTs) acting as APB slaves.

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through SPEAr300 configuration registers (frequencies ranging from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available:

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

2.5 Watchdog timer

The watchdog timer consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

2.16 SPI_I2C multiple slave control

The SPI interface has only one slave select signal, SS0.

The I^2C interface does not allow control of several devices with the same address, which is frequently required for CODECs.

The SPI_I2C extension allows management of up to 8 SPI devices, or 8 I^2C devices at the same address (total SPI+I^2C devices=8).

The SPI extension is made by generating three more slave select signals SS1, SS2 and SS3.

The I^2C extension is done by replicating the I2C_SCL signal if the corresponding pin is set active.Otherwise the pin remains low, so that the start condition is not met.

Each of the 8 pins can reproduce either the SPI SS0 signal, or the I2C_SCL signal. The selection is made through a register.

2.17 TDM interface

The TDM block implements time division multiplexing.

Main features:

- TDM interface with 512 timeslots and up to 16 bufferization channels.
- 32 ms bufferization for 16 channels (of 4 bytes each)
- Supports master and slave mode operation
- Programmable clock and synchronization signal generation in master mode
- Clock & synchronization signal recovery in slave mode
- 8 programmable synchronization signals for CODECs
- Uses 11 pins:
  - SYNC7-0 are dedicated frame syncs for CODECs without timeslot recognition
  - CLK is the TDM clock
  - DIN is the TDM input and receives the data
  - DOUT is the TDM output and transmits the data. It can be high impedance on a unused timeslot
- The TDM interface can be the master or a slave of the CLK or SYNC0 signals.
- Timeslots can be used for switching or bufferization purposes:
  - Switching and bufferization can be used concurrently for different timeslots on the same TDM
  - The only limitation is that an output timeslot can not be switched and bufferized at the same time.
  - Timeslot switching: any of the output time slots can receive any input timeslot of the previous frame. The connection memory is part of the action memory, indicating which timeslot has to be output.
  - Timeslot bufferization: data from DIN is stored in an input buffer and data from an output buffer is played on DOUT. When the number of samples stored/played reaches the buffer size, the processor is interrupted in order to read the input buffer and prepare a new output buffer (or a DMA request is generated).

2.20 Keyboard controller

SPEAr300 provides a GPIO/keyboard controller block which is a two-mode input and output port.

Main features:

- The selection between the two modes is an APB Bus programmable bit.
- Keyboard interface uses 18 pins
- 18-bit general-purpose parallel port with input or output single pin programmability
- Pins can be used as general purpose I/O or to drive a 9 x 9 keyboard (81 keys)
- Keyboard scan period can be adjusted between 10 ms and 80 ms
- Supports auto-scanning with debouncing.

2.21 CLCD controller

SPEAr300 has a color liquid crystal display controller (CLCDC) that provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian

Main features:

- Input data must be 32-bits wide, either in 2's complement or binary form.
- Oversampling min 32, max 256
- S/N ratio is 82 dB, THD is 72 dB (Measured on a 1 kHz sine wave x64 over sampled by the processor and x32 by the DAC)
- Dynamic: 80% of full scale
- Optionally, the order of the noise shaper can be set to 1

Table 8. DDR pin description (continued)

Group	Signal name	Ball	Direction	Function	Pin type
DDR	DDR_CS_0	P9	Output	Chip Select	SSTL_2/SSTL_18
	DDR_CS_1	R9			
	DDR_ODT_0	T3	I/O	On-Die Termination Enable lines	
	DDR_ODT_1	T4			
	DDR_DATA_0	P11	I/O	Data Lines (Lower byte)	
	DDR_DATA_1	R11			
	DDR_DATA_2	T11			
	DDR_DATA_3	U11			
	DDR_DATA_4	T12			
	DDR_DATA_5	R12			
	DDR_DATA_6	P12			
	DDR_DATA_7	P13			
	DDR_DQS_0	U10	Output	Lower Data Strobe	Differential SSTL_2/SSTL_18
	DDR_nDQS_0	T10			
	DDR_DM_0	U12	Output	Lower Data Mask	SSTL_2/SSTL_18
	DDR_GATE_0	R10	I/O	Lower Gate Open	
	DDR_DATA_8	T17	I/O	Data Lines (Upper byte)	
	DDR_DATA_9	T16			
	DDR_DATA_10	U17			
	DDR_DATA_11	U16			
	DDR_DATA_12	U14			
	DDR_DATA_13	U13			
	DDR_DATA_14	T13			
	DDR_DATA_15	R13			
	DDR_DQS_1	U15	I/O	Upper Data Strobe	Differential SSTL_2/SSTL_18
	DDR_nDQS_1	T15			
	DDR_DM_1	T14	I/O	Upper Data Mask	SSTL_2/SSTL_18
	DDR_GATE_1	R14		Upper Gate Open	
	DDR_VREF	P10	Input	Reference Voltage	Analog
	DDR_MEM_COMP_GND	R4	Power	Return for Ext. Resistors	Power
	DDR_MEM_COMP_REXT	P4	Power	Ext. Resistor	Analog
	DDR2_EN	J13	Input	Configuration	TTL Input Buffer 3.3 V Tolerant, PU

3.3 Shared I/O pins (PL_GPIOs)

SPEAr300 devices feature, in the Reconfigurable Array Subsystem (RAS), specific sets of IPs as well as groups of software controllable GPIOs (that can be used alternatively). In the SPEAr300 the following IPs are implemented in the RAS:

- FSMC NAND/NOR Flash interface
- GPIO/Keyboard controller
- 8-bit camera interface
- CLCD controller interface
- Digital-to-analog converter (DAC)
- I2S
- 4 SPI/I2C control signals
- TDM block
- SDIO interface
- GPIOs

The 98 PL_GPIO and 4 PL_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

The PL_GPIOs can be configured in 13 different modes. This allows SPEAr300 to be tailored for use in various applications, see *Section 3.3.2*.

3.3.1 PL_GPIO pin description

Table 9. PL_GPIO pin description

Group	Signal name	Ball	Direction	Function	Pin type
PL_GPIOs	PL_GPIO_97... PL_GPIO_0	(see *Table 11*)	I/O	General purpose I/O or multiplexed pins (see *Table 11*)	(see the introduction of the *Section 3.3* above)
	PL_CLK1... PL_CLK4			Programmable logic external clocks	

3.3.2 Configuration modes

This section describes the main operating modes created by using a selection of the embedded IPs.

13 configurations are available selected by RAS register 2. The peripherals available in each configuration are shown in *Table 10: Available peripherals in each configuration mode* Details of each PL_GPIO pin are given for each mode in *Table 11: PL_GPIO multiplexing scheme*.

Table 10. Available peripherals in each configuration mode

Modes	FSMC	Boot pins	SPI/I2C Multi slave control	I2S	CLCD	DAC	Camera interface	TDM No of voice devices	SDIO/MMC data lines	Keyboard keys	GPIOs					
											Max. no. of I/Os	Bidirectional	Input only	Output only	Special outputs (sync)	Max. no. of I/Os with Interrupt
1	16-bit NAND	4									18	6	12			6
2	16-bit NOR	4									18	6	12			6
3	16-bit NAND				1			1	8		28	28				22
4			8	1		1		8	8	9*9	62	38	8	12	4	14
5			4	1	1	1		2	8	9*9	42	38		4		14
6			8	1		1		8	8	9*9	58	38	8	8	4	14
7			4	1	1	1		2	8	9*9	42	38		4		14
8	8-bit NOR		8					8	4		44	24	8	8	4	14
9	8-bit NAND /NOR		8	1		1		4	4		42	24	8	8	2	14
10			4	1		1	8-bit	2	8	9*9	36	32		4		10
11				1	1	1	14-bit	2	8	7*5	26	26				10
12				1		1	14-bit	2	8	7*5	26	26				10
13			4	1	1	1	8-bit	2	8	9*9	32	28		4		6

TDM interfacing using GPIOs

In some configuration modes where less than 8 TDM devices are indicated in *Table 10*, additional TDM devices can be supported by using GPIO pins. The TDM needs a dedicated interrupt line, an SPI and an independent frame sync signal to interface each device. When enough SPI chip selects signals are not available (SPI_I2C signals), the chip select can be performed by a GPIO. In this case the number of possible TDM devices supported is:

Modes 5, 7, 8 and 9: up to 8 devices

Modes 3 and 10: up to 6 devices

Modes 11 and 12: up to 4 devices

Table 11. PL_GPIO multiplexing scheme (continued)

PL_GPIO_# / ball number	Configuration mode (enabled by RAS register 2)													Alternate function (enabled by RAS register 1)
	1	2	3	4	5	6	7	8	9	10	11	12	13	
PL_GPIO_51/D10	0	0	CLLP	G10_6	CLLP	G10_6	CLLP	G10_6	G10_6	G10_6	CLLP	G10_6	CLLP	
PL_GPIO_50/A12	0	0	CLLE	G10_5	CLLE	G10_5	CLLE	G10_5	G10_5	G10_5	CLLE	G10_5	CLLE	TMR_CPTR4
PL_GPIO_49/C11	0	0	CLPP	G10_4	CLPP	G10_4	CLPP	G10_4	G10_4	G10_4	CLPP	G10_4	CLPP	TMR_CPTR3
PL_GPIO_48/B11	B0	B0	CLD22	SPI_I2C0	SPI_I2C0	SPI_I2C0	SPI_I2C0	SPI_I2C0	SPI_I2C0	SPI_I2C0	DIO4_1	DIO4_1	SPI_I2C0	TMR_CPTR2
PL_GPIO_47/C10	B1	B1	CLD23	SPI_I2C1	SPI_I2C1	SPI_I2C1	SPI_I2C1	SPI_I2C1	SPI_I2C1	SPI_I2C1	DIO5_1	DIO5_1	SPI_I2C1	TMR_CPTR1
PL_GPIO_46/A11	B2	B2	GPIO7	SPI_I2C2	SPI_I2C2	SPI_I2C2	SPI_I2C2	SPI_I2C2	SPI_I2C2	SPI_I2C2	DIO6_1	DIO6_1	SPI_I2C2	TMR_CLK4
PL_GPIO_45/B10	B3	B3	GPIO6	SPI_I2C3	SPI_I2C3	SPI_I2C3	SPI_I2C3	SPI_I2C3	SPI_I2C3	SPI_I2C3	DIO7_1	DIO7_1	SPI_I2C3	TMR_CLK3
PL_GPIO_44/A10	H0	H0	GPIO5	G10_3/ DAC_O0	G10_3/ DAC_O0	G10_3/ DAC_O0	G10_3/ DAC_O0	G10_3	DAC_O0	DAC_O0	DAC_O0	DAC_O0	DAC_O0	TMR_CLK2
PL_GPIO_43/E9	H1	H1	GPIO4	G10_2/ DAC_O1	G10_2/ DAC_O1	G10_2/ DAC_O1	G10_2/ DAC_O1	G10_2	DAC_O1	DAC_O1	DAC_O1	DAC_O1	DAC_O1	TMR_CLK1
PL_GPIO_42/D9	H2	H2	GPIO3	I2S_DIN	I2S_DIN	I2S_DIN	I2S_DIN	G10_1	I2S_DIN	I2S_DIN	I2S_DIN	I2S_DIN	I2S_DIN	UART_DTR
PL_GPIO_41/C9	H3	H3	GPIO2	I2S_ LRCK	I2S_ LRCK	I2S_ LRCK	I2S_ LRCK	G10_0	I2S_LRCK	I2S_LRCK	I2S_LRCK	I2S_LRCK	I2S_LRCK	UART_RI
PL_GPIO_40/B9	H4	H4	GPIO1	I2S_CLK	I2S_CLK	I2S_CLK	I2S_CLK	TDM_SYNC3	I2S_CLK	I2S_CLK	I2S_CLK	I2S_CLK	I2S_CLK	UART_DSR
PL_GPIO_39/A9	H5	H5	GPIO0	I2S_ DOUT	I2S_ DOUT	I2S_ DOUT	I2S_ DOUT	TDM_SYNC2	DOUT	I2S_DOUT	I2S_DOUT	I2S_DOUT	I2S_DOUT	UART_DCD
PL_GPIO_38/A8	H6	H6	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	TDM_ SYNC1	UART_CTS
PL_GPIO_37/B8	H7	H7	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	TDM_ DOUT	UART_RTS
PL_GPIO_36/C8	0	0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	TDM_ SYNC0	SSP_CS4
PL_GPIO_35/D8	Reserved	Reserved	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	SSP_CS3
PL_GPIO_34/E8	0	0	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	SSP_CS2
PL_GPIO_33/E7	0	0	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	BasGPIO5
PL_GPIO_32/D7	0	0	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	BasGPIO4
PL_GPIO_31/C7	0	0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	SD_DAT0	BasGPIO3

Table 13. Ball sharing during debug

Signal	Case 1 - Board Debug	Case 2 - Static Debug	Case 3 - Full Debug
Test[0]	0	1	0
Test[1]	0	0	1
Test[2]	0	0/1	0/1
Test[3]	0	0/1	0/1
Test[4]	1	0	0
nTRST	nTRST_bscan	nTRST_ARM	nTRST_ARM
TCK	TCK_bscan	TCK_ARM	TCK_ARM
TMS	TSM_bscan	TMS_ARM	TSM_ARM
TDI	TDI_bscan	TDI_ARM	TDI_ARM
TDO	TDO_bscan	TDO_ARM	TDO_ARM
PL_GPIO[97]	BSR Value	Functional I/O	ARM_TRACE_CLK
PL_GPIO[96]	BSR Value	Functional I/O	ARM_TRACE_PKTA[0]
PL_GPIO[95]	BSR Value	Functional I/O	ARM_TRACE_PKTA[1]
PL_GPIO[94]	BSR Value	Functional I/O	ARM_TRACE_PKTA[2]
PL_GPIO[93]	BSR Value	Functional I/O	ARM_TRACE_PKTA[3]
PL_GPIO[92]	BSR Value	Functional I/O	ARM_TRACE_PKTB[0]
PL_GPIO[91]	BSR Value	Functional I/O	ARM_TRACE_PKTB[1]
PL_GPIO[90]	BSR Value	Functional I/O	ARM_TRACE_PKTB[2]
PL_GPIO[89]	BSR Value	Functional I/O	ARM_TRACE_PKTB[3]
PL_GPIO[88]	BSR Value	Functional I/O	ARM_TRACE_SYNCA
PL_GPIO[87]	BSR Value	Functional I/O	ARM_TRACE_SYNCB
PL_GPIO[86]	BSR Value	Functional I/O	ARM_PIPESTATA[0]
PL_GPIO[85]	BSR Value	Functional I/O	ARM_PIPESTATA[1]
PL_GPIO[84]	BSR Value	Functional I/O	ARM_PIPESTATA[2]
PL_GPIO[83]	BSR Value	Functional I/O	ARM_PIPESTATB[0]
PL_GPIO[82]	BSR Value	Functional I/O	ARM_PIPESTATB[1]
PL_GPIO[81]	BSR Value	Functional I/O	ARM_PIPESTATB[2]
PL_GPIO[80]	BSR Value	Functional I/O	ARM_TRACE_PKTA[4]
PL_GPIO[79]	BSR Value	Functional I/O	ARM_TRACE_PKTA[5]
PL_GPIO[78]	BSR Value	Functional I/O	ARM_TRACE_PKTA[6]
PL_GPIO[77]	BSR Value	Functional I/O	ARM_TRACE_PKTA[7]
PL_GPIO[76]	BSR Value	Functional I/O	ARM_TRACE_PKTB[4]
PL_GPIO[75]	BSR Value	Functional I/O	ARM_TRACE_PKTB[5]
PL_GPIO[74]	BSR Value	Functional I/O	ARM_TRACE_PKTB[6]

Table 14. Memory mapping (continued)

Start address	End address	Peripheral	Description
0xD280.0000	0xD2FF.FFFF	SRAM	Static RAM shared memory (57 Kbytes)
0xD300.0000	0xE07F.FFFF	-	Reserved
0xE0800.0000	0xE0FF.FFFF	Ethernet controller	MAC
0xE100.0000	0xE10F.FFFF	USB 2.0 device	FIFO
0xE110.0000	0xE11F.FFFF	USB 2.0 device	Configuration registers
0xE120.0000	0xE12F.FFFF	USB 2.0 device	Plug detect
0xE130.0000	0xE17F.FFFF	-	Reserved
0xE180.0000	0xE18F.FFFF	USB2.0 EHCI 0-1	
0xE190.0000	0xE19F.FFFF	USB2.0 OHCI 0	
0xE1A0.0000	0xE20F.FFFF	-	Reserved
0xE210.0000	0xE21F.FFFF	USB2.0 OHCI 1	
0xE220.0000	0xE27F.FFFF	-	Reserved
0xE280.0000	0xE28F.FFFF	ML USB ARB	Configuration register
0xE290.0000	0xE7FF.FFFF	-	Reserved
0xE800.0000	0xEFFF.FFFF	-	Reserved
0xF000.0000	0xF00F.FFFF	Timer	
0xF010.0000	0xF10F.FFFF	-	Reserved
0xF110.0000	0xF11F.FFFF	VIC	
0xF120.0000	0xF7FF.FFFF	-	Reserved
0xF800.0000	0xFBFF.FFFF	Serial Flash memory	
0xFC00.0000	0xFC1F.FFFF	Serial Flash controller	
0xFC20.0000	0xFC3F.FFFF	-	Reserved
0xFC40.0000	0xFC5F.FFFF	DMA controller	
0xFC60.0000	0xFC7F.FFFF	DRAM controller	
0xFC80.0000	0xFC87.FFFF	Timer 1	
0xFC88.0000	0xFC8F.FFFF	Watchdog timer	
0xFC90.0000	0xFC97.FFFF	Real-time clock	
0xFC98.0000	0xFC9F.FFFF	General purpose I/O	
0xFCA0.0000	0xFCA7.FFFF	System controller	
0xFCA8.0000	0xFCAF.FFFF	Miscellaneous registers	
0xFCB0.0000	0xFCB7.FFFF	Timer 2	
0xFCB8.0000	0xFCFF.FFFF	-	Reserved
0xFD00.0000	0xFEFF.FFFF	-	Reserved
0xFF00.0000	0xFFFF.FFFF	Internal ROM	Boot

5 Electrical characteristics

5.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high/low static voltages. However it is advisable to take normal precaution to avoid application of any voltage higher/lower than the specified maximum/minimum rated voltages.

The absolute maximum rating is the maximum stress that can be applied to a device without causing permanent damage. However, extended exposure to minimum/maximum ratings may affect long-term device reliability.

Table 15. Absolute maximum ratings

Symbol	Parameter	Minimum value	Maximum value	Unit
V_{DD} 1.2	Supply voltage for the core	- 0.3	1.44	V
V_{DD} 3.3	Supply voltage for the I/Os	- 0.3	3.9	V
V_{DD} 2.5	Supply voltage for the analog blocks	- 0.3	3	V
V_{DD} 1.8	Supply voltage for the DRAM interface	- 0.3	2.16	V
V_{DD} RTC	RTC supply voltage	-0.3	2.16	V
T_{STG}	Storage temperature	-55	150	°C
T_J	Junction temperature	-40	125	°C

5.2 Maximum power consumption

Note: These values take into consideration the worst cases of process variation and voltage range and must be used to design the power supply section of the board.

Table 16. Maximum power consumption

Symbol	Description	Max	Unit
V_{DD} 1.2	Supply voltage for the core	420	mA
V_{DD} 1.8	Supply voltage for the DRAM interface (1)	160	mA
V_{DD} RTC	RTC supply voltage	8	µA
V_{DD} 2.5	Supply voltage for the analog blocks	35	mA
V_{DD} 3.3	Supply voltage for the I/Os (2)	15	mA
P_D	Maximum power consumption	930(3)	mW

1. Peak current with Linux memory test (50% write and 50% read) plus DMA reading memory.
2. With 30 logic channels connected to the device and simultaneously switching at 10 MHz.

5.5 3.3V I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b

Table 19. Low voltage TTL DC input specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low level input voltage		0.8	V
V_{IH}	High level input voltage	2		V
V_{hyst}	Schmitt trigger hysteresis	300	800	mV

Table 20. Low voltage TTL DC output specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Test condition	Min	Max	Unit
V_{OL}	Low level output voltage	I_{OL}= X mA (1)		0.3	V
V_{OH}	High level output voltage	I_{OH}= -X mA (1)	V_{DD} - 0.3		V

1. For the max current value (X mA) refer to *Section 2.29: 8-channel ADC*.

Table 21. Pull-up and pull-down characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_I = 0 V	29	67	kΩ
R_{PD}	Equivalent pull-down resistance	V_I = V_{DDE}3V3	29	103	kΩ

5.6 LPDDR and DDR2 pin characteristics

Table 22. DC characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
V_{IL}	Low level input voltage	SSTL2	-0.3	V_{REF}-0.15	V
		SSTL18	-0.3	V_{REF}-0.125	V
V_{IH}	High level input voltage	SSTL2	V_{REF}+0.15	V_{DDE}2V5+0.3	V
		SSTL18	V_{REF}+0.125	V_{DDE}1V8+0.3	V
V_{hyst}	Input voltage hysteresis		200		mV

Table 23. Driver characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_O	Output impedance (strong value)	40.5	45	49.5	Ω
	Output impedance (weak value)	44.1	49	53.9	Ω

6.2.2 CLCD timing characteristics divided clock

Figure 15. CLCD waveform with CLCP divided

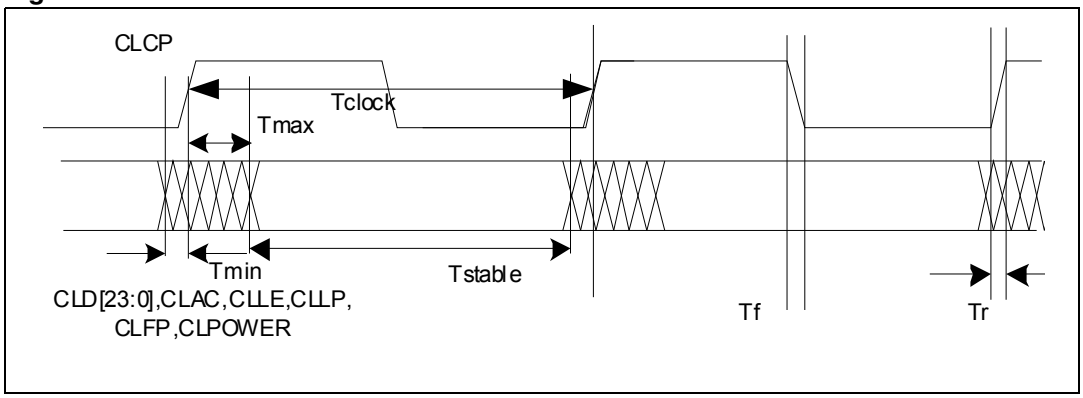


Figure 16. CLCD block diagram with CLCP divided

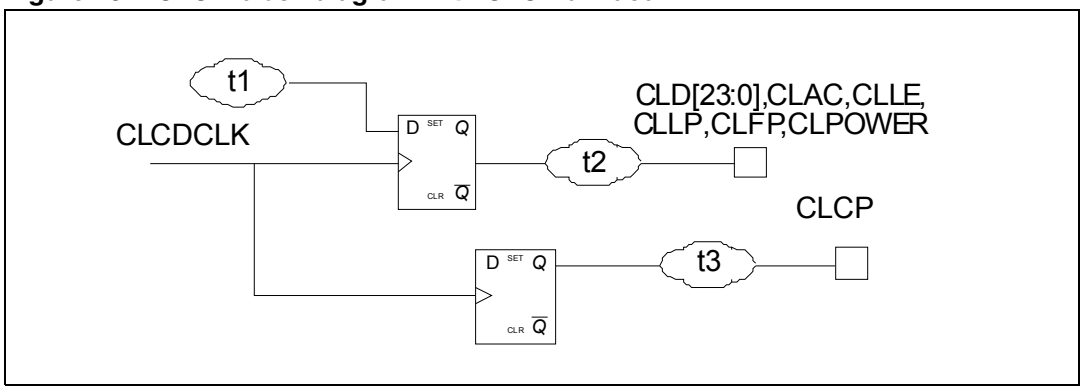


Table 30. CLCD timings with CLCP divided

Parameter	Value	Frequency
t_{CLOCK} divided max	12 ns	83.3 MHz
t_{CLOCK} divided max rise (t_r)	0.81 ns	
t_{CLOCK} divided max (t_f)	0.87 ns	
t_{min}	-0.49 ns	
t_{max}	2.38 ns	
t_{STABLE}	9.13 ns	

Note: 1 $t_{STABLE} = t_{CLOCK}$ direct max - (tmax + tmin)

2 For t_{max} the maximum value is taken from the worst case and for t_{min} the minimum value is taken from the best case.

3 CLCP should be delayed by {t_{max} + [t_{CLOCK} direct max - (t_{max} + t_{min})]/2} = 6.945 ns

6.3 I²C timing characteristics

The characterization timing is done considering an output load of 10 pF on SCL and SDA. The operating conditions are V = 0.90 V, T_A=125° C in worst case and V =1.10 V, T_A= 40° C in best case.

Figure 17. I²C output pins

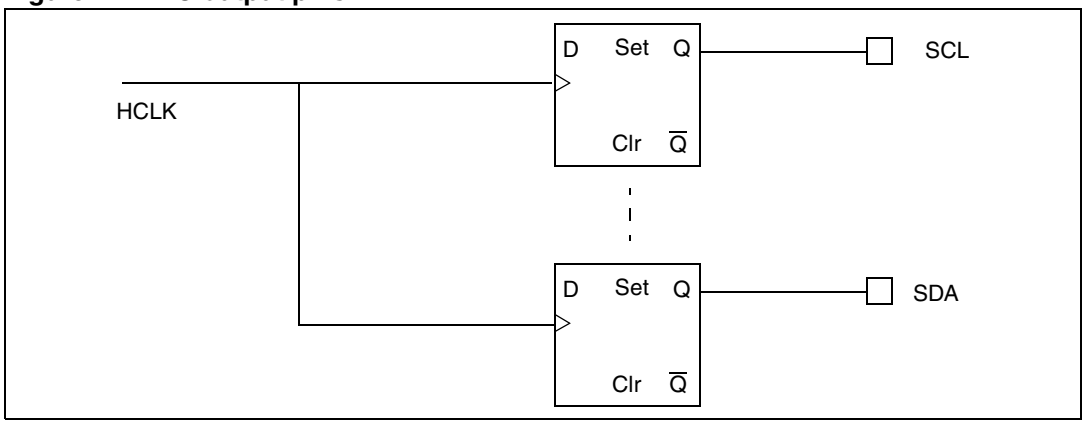
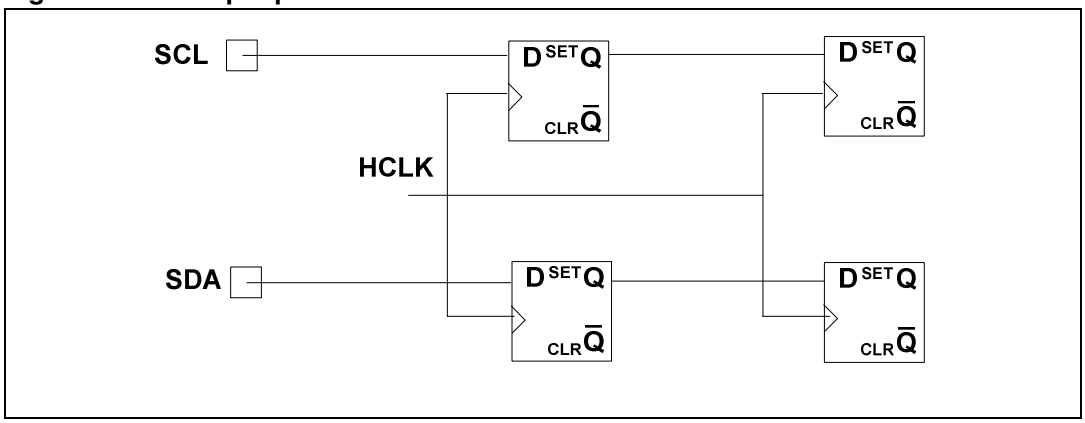


Figure 18. I²C input pins



The flip-flops used to capture the incoming signals are re-synchronized with the AHB clock (HCLK): so, no input delay calculation is required.

Table 31. Output delays for I²C signals

Parameter	Min	Max	Unit
$t_{HCLK->SCLH}$	8.1067	11.8184	ns
$t_{HCLK->SCLL}$	7.9874	12.6269	ns
$t_{HCLK->SDAH}$	7.5274	11.2453	ns
$t_{HCLK->SDAL}$	7.4081	12.0530	ns

Those values are referred to the common internal source clock which has a period of:

t_{HCLK} = 6 ns.

6.4.1 8-bit NAND Flash configuration

Figure 21. Output pads for 8-bit NAND Flash configuration

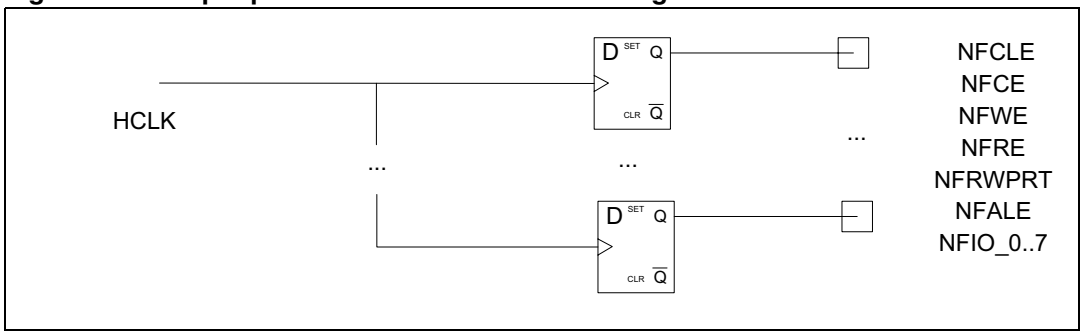


Figure 22. Input pads for 8-bit NAND Flash configuration

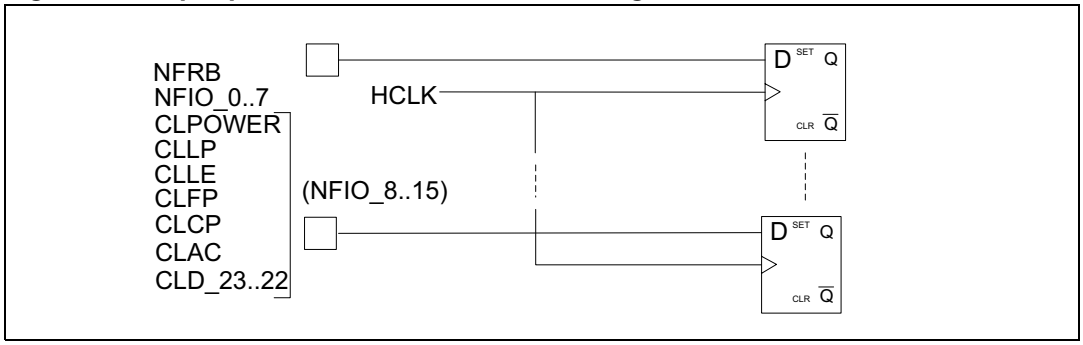


Figure 23. Output command signal waveforms for 8-bit NAND Flash configuration

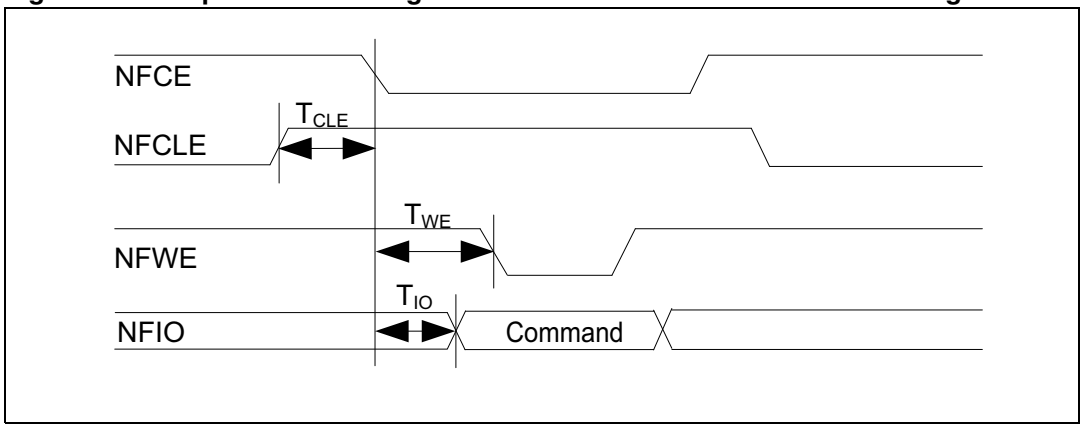


Table 49. UART transmit timing characteristics

S.No.	Parameters	Min	Max	Unit
1	UART Maximum Baud Rate		3	Mbps
2	UART Pulse Duration Transmit Data (TxD)	$0.99B_{(1)}$	$B_{(1)}$	ns
3	UART Transmit Start Bit	$0.99B_{(1)}$	$B_{(1)}$	ns

Table 50. UART receive timing characteristics

S.No.	Parameters	Min	Max	Units
4	UART Pulse Duration Receive Data (RxD)	$0.97B_{(1)}$	$1.06B_{(1)}$	ns
5	UART Receive Start Bit	$0.97B_{(1)}$	$1.06B_{(1)}$	ns

where (1) B = UART baud rate

8 Revision history

Table 53. Document revision history

Date	Revision	Changes
15-Oct-2009	1	Initial release.
29-Apr-2010	2	Changed the order of chapters in *Section 2: Architecture overview* Updated *Section 3.3: Shared I/O pins (PL_GPIOs) on page 35* Updated number of GPIOs in *Table 10 on page 41* Updated *Table 11: PL_GPIO multiplexing scheme on page 42* Added *Section 3.4: PL_GPIO pin sharing for debug modes on page 47* Updated *Section 5: Electrical characteristics*, *Section 6.1: DDR2 timing characteristics*, *Section 6.3: I^2C timing characteristics*, *Section 6.4: FSMC timing characteristics* and *Section 6.7: SSP timing characteristics* Added *Table 52: Thermal resistance characteristics* in Package information.