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Details

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Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	1.5K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08dz48amlh

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Section Number

Title

Page

	8.1.2	Modes of Operation	139
8.2	Externa	l Signal Description	139
8.3	Register	r Definition	140
	8.3.1	MCG Control Register 1 (MCGC1)	140
	8.3.2	MCG Control Register 2 (MCGC2)	141
	8.3.3	MCG Trim Register (MCGTRM)	142
	8.3.4	MCG Status and Control Register (MCGSC)	143
	8.3.5	MCG Control Register 3 (MCGC3)	144
8.4	Functio	nal Description	146
	8.4.1	Operational Modes	146
	8.4.2	Mode Switching	150
	8.4.3	Bus Frequency Divider	151
	8.4.4	Low Power Bit Usage	151
	8.4.5	Internal Reference Clock	151
	8.4.6	External Reference Clock	151
	8.4.7	Fixed Frequency Clock	152
8.5	Initializ	ation / Application Information	152
	8.5.1	MCG Module Initialization Sequence	152
	8.5.2	MCG Mode Switching	153
	8.5.3	Calibrating the Internal Reference Clock (IRC)	164

Chapter 9 Analog Comparator (S08ACMPV3)

9.1	Introduc	ction	167
	9.1.1	ACMP Configuration Information	167
	9.1.2	Features	169
	9.1.3	Modes of Operation	169
	9.1.4	Block Diagram	170
9.2	Externa	l Signal Description	170
9.3	Memory	/ Map/Register Definition	171
	9.3.1	ACMPx Status and Control Register (ACMPxSC)	171
9.4	Function	nal Description	172

Chapter 10 Analog-to-Digital Converter (S08ADC12V1)

10.1	Introduction	173
	10.1.1 Analog Power and Ground Signal Names	
	10.1.2 Channel Assignments	173
	10.1.3 Alternate Clock	174
	10.1.4 Hardware Trigger	174
	10.1.5 Temperature Sensor	175
	10.1.6 Features	177

MC9S08DZ60 Series Data Sheet, Rev. 4



Chapter 1 Device Overview



Figure 1-2. MC9S08DZ60 System Clock Distribution Diagram





 V_{REFH} and V_{REFL} are internally connected to V_{DDA} and V_{SSA} , respectively.

Figure 2-3. 32-Pin LQFP



Chapter 4 Memory

Table 4-3. High-Page Register Summary (Sheet 2 of 3)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x1847	Reserved	—	_	—	—	—	—	—	—
0x1848	PTBPE	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
0x1849	PTBSE	PTBSE7	PTBSE6	PTBSE5	PTBSE4	PTBSE3	PTBSE2	PTBSE1	PTBSE0
0x184A	PTBDS	PTBDS7	PTBDS6	PTBDS5	PTBDS4	PTBDS3	PTBDS2	PTBDS1	PTBDS0
0x184B	Reserved	_						_	
0x184C	PTBSC	0	0	0	0	PTBIF	PTBACK	PTBIE	PTBMOD
0x184D	PTBPS	PTBPS7	PTBPS6	PTBPS5	PTBPS4	PTBPS3	PTBPS2	PTBPS1	PTBPS0
0x184E	PTBES	PTBES7	PTBES6	PTBES5	PTBES4	PTBES3	PTBES2	PTBES1	PTBES0
0x184F	Reserved	_			—	_	_	_	—
0x1850	PTCPE	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
0x1851	PTCSE	PTCSE7	PTCSE6	PTCSE5	PTCSE4	PTCSE3	PTCSE2	PTCSE1	PTCSE0
0x1852	PTCDS	PTCDS7	PTCDS6	PTCDS5	PTCDS4	PTCDS3	PTCDS2	PTCDS1	PTCDS0
0x1853– 0x1857	Reserved								
0x1858	PTDPE	PTDPE7	PTDPE6	PTDPE5	PTDPE4	PTDPE3	PTDPE2	PTDPE1	PTDPE0
0x1859	PTDSE	PTDSE7	PTDSE6	PTDSE5	PTDSE4	PTDSE3	PTDSE2	PTDSE1	PTDSE0
0x185A	PTDDS	PTDDS7	PTDDS6	PTDDS5	PTDDS4	PTDDS3	PTDDS2	PTDDS1	PTDDS0
0x185B	Reserved					_	_	_	_
0x185C	PTDSC	0	0	0	0	PTDIF	PTDACK	PTDIE	PTDMOD
0x185D	PTDPS	PTDPS7	PTDPS6	PTDPS5	PTDPS4	PTDPS3	PTDPS2	PTDPS1	PTDPS0
0x185E	PTDES	PTDES7	PTDES6	PTDES5	PTDES4	PTDES3	PTDES2	PTDES1	PTDES0
0x185F	Reserved		—	_	—				—
0x1860	PTEPE	PTEPE7	PTEPE6	PTEPE5	PTEPE4	PTEPE3	PTEPE2	PTEPE1	PTEPE0
0x1861	PTESE	PTESE7	PTESE6	PTESE5	PTESE4	PTESE3	PTESE2	PTESE1	PTESE0
0x1862	PTEDS	PTEDS7	PTEDS6	PTEDS5	PTEDS4	PTEDS3	PTEDS2	PTEDS1	PTEDS0
0x1863– 0x1867	Reserved	_	_	_	_	_	_	_	_
0x1868	PTFPE	PTFPE7	PTFPE6	PTFPE5	PTFPE4	PTFPE3	PTFPE2	PTFPE1	PTFPE0
0x1869	PTFSE	PTFSE7	PTFSE6	PTFSE5	PTFSE4	PTFSE3	PTFSE2	PTFSE1	PTFSE0
0x186A	PTFDS	PTFDS7	PTFDS6	PTFDS5	PTFDS4	PTFDS3	PTFDS2	PTFDS1	PTFDS0
0x186B– 0x186F	Reserved								
0x1870	PTGPE	0	0	PTGPE5	PTGPE4	PTGPE3	PTGPE2	PTGPE1	PTGPE0
0x1871	PTGSE	0	0	PTGSE5	PTGSE4	PTGSE3	PTGSE2	PTGSE1	PTGSE0
0x1872	PTGDS	0	0	PTGDS5	PTGDS4	PTGDS3	PTGDS2	PTGDS1	PTGDS0
0x1873– 0x187F	Reserved							_	_
0x1880	CANCTL0	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
0x1881	CANCTL1	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
0x1882	CANBTR0	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0

MC9S08DZ60 Series Data Sheet, Rev. 4



4.5.10 EEPROM Mapping

Only half of the EEPROM is in the memory map. The EPGSEL bit in FCNFG register selects which half of the array can be accessed in foreground while the other half can not be accessed in background. There are two mapping mode options that can be selected to configure the 8-byte EEPROM sectors: 4-byte mode and 8-byte mode. Each mode is selected by the EPGMOD bit in the FOPT register.

In 4-byte sector mode (EPGMOD = 0), each 8-byte sector splits four bytes on foreground and four bytes on background but on the same addresses. The EPGSEL bit selects which four bytes can be accessed. During a sector erase, the entire 8-byte sector (four bytes in foreground and four bytes in background) is erased.

In 8-byte sector mode (EPGMOD = 1), each entire 8-byte sector is in a single page. The EPGSEL bit selects which sectors are on background. During a sector erase, the entire 8-byte sector in foreground is erased.

4.5.11 Flash and EEPROM Registers and Control Bits

The Flash and EEPROM modules have seven 8-bit registers in the high-page register space and three locations in the nonvolatile register space in Flash memory. Two of those locations are copied into two corresponding high-page control registers at reset. There is also an 8-byte comparison key in Flash memory. Refer to Table 4-3 and Table 4-5 for the absolute address assignments for all Flash and EEPROM registers. This section refers to registers and control bits only by their names. A Freescale Semiconductor-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

4.5.11.1 Flash and EEPROM Clock Divider Register (FCDIV)

Bit 7 of this register is a read-only flag. Bits 6:0 may be read at any time but can be written only one time. Before any erase or programming operations are possible, write to this register to set the frequency of the clock for the nonvolatile memory system within acceptable limits.







Table 5-3. SRS Register Field Descriptions

Field	Description
2 LOC	 Loss of Clock — Reset was caused by a loss of external clock. 0 Reset not caused by loss of external clock 1 Reset caused by loss of external clock
1 LVD	 Low-Voltage Detect — If the LVDRE bit is set and the supply drops below the LVD trip voltage, an LVD reset will occur. This bit is also set by POR. 0 Reset not caused by LVD trip or POR. 1 Reset caused by LVD trip or POR.

5.8.3 System Background Debug Force Reset Register (SBDFR)

This high page register contains a single write-only control bit. A serial background command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.



¹ BDFR is writable only through serial background debug commands, not from user programs.

Figure 5-4. System Background Debug Force Reset Register (SBDFR)

Table 5-4. SBDFR Register Field Descriptions

Field	Description
0 BDFR	Background Debug Force Reset — A serial background command such as WRITE_BYTE can be used to allow an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.



Chapter 6 Parallel Input/Output Control

6.5.1.5 Port A Drive Strength Selection Register (PTADS)



Figure 6-7. Drive Strength Selection for Port A Register (PTADS)

Table 6-5. PTADS Register Field Descriptions

Field	Description
7:0 PTADS[7:0]	 Output Drive Strength Selection for Port A Bits — Each of these control bits selects between low and high output drive for the associated PTA pin. For port A pins that are configured as inputs, these bits have no effect. 0 Low output drive strength selected for port A bit n. 1 High output drive strength selected for port A bit n.

6.5.1.6 Port A Interrupt Status and Control Register (PTASC)



Figure 6-8. Port A Interrupt Status and Control Register (PTASC)

Table 6-6. PTASC Register Field Descriptions

Field	Description
3 PTAIF	 Port A Interrupt Flag — PTAIF indicates when a port A interrupt is detected. Writes have no effect on PTAIF. 0 No port A interrupt detected. 1 Port A interrupt detected.
2 PTAACK	Port A Interrupt Acknowledge — Writing a 1 to PTAACK is part of the flag clearing mechanism. PTAACK always reads as 0.
1 PTAIE	 Port A Interrupt Enable — PTAIE determines whether a port A interrupt is requested. 0 Port A interrupt request not enabled. 1 Port A interrupt request enabled.
0 PTAMOD	 Port A Detection Mode — PTAMOD (along with the PTAES bits) controls the detection mode of the port A interrupt pins. 0 Port A pins detect edges only. 1 Port A pins detect both edges and levels.



Chapter 8 Multi-Purpose Clock Generator (S08MCGV1)

- 4. Lastly, FBI transitions into BLPI mode.
 - a) MCGC2 = 0x08 (%00001000)
 - LP (bit 3) in MCGSC is 1



Figure 8-10. Flowchart of PEE to BLPI Mode Transition using a 4 MHz crystal

MC9S08DZ60 Series Data Sheet, Rev. 4



Chapter 8 Multi-Purpose Clock Generator (S08MCGV1)



Figure 8-13. Trim Procedure

In this particular case, the MCU has been attached to a PCB and the entire assembly is undergoing final test with automated test equipment. A separate signal or message is provided to the MCU operating under user provided software control. The MCU initiates a trim procedure as outlined in Figure 8-13 while the tester supplies a precision reference signal.

If the intended bus frequency is near the maximum allowed for the device, it is recommended to trim using a reference divider value (RDIV setting) of twice the final value. After the trim procedure is complete, the reference divider can be restored. This will prevent accidental overshoot of the maximum clock frequency.



Chapter 9 Analog Comparator (S08ACMPV3)

9.1.4 Block Diagram

The block diagram for the analog comparator module is shown Figure 9-2.



Figure 9-2. Analog Comparator (ACMP) Block Diagram

9.2 External Signal Description

The ACMP has two analog input pins, ACMPx+ and ACMPx– and one digital output pin ACMPxO. Each of these pins can accept an input voltage that varies across the full operating voltage range of the MCU. As shown in Figure 9-2, the ACMPx- pin is connected to the inverting input of the comparator, and the ACMPx+ pin is connected to the comparator non-inverting input if ACBGS is a 0. As shown in Figure 9-2, the ACMPxO pin can be enabled to drive an external pin.

The signal properties of ACMP are shown in Table 9-1.

Signal	Function	I/O
ACMPx-	Inverting analog input to the ACMP. (Minus input)	I
ACMPx+	Non-inverting analog input to the ACMP. (Positive input)	I
ACMPxO	Digital output of the ACMP.	0

Table 9-1. Signal Properties



Chapter 10 Analog-to-Digital Converter (S08ADC12V1)

For 12-bit conversions the code transitions only after the full code width is present, so the quantization error is -1 lsb to 0 lsb and the code width of each step is 1 lsb.

10.6.2.5 Linearity Errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors but the system should be aware of them because they affect overall accuracy. These errors are:

- Zero-scale error (E_{ZS}) (sometimes called offset) This error is defined as the difference between the actual code width of the first conversion and the ideal code width (1/2 lsb in 8-bit or 10-bit modes and 1 lsb in 12-bit mode). If the first conversion is 0x001, the difference between the actual 0x001 code width and its ideal (1 lsb) is used.
- Full-scale error (E_{FS}) This error is defined as the difference between the actual code width of the last conversion and the ideal code width (1.5 lsb in 8-bit or 10-bit modes and 1LSB in 12-bit mode). If the last conversion is 0x3FE, the difference between the actual 0x3FE code width and its ideal (1LSB) is used.
- Differential non-linearity (DNL) This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.
- Integral non-linearity (INL) This error is defined as the highest-value the (absolute value of the) running sum of DNL achieves. More simply, this is the worst-case difference of the actual transition voltage to a given code and its corresponding ideal transition voltage, for all codes.
- Total unadjusted error (TUE) This error is defined as the difference between the actual transfer function and the ideal straight-line transfer function and includes all forms of error.

10.6.2.6 Code Jitter, Non-Monotonicity, and Missing Codes

Analog-to-digital converters are susceptible to three special forms of error. These are code jitter, non-monotonicity, and missing codes.

Code jitter is when, at certain points, a given input voltage converts to one of two values when sampled repeatedly. Ideally, when the input voltage is infinitesimally smaller than the transition voltage, the converter yields the lower code (and vice-versa). However, even small amounts of system noise can cause the converter to be indeterminate (between two codes) for a range of input voltages around the transition voltage. This range is normally around 1/2lsb in 8-bit or 10-bit mode, or around 2 lsb in 12-bit mode, and increases with noise.

This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Section 10.6.2.3 reduces this error.

Non-monotonicity is defined as when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and have no missing codes.



Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except bits IDHITx, which are read-only

Table 12-16. CANIDAC Register Field Descriptions

Field	Description
5:4 IDAM[1:0]	Identifier Acceptance Mode — The CPU sets these flags to define the identifier acceptance filter organization (see Section 12.5.3, "Identifier Acceptance Filter"). Table 12-17 summarizes the different settings. In filter closed mode, no message is accepted such that the foreground buffer is never reloaded.
2:0 IDHIT[2:0]	Identifier Acceptance Hit Indicator — The MSCAN sets these flags to indicate an identifier acceptance hit (see Section 12.5.3, "Identifier Acceptance Filter"). Table 12-18 summarizes the different settings.

Table 12-17. Identifier Acceptance Mode Settings

IDAM1	IDAM0	Identifier Acceptance Mode
0	0	Two 32-bit acceptance filters
0	1	Four 16-bit acceptance filters
1	0	Eight 8-bit acceptance filters
1	1	Filter closed

IDHIT2	IDHIT1	IDHIT0	Identifier Acceptance Hit			
0	0	0	Filter 0 hit			
0	0	1	Filter 1 hit			
0	1	0	Filter 2 hit			
0	1	1	Filter 3 hit			
1	0	0	Filter 4 hit			
1	0	1	Filter 5 hit			
1	1	0	Filter 6 hit			
1	1	1	Filter 7 hit			

 Table 12-18. Identifier Acceptance Hit Indication

The IDHITx indicators are always related to the message in the foreground buffer (RxFG). When a message gets shifted into the foreground buffer of the receiver FIFO the indicators are updated as well.

12.3.12 MSCAN Miscellaneous Register (CANMISC)

This register provides additional features.



12.6.2 Bus-Off Recovery

The bus-off recovery is user configurable. The bus-off state can either be exited automatically or on user request.

For reasons of backwards compatibility, the MSCAN defaults to automatic recovery after reset. In this case, the MSCAN will become error active again after counting 128 occurrences of 11 consecutive recessive bits on the CAN bus (See the Bosch CAN specification for details).

If the MSCAN is configured for user request (BORM set in Section 12.3.2, "MSCAN Control Register 1 (CANCTL1)"), the recovery from bus-off starts after both independent events have become true:

- 128 occurrences of 11 consecutive recessive bits on the CAN bus have been monitored
- BOHOLD in Section 12.3.12, "MSCAN Miscellaneous Register (CANMISC) has been cleared by the user

These two events may occur in any order.



Field	Description
3 WAKE	 Receiver Wakeup Method Select — Refer to Section 14.3.3.2, "Receiver Wakeup Operation" for more information. 0 Idle-line wakeup. 1 Address-mark wakeup.
2 ILT	Idle Line Type Select — Setting this bit to 1 ensures that the stop bit and logic 1 bits at the end of a characterdo not count toward the 10 or 11 bit times of logic high level needed by the idle line detection logic. Refer toSection 14.3.3.2.1, "Idle-Line Wakeup" for more information.0 Idle character bit count starts after start bit.1 Idle character bit count starts after stop bit.
1 PE	 Parity Enable — Enables hardware parity generation and checking. When parity is enabled, the most significant bit (MSB) of the data character (eighth or ninth data bit) is treated as the parity bit. 0 No hardware parity generation or checking. 1 Parity enabled.
0 PT	 Parity Type — Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even. 0 Even parity. 1 Odd parity.

14.2.3 SCI Control Register 2 (SCIxC2)

This register can be read or written at any time.



Figure 14-7. SCI Control Register 2 (SCIxC2)

Table 14-5. SCIxC2 Field Descriptions

Field	Description		
7 TIE	Transmit Interrupt Enable (for TDRE)00111Hardware interrupt requested when TDRE flag is 1.		
6 TCIE	Transmission Complete Interrupt Enable (for TC)0011Hardware interrupt requested when TC flag is 1.		
5 RIE	Receiver Interrupt Enable (for RDRF)0Hardware interrupts from RDRF disabled (use polling).1Hardware interrupt requested when RDRF flag is 1.		
4 ILIE	Idle Line Interrupt Enable (for IDLE)00111Hardware interrupt requested when IDLE flag is 1.		



16.2.1.1 EXTCLK — External Clock Source

Control bits in the timer status and control register allow the user to select nothing (timer disable), the bus-rate clock (the normal default source), a crystal-related clock, or an external clock as the clock which drives the TPM prescaler and subsequently the 16-bit TPM counter. The external clock source is synchronized in the TPM. The bus clock clocks the synchronizer; the frequency of the external source must be no more than one-fourth the frequency of the bus-rate clock, to meet Nyquist criteria and allowing for jitter.

The external clock signal shares the same pin as a channel I/O pin, so the channel pin will not be usable for channel I/O function when selected as the external clock source. It is the user's responsibility to avoid such settings. If this pin is used as an external clock source (CLKSB:CLKSA = 1:1), the channel can still be used in output compare mode as a software timer (ELSnB:ELSnA = 0:0).

16.2.1.2 TPMxCHn — TPM Channel n I/O Pin(s)

Each TPM channel is associated with an I/O pin on the MCU. The function of this pin depends on the channel configuration. The TPM pins share with general purpose I/O pins, where each pin has a port data register bit, and a data direction control bit, and the port has optional passive pullups which may be enabled whenever a port pin is acting as an input.

The TPM channel does not control the I/O pin when (ELSnB:ELSnA = 0:0) or when (CLKSB:CLKSA = 0:0) so it normally reverts to general purpose I/O control. When CPWMS = 1 (and ELSnB:ELSnA not = 0:0), all channels within the TPM are configured for center-aligned PWM and the TPMxCHn pins are all controlled by the TPM system. When CPWMS=0, the MSnB:MSnA control bits determine whether the channel is configured for input capture, output compare, or edge-aligned PWM.

When a channel is configured for input capture (CPWMS=0, MSnB:MSnA = 0:0 and ELSnB:ELSnA not = 0:0), the TPMxCHn pin is forced to act as an edge-sensitive input to the TPM. ELSnB:ELSnA control bits determine what polarity edge or edges will trigger input-capture events. A synchronizer based on the bus clock is used to synchronize input edges to the bus clock. This implies the minimum pulse width—that can be reliably detected—on an input capture pin is four bus clock periods (with ideal clock pulses as near as two bus clocks can be detected). TPM uses this pin as an input capture input to override the port data and data direction controls for the same pin.

When a channel is configured for output compare (CPWMS=0, MSnB:MSnA = 0:1 and ELSnB:ELSnA not = 0:0), the associated data direction control is overridden, the TPMxCHn pin is considered an output controlled by the TPM, and the ELSnB:ELSnA control bits determine how the pin is controlled. The remaining three combinations of ELSnB:ELSnA determine whether the TPMxCHn pin is toggled, cleared, or set each time the 16-bit channel value register matches the timer counter.

When the output compare toggle mode is initially selected, the previous value on the pin is driven out until the next output compare event—then the pin is toggled.

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
00	No clock selected (TPM counter disabled)
01	Bus rate clock
10	Fixed system clock
11	External source

	Table 16-7.	TPM	Clock	Source	Selection
--	-------------	-----	-------	--------	-----------

The bus rate clock is the main system bus clock for the MCU. This clock source requires no synchronization because it is the clock that is used for all internal MCU activities including operation of the CPU and buses.

In MCUs that have no PLL and FLL or the PLL and FLL are not engaged, the fixed system clock source is the same as the bus-rate-clock source, and it does not go through a synchronizer. When a PLL or FLL is present and engaged, a synchronizer is required between the crystal divided-by two clock source and the timer counter so counter transitions will be properly aligned to bus-clock transitions. A synchronizer will be used at chip level to synchronize the crystal-related source clock to the bus clock.

The external clock source may be connected to any TPM channel pin. This clock source always has to pass through a synchronizer to assure that counter transitions are properly aligned to bus clock transitions. The bus-rate clock drives the synchronizer; therefore, to meet Nyquist criteria even with jitter, the frequency of the external clock source must not be faster than the bus rate divided-by four. With ideal clocks the external clock can be as fast as bus clock divided by four.

When the external clock source shares the TPM channel pin, this pin should not be used for other channel timing functions. For example, it would be ambiguous to configure channel 0 for input capture when the TPM channel 0 pin was also being used as the timer external clock source. (It is the user's responsibility to avoid such settings.) The TPM channel could still be used in output compare mode for software timing functions (pin controls set not to affect the TPM channel pin).

16.4.1.2 Counter Overflow and Modulo Reset

An interrupt flag and enable are associated with the 16-bit main counter. The flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE=0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE=1) where a static hardware interrupt is generated whenever the TOF flag is equal to one.

The conditions causing TOF to become set depend on whether the TPM is configured for center-aligned PWM (CPWMS=1). In the simplest mode, there is no modulus limit and the TPM is not in CPWMS=1 mode. In this case, the 16-bit timer counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the TPM is in center-aligned PWM mode (CPWMS=1), the TOF flag gets set as the counter changes direction at the end of the count value set in the modulus register (that is, at the transition from the value set in the modulus register to the next lower count value). This corresponds to the end of a PWM period (the 0x0000 count value corresponds to the center of a period).



Num	с	Rating	Symbol	Value	Unit	Temp. Code
1	D	Operating temperature range (packaged)	T _A	-40 to 125 -40 to 105 -40 to 85	°C	M > C
2	Т	Maximum Junction Temperature ¹	TJ	135	°C	_
3	D	Thermal resistance ²				
		Single-layer board				
		64-pin LQFP	θ_{JA}	69	°C/W	
		48-pin LQFP	θ_{JA}	75	°C/W	
		32-pin LQFP	θ_{JA}	80	°C/W	
		Four-Layer board				
		64-pin LQFP	θ_{JA}	51	°C/W	
		48-pin LQFP	θ _{JA}	51	°C/W	
		32-pin LQFP	θ_{JA}	52	°C/W	

 Table A-3. Thermal Characteristics

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Junction to Ambient Natural Convection

The average chip-junction temperature (T_I) in °C can be obtained from:

$$T_{J} = T_{A} + (P_{D} \times \theta_{JA})$$
 Eqn. A-1

where:

 T_A = Ambient temperature, °C θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W $P_D = P_{int} + P_{I/O}$ $P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power $P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_{D} = K \div (T_{J} + 273^{\circ}C) \qquad \qquad Eqn. A-2$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^{\circ}C) + \theta_{JA} \times (P_D)^2$$
 Eqn. A-3

Num	с	Parameter	Symbol	V _{DD} (V)	Typical ¹	Max ²	Unit
6		RTC adder to stop2 or stop3 ⁵ , 25°C		5	300	_	nA
0				3	300	_	nA
7		LVD adder to stop3 (LVDE = LVDSE = 1)		5	110	—	μA
1				3	90	—	μA
		Adder to stop3 for oscillator enabled ⁶		5	5	—	μA
8		(IRCLKEN = 1 and IREFSTEN = 1 or ERCLKEN = 1 and EREFSTEN = 1)		3	5		μA

Table A-7. Supply Current Characteristics (continued)

¹ Typicals are measured at 25°C, unless otherwise noted.

² Maximum values in this column apply for the full operating temperature range of the device unless otherwise noted.

³ All modules except ADC active, MCG configured for FBE, and does not include any dc loads on port pins

⁴ Stop currents are tested in production for 25°C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

⁵ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

⁶ Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

A.8 Analog Comparator (ACMP) Electricals

Table A-8. Analog Comparator Electrical Specifications

Num	С	Rating	Symbol	Min	Typical	Max	Unit
1		Supply voltage	V _{DD}	2.7	_	5.5	V
2	D	Supply current (active)	I _{DDAC}	_	20	35	μA
3	D	Analog input voltage	V _{AIN}	V _{SS} – 0.3	_	V _{DD}	V
4	D	Analog input offset voltage	V _{AIO}		20	40	mV
5	D	Analog Comparator hysteresis	V _H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I _{ALKG}			1.0	μΑ
7	D	Analog Comparator initialization delay	t _{AINIT}	—	_	1.0	μs

A.9 ADC Characteristics

Table A-9	. 12-bit	ADC	Operating	Conditions
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Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V _{DDAD}	2.7	—	5.5	V	
	Delta to V _{DD} (V _{DD} -V _{DDAD}) ²	ΔV_{DDAD}	-100	0	+100	mV	
Ground voltage	Delta to $V_{SS} (V_{SS} - V_{SSAD})^2$	ΔV_{SSAD}	-100	0	+100	mV	



Appendix B Timer Pulse-Width Modulator (TPMV2)



When background mode is active, the timer counter and the coherency mechanism are frozen such that the buffer latches remain in the state they were in when the background mode became active even if one or both bytes of the counter are read while background mode is active.

B.2.3 Timer Counter Modulo Registers (TPMxMODH:TPMxMODL)

The read/write TPM modulo registers contain the modulo value for the TPM counter. After the TPM counter reaches the modulo value, the TPM counter resumes counting from 0x0000 at the next clock (CPWMS = 0) or starts counting down (CPWMS = 1), and the overflow flag (TOF) becomes set. Writing to TPMxMODH or TPMxMODL inhibits TOF and overflow interrupts until the other byte is written. Reset sets the TPM counter modulo registers to 0x0000, which results in a free-running timer counter (modulo disabled).



It is good practice to wait for an overflow interrupt so both bytes of the modulo register can be written well before a new overflow. An alternative approach is to reset the TPM counter before writing to the TPM modulo registers to avoid confusion about when the first counter overflow will occur.





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