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Details

Product Status	Active
Core Processor	508
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
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Chapter 1 Device Overview





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 V_{REFH} and V_{REFL} are internally connected to V_{DDA} and V_{SSA} , respectively.

Figure 2-3. 32-Pin LQFP



Table 4-1. Reset and Interrupt Vectors

Address (High/Low)	Vector	Vector Name
0xFFCC:0xFFCD	RTC	Vrtc
0xFFCE:0xFFCF	IIC	Viic
0xFFD0:0xFFD1	ADC Conversion	Vadc
0xFFD2:0xFFD3	Port A, Port B, Port D	Vport
0xFFD4:0xFFD5	SCI2 Transmit	Vsci2tx
0xFFD6:0xFFD7	SCI2 Receive	Vsci2rx
0xFFD8:0xFFD9	SCI2 Error	Vsci2err
0xFFDA:0xFFDB	SCI1 Transmit	Vsci1tx
0xFFDC:0xFFDD	SCI1 Receive	Vsci1rx
0xFFDE:0xFFDF	SCI1 Error	Vsci1err
0xFFE0:0xFFE1	SPI	Vspi
0xFFE2:0xFFE3	TPM2 Overflow	Vtpm2ovf
0xFFE4:0xFFE5	TPM2 Channel 1	Vtpm2ch1
0xFFE6:0xFFE7	TPM2 Channel 0	Vtpm2ch0
0xFFE8:0xFFE9	TPM1 Overflow	Vtpm1ovf
0xFFEA:0xFFEB	TPM1 Channel 5	Vtpm1ch5
0xFFEC:0xFFED	TPM1 Channel 4	Vtpm1ch4
0xFFEE:0xFFEF	TPM1 Channel 3	Vtpm1ch3
0xFFF0:0xFFF1	TPM1 Channel 2	Vtpm1ch2
0xFFF2:0xFFF3	TPM1 Channel 1	Vtpm1ch1
0xFFF4:0xFFF5	TPM1 Channel 0	Vtpm1ch0
0xFFF6:0xFFF7	MCG Loss of lock	Vlol
0xFFF8:0xFFF9	Low-Voltage Detect VIvd	
0xFFFA:0xFFFB	IRQ	Virq
0xFFFC:0xFFFD	SWI	Vswi
0xFFFE:0xFFFF	Reset	Vreset



1

F

SEC

0

F



= Unimplemented or Reserved

F

Reset

F

F

F = loaded from nonvolatile location NVOPT during reset

0

2

0

0

Figure 4-6. Flash and EEPROM Options Register (FOPT)

0

Table 4-9. FOPT Register Field Descriptions

Field	Description
7 KEYEN	 Backdoor Key Mechanism Enable — When this bit is 0, the backdoor key mechanism cannot be used to disengage security. The backdoor key mechanism is accessible only from user (secured) firmware. BDM commands cannot be used to write key comparison values that would unlock the backdoor key. For more detailed information about the backdoor key mechanism, refer to Section 4.5.9, "Security." 0 No backdoor key access allowed. 1 If user firmware writes an 8-byte value that matches the nonvolatile backdoor key (NVBACKKEY through NVBACKKEY+7 in that order), security is temporarily disengaged until the next MCU reset.
6 FNORED	 Vector Redirection Disable — When this bit is 1, then vector redirection is disabled. 0 Vector redirection enabled. 1 Vector redirection disabled.
5 EPGMOD	 EEPROM Sector Mode — When this bit is 0, each sector is split into two pages (4-byte mode). When this bit is 1, each sector is in a single page (8-byte mode). 0 Half of each EEPROM sector is in Page 0 and the other half is in Page 1. 1 Each sector is in a single page.
1:0 SEC	Security State Code — This 2-bit field determines the security state of the MCU as shown in Table 4-10. When the MCU is secure, the contents of RAM, EEPROM and Flash memory cannot be accessed by instructions from any unsecured source including the background debug interface. SEC changes to 1:0 after successful backdoor key entry or a successful blank check of Flash. For more detailed information about security, refer to Section 4.5.9, "Security."

Table 4-10. Security States¹

SEC[1:0]	Description
0:0	secure
0:1	secure
1:0	unsecured
1:1	secure

¹ SEC changes to 1:0 after successful backdoor key entry or a successful blank check of Flash.



Chapter 5 Resets, Interrupts, and General System Control

5.8.2 System Reset Status Register (SRS)

This high page register includes read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to BDFR in the SBDFR register, none of the status bits in SRS will be set. Writing any value to this register address causes a COP reset when the COP is enabled except the values 0x55 and 0xAA. Writing a 0x55-0xAA sequence to this address clears the COP watchdog timer without affecting the contents of this register. The reset state of these bits depends on what caused the MCU to reset.

	7	6	5	4	3	2	1	0
R	POR	PIN	COP	ILOP	ILAD	LOC	LVD	0
W		Wr	iting 0x55, 0xA	A to SRS addr	ess clears CO	P watchdog tim	ier.	
POR:	1	0	0	0	0	0	1	0
LVD:	u	0	0	0	0	0	1	0
Any other reset:	0	Note ⁽¹⁾	Note ⁽¹⁾	Note ⁽¹⁾	Note ⁽¹⁾	0	0	0

¹ Any of these reset sources that are active at the time of reset entry will cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset entry will be cleared.

Figure 5-3. System Reset Status (SRS)

Table 5-3. SRS Register Field Descriptions

Field	Description
7 POR	 Power-On Reset — Reset was caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVD) status bit is also set to indicate that the reset occurred while the internal supply was below the LVD threshold. 0 Reset not caused by POR. 1 POR caused reset.
6 PIN	 External Reset Pin — Reset was caused by an active-low level on the external reset pin. 0 Reset not caused by external reset pin. 1 Reset came from external reset pin.
5 COP	 Computer Operating Properly (COP) Watchdog — Reset was caused by the COP watchdog timer timing out. This reset source can be blocked by COPE = 0. 0 Reset not caused by COP timeout. 1 Reset caused by COP timeout.
4 ILOP	 Illegal Opcode — Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register. 0 Reset not caused by an illegal opcode. 1 Reset caused by an illegal opcode.
3 ILAD	 Illegal Address — Reset was caused by an attempt to access either data or an instruction at an unimplemented memory address. 0 Reset not caused by an illegal address. 1 Reset caused by an illegal address.



Chapter 6 Parallel Input/Output Control

6.5.3.5 Port C Drive Strength Selection Register (PTCDS)

_	7	6	5	4	3	2	1	0
R W	PTCDS7	PTCDS6	PTCDS5	PTCDS4	PTCDS3	PTCDS2	PTCDS1	PTCDS0
Reset:	0	0	0	0	0	0	0	0

Figure 6-23. Drive Strength Selection for Port C Register (PTCDS)

Table 6-21. PTCDS Register Field Descriptions

Field	Description
7:0 PTCDS[7:0]	 Output Drive Strength Selection for Port C Bits — Each of these control bits selects between low and high output drive for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect. 0 Low output drive strength selected for port C bit n. 1 High output drive strength selected for port C bit n.



Chapter 7 Central Processor Unit (S08CPUV3)

Source	Operation	dress ode	Object Code	rcles	Cyc-by-Cyc	Affect on CCR	
1 Onn		PdA		රි	Details	V 1 1 H	INZC
INC opr8a INCA INCX INC oprx8,X INC ,X INC oprx8,SP	$\begin{array}{llllllllllllllllllllllllllllllllllll$	DIR INH INH IX1 IX SP1	3C dd 4C 5C 6C ff 7C 9E 6C ff	5 1 1 5 4 6	rfwpp p rfwpp rfwp prfwpp	↓11-	- \$ \$ -
JMP opr8a JMP opr16a JMP oprx16,X JMP oprx8,X JMP ,X	Jump PC ← Jump Address	DIR EXT IX2 IX1 IX	BC dd CC hh ll DC ee ff EC ff FC	3 4 4 3 3	2000 2000 2000 2000 2000 2000 2000 200	- 1 1 -	
JSR opr8a JSR opr16a JSR oprx16,X JSR oprx8,X JSR ,X	Jump to Subroutine PC \leftarrow (PC) + n ($n = 1, 2, \text{ or } 3$) Push (PCL); SP \leftarrow (SP) – \$0001 Push (PCH); SP \leftarrow (SP) – \$0001 PC \leftarrow Unconditional Address	DIR EXT IX2 IX1 IX	BD dd CD hh ll DD ee ff ED ff FD	5 6 5 5	ssppp pssppp ssppp ssppp	- 1 1 -	
LDA #opr8i LDA opr8a LDA opr16a LDA oprx16,X LDA oprx8,X LDA ,X LDA oprx16,SP LDA oprx8,SP	Load Accumulator from Memory $A \leftarrow (M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	A6 ii B6 dd C6 hh ll D6 ee ff E6 ff F6 9E D6 ee ff 9E E6 ff	2 3 4 3 3 5 4	pp rpp prpp rpp rfp pprpp prpp	011-	- ‡ ‡ -
LDHX #opr16i LDHX opr8a LDHX opr16a LDHX ,X LDHX oprx16,X LDHX oprx8,X LDHX oprx8,SP	Load Index Register (H:X) H:X ← (M:M + \$0001)	IMM DIR EXT IX IX2 IX1 SP1	45 jj kk 55 dd 32 hh ll 9E AE 9E BE ee ff 9E CE ff 9E FE ff	3 4 5 5 6 5 5	ppp rrpp prrpp prrfp pprrpp prrpp prrpp	011-	- \$ \$ -
LDX #opr8i LDX opr8a LDX opr16a LDX oprx16,X LDX oprx8,X LDX ,X LDX oprx16,SP LDX oprx8,SP	Load X (Index Register Low) from Memory $X \leftarrow (M)$	IMM DIR EXT IX2 IX1 IX SP2 SP1	AE ii BE dd CE hh ll DE ee ff EE ff FE 9E DE ee ff 9E EE ff	2 3 4 3 3 5 4	pp rpp prpp rpp rfp pprpp prpp	011-	- \$ \$ -
LSL opr8a LSLA LSLX LSL oprx8,X LSL ,X LSL oprx8,SP	Logical Shift Left 	DIR INH INH IX1 IX SP1	38 dd 48 58 68 ff 78 9E 68 ff	5 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	↓11-	- ↓ ↓ ↓
LSR opr8a LSRA LSRX LSR oprx8,X LSR ,X LSR oprx8,SP	Logical Shift Right $0 \rightarrow \boxed{1} \\ b7 \\ b0$	DIR INH INH IX1 IX SP1	34 dd 44 54 64 ff 74 9E 64 ff	5 1 1 5 4 6	rfwpp p rfwpp rfwp prfwp	↓11-	- 0 ‡ ‡

Table 7-2. Instruction Set Summary (Sheet 5 of 9)



Source	Operation	dress lode	Object Code	/cles	Cyc-by-Cyc	Affect on CCR	
		PΑ		ΰ	Dotano	V 1 1 H	INZC
SUB #opr8i SUB opr8a SUB opr16a SUB oprx16,X SUB oprx8,X SUB ,X SUB oprx16,SP SUB oprx8,SP	Subtract A \leftarrow (A) – (M)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A0 ii B0 dd C0 hh ll D0 ee ff E0 ff F0 9E D0 ee ff 9E E0 ff	2 3 4 3 3 5 4	pp rpp prpp rpp rfp pprpp prpp	↓11-	- ↓ ↓ ↓
SWI	Software Interrupt PC \leftarrow (PC) + \$0001 Push (PCL); SP \leftarrow (SP) - \$0001 Push (PCH); SP \leftarrow (SP) - \$0001 Push (X); SP \leftarrow (SP) - \$0001 Push (A); SP \leftarrow (SP) - \$0001 Push (CCR); SP \leftarrow (SP) - \$0001 I \leftarrow 1; PCH \leftarrow Interrupt Vector High Byte PCL \leftarrow Interrupt Vector Low Byte	INH	83	11	sssssvvfppp	- 1 1 -	1
ТАР	Transfer Accumulator to CCR $CCR \leftarrow (A)$	INH	84	1	р	\$11\$	¢ ¢ ¢ ¢ ¢
ТАХ	Transfer Accumulator to X (Index Register Low) $X \leftarrow (A)$	INH	97	1	р	- 1 1 -	
ТРА	Transfer CCR to Accumulator $A \leftarrow (CCR)$	INH	85	1	q	- 1 1 -	
TST opr8a TSTA TSTX TST oprx8,X TST oprx8,SP	Test for Negative or Zero (M) - \$00 (A) - \$00 (X) - \$00 (M) - \$00 (M) - \$00 (M) - \$00 (M) - \$00	DIR INH INH IX1 IX SP1	3D dd 4D 5D 6D ff 7D 9E 6D ff	4 1 4 3 5	rfpp p rfpp rfp prfpp	011-	- \$ \$ -
TSX	Transfer SP to Index Reg. H:X \leftarrow (SP) + \$0001	INH	95	2	fp	- 1 1 -	
ТХА	Transfer X (Index Reg. Low) to Accumulator $A \leftarrow (X)$	INH	9F	1	q	- 1 1 -	

Table 7-2. Instruction Set Summary (Sheet 8 of 9)



Chapter 8 Multi-Purpose Clock Generator (S08MCGV1)

8.4 Functional Description

8.4.1 Operational Modes



Figure 8-8. Clock Switching Modes

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Chapter 11 Inter-Integrated Circuit (S08IICV2)

Refer to the direct-page register summary in the memory chapter of this document for the absolute address assignments for all IIC registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

11.3.1 IIC Address Register (IICA)



Figure 11-3. IIC Address Register (IICA)

Table	11-1.	IICA	Field	Descriptions
-------	-------	------	-------	--------------

Field	Description
7–1 AD[7:1]	Slave Address. The AD[7:1] field contains the slave address to be used by the IIC module. This field is used on the 7-bit address scheme and the lower seven bits of the 10-bit address scheme.

11.3.2 IIC Frequency Divider Register (IICF)



Figure 11-4. IIC Frequency Divider Register (IICF)



11.4.1.3 Data Transfer

Before successful slave addressing is achieved, the data transfer can proceed byte-by-byte in a direction specified by the R/\overline{W} bit sent by the calling master.

All transfers that come after an address cycle are referred to as data transfers, even if they carry sub-address information for the slave device

Each data byte is 8 bits long. Data may be changed only while SCL is low and must be held stable while SCL is high as shown in Figure 11-9. There is one clock pulse on SCL for each data bit, the msb being transferred first. Each data byte is followed by a 9th (acknowledge) bit, which is signalled from the receiving device. An acknowledge is signalled by pulling the SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit time, the SDA line must be left high by the slave. The master interprets the failed acknowledge as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets this as an end of data transfer and releases the SDA line.

In either case, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a stop signal.
- Commences a new calling by generating a repeated start signal.

11.4.1.4 Stop Signal

The master can terminate the communication by generating a stop signal to free the bus. However, the master may generate a start signal followed by a calling command without generating a stop signal first. This is called repeated start. A stop signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see Figure 11-9).

The master can generate a stop even if the slave has generated an acknowledge at which point the slave must release the bus.

11.4.1.5 Repeated Start Signal

As shown in Figure 11-9, a repeated start signal is a start signal generated without first generating a stop signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

11.4.1.6 Arbitration Procedure

The IIC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case,



Field	Description
7 RXFRM ¹	 Received Frame Flag — This bit is read and clear only. It is set when a receiver has received a valid message correctly, independently of the filter configuration. After it is set, it remains set until cleared by software or reset. Clearing is done by writing a 1. Writing a 0 is ignored. This bit is not valid in loopback mode. 0 No valid message was received since last clearing this flag 1 A valid message was received since last clearing of this flag
6 RXACT	 Receiver Active Status — This read-only flag indicates the MSCAN is receiving a message. The flag is controlled by the receiver front end. This bit is not valid in loopback mode. MSCAN is transmitting or idle² MSCAN is receiving a message (including when arbitration is lost)²
5 CSWAI ³	 CAN Stops in Wait Mode — Enabling this bit allows for lower power consumption in wait mode by disabling all the clocks at the CPU bus interface to the MSCAN module. 0 The module is not affected during wait mode 1 The module ceases to be clocked during wait mode
4 SYNCH	Synchronized Status — This read-only flag indicates whether the MSCAN is synchronized to the CAN bus and able to participate in the communication process. It is set and cleared by the MSCAN.0MSCAN is not synchronized to the CAN bus1MSCAN is synchronized to the CAN bus
3 TIME	Timer Enable — This bit activates an internal 16-bit wide free running timer which is clocked by the bit clock rate. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active TX/RX buffer. As soon as a message is acknowledged on the CAN bus, the time stamp will be written to the highest bytes (0x000E, 0x000F) in the appropriate buffer (see Section 12.4, "Programmer's Model of Message Storage"). The internal timer is reset (all bits set to 0) when disabled. This bit is held low in initialization mode. 0 Disable internal MSCAN timer 1 Enable internal MSCAN timer
2 WUPE ⁴	 Wake-Up Enable — This configuration bit allows the MSCAN to restart from sleep mode when traffic on CAN is detected (see Section 12.5.5.4, "MSCAN Sleep Mode"). This bit must be configured before sleep mode entry for the selected function to take effect. 0 Wake-up disabled — The MSCAN ignores traffic on CAN 1 Wake-up enabled — The MSCAN is able to restart

Table 12-1. CANCTL0 Register Field Descriptions



The MSCAN then schedules the message for transmission and signals the successful transmission of the buffer by setting the associated TXE flag. A transmit interrupt (see Section 12.5.7.2, "Transmit Interrupt") is generated¹ when TXEx is set and can be used to drive the application software to re-load the buffer.

If more than one buffer is scheduled for transmission when the CAN bus becomes available for arbitration, the MSCAN uses the local priority setting of the three buffers to determine the prioritization. For this purpose, every transmit buffer has an 8-bit local priority field (PRIO). The application software programs this field when the message is set up. The local priority reflects the priority of this particular message relative to the set of messages being transmitted from this node. The lowest binary value of the PRIO field is defined to be the highest priority. The internal scheduling process takes place whenever the MSCAN arbitrates for the CAN bus. This is also the case after the occurrence of a transmission error.

When a high priority message is scheduled by the application software, it may become necessary to abort a lower priority message in one of the three transmit buffers. Because messages that are already in transmission cannot be aborted, the user must request the abort by setting the corresponding abort request bit (ABTRQ) (see Section 12.3.8, "MSCAN Transmitter Message Abort Request Register (CANTARQ)".) The MSCAN then grants the request, if possible, by:

- 1. Setting the corresponding abort acknowledge flag (ABTAK) in the CANTAAK register.
- 2. Setting the associated TXE flag to release the buffer.
- 3. Generating a transmit interrupt. The transmit interrupt handler software can determine from the setting of the ABTAK flag whether the message was aborted (ABTAK = 1) or sent (ABTAK = 0).

12.5.2.3 Receive Structures

The received messages are stored in a five stage input FIFO. The five message buffers are alternately mapped into a single memory area (see Figure 12-38). The background receive buffer (RxBG) is exclusively associated with the MSCAN, but the foreground receive buffer (RxFG) is addressable by the CPU (see Figure 12-38). This scheme simplifies the handler software because only one address area is applicable for the receive process.

All receive buffers have a size of 15 bytes to store the CAN control bits, the identifier (standard or extended), the data contents, and a time stamp, if enabled (see Section 12.4, "Programmer's Model of Message Storage").

The receiver full flag (RXF) (see Section 12.3.4.1, "MSCAN Receiver Flag Register (CANRFLG)") signals the status of the foreground receive buffer. When the buffer contains a correctly received message with a matching identifier, this flag is set.

On reception, each message is checked to see whether it passes the filter (see Section 12.5.3, "Identifier Acceptance Filter") and simultaneously is written into the active RxBG. After successful reception of a valid message, the MSCAN shifts the content of RxBG into the receiver FIFO², sets the RXF flag, and generates a receive interrupt (see Section 12.5.7.3, "Receive Interrupt") to the CPU³. The user's receive handler must read the received message from the RxFG and then reset the RXF flag to acknowledge the interrupt and to release the foreground buffer. A new message, which can follow immediately after the IFS

^{1.} The transmit interrupt occurs only if not masked. A polling scheme can be applied on TXEx also.

^{2.} Only if the RXF flag is not set.

^{3.} The receive interrupt occurs only if not masked. A polling scheme can be applied on RXF also.



When the TPM is configured for center-aligned PWM (and ELSnB:ELSnA not = 0:0), the data direction for all channels in this TPM are overridden, the TPMxCHn pins are forced to be outputs controlled by the TPM, and the ELSnA bits control the polarity of each TPMxCHn output. If ELSnB:ELSnA=1:0, the corresponding TPMxCHn pin is cleared when the timer counter is counting up, and the channel value register matches the timer counter; the TPMxCHn pin is set when the timer counter is counting down, and the channel value register matches the timer counter. If ELSnA=1, the corresponding TPMxCHn pin is set when the timer counter; the TPMxCHn pin is cleared when the channel value register matches the timer counter is counting up and the channel value register matches the timer counter; the TPMxCHn pin is cleared when the timer counter is the timer counter; the timer counter is counting up and the channel value register matches the timer counter is counting the timer counter; the timer counter is counter is counter; the timer counter is counting up and the channel value register matches the timer counter; the timer counter is counter is counter; the timer counter is counter is counter is counter.

TPMxMODH:TPMxMODL = 0x0008 TPMxCnVH:TPMxCnVL = 0x0005





TPMxMODH:TPMxMODL = 0x0008 TPMxCnVH:TPMxCnVL = 0x0005



Figure 16-6. Low-True Pulse of a Center-Aligned PWM



Chapter 17 Development Support

A-Only — Trigger when the address matches the value in comparator A

A OR B — Trigger when the address matches either the value in comparator A or the value in comparator B

A Then B — Trigger when the address matches the value in comparator B but only after the address for another cycle matched the value in comparator A. There can be any number of cycles after the A match and before the B match.

A AND B Data (Full Mode) — This is called a full mode because address, data, and R/W (optionally) must match within the same bus cycle to cause a trigger event. Comparator A checks address, the low byte of comparator B checks data, and R/W is checked against RWA if RWAEN = 1. The high-order half of comparator B is not used.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

A AND NOT B Data (Full Mode) — Address must match comparator A, data must not match the low half of comparator B, and R/W must match RWA if RWAEN = 1. All three conditions must be met within the same bus cycle to cause a trigger.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

Event-Only B (Store Data) — Trigger events occur each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

A Then Event-Only B (Store Data) — After the address has matched the value in comparator A, a trigger event occurs each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

Inside Range ($A \le Address \le B$) — A trigger occurs when the address is greater than or equal to the value in comparator A and less than or equal to the value in comparator B at the same time.

Outside Range (Address < A or Address > B) — A trigger occurs when the address is either less than the value in comparator A or greater than the value in comparator B.



Field	Description
2 WS	 Wait or Stop Status — When the target CPU is in wait or stop mode, most BDC commands cannot function. However, the BACKGROUND command can be used to force the target CPU out of wait or stop and into active background mode where all BDC commands work. Whenever the host forces the target MCU into active background mode, the host should issue a READ_STATUS command to check that BDMACT = 1 before attempting other BDC commands. 0 Target CPU is running user application code or in active background mode (was not in wait or stop mode when background became active) 1 Target CPU is in wait or stop mode, or a BACKGROUND command was used to change from wait or stop to active background mode
1 WSF	 Wait or Stop Failure Status — This status bit is set if a memory access command failed due to the target CPU executing a wait or stop instruction at or about the same time. The usual recovery strategy is to issue a BACKGROUND command to get out of wait or stop mode into active background mode, repeat the command that failed, then return to the user program. (Typically, the host would restore CPU registers and stack values and re-execute the wait or stop instruction.) 0 Memory access did not conflict with a wait or stop instruction 1 Memory access command failed because the CPU entered wait or stop mode
0 DVF	 Data Valid Failure Status — This status bit is not used in the MC9S08DZ60 Series because it does not have any slow access memory. 0 Memory access did not conflict with a slow memory access 1 Memory access command failed because CPU was not finished with a slow memory access

Table 17-2. BDCSCR Register Field Descriptions (continued)

17.4.1.2 BDC Breakpoint Match Register (BDCBKPT)

This 16-bit register holds the address for the hardware breakpoint in the BDC. The BKPTEN and FTS control bits in BDCSCR are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDCBKPT register but is not accessible to user programs because it is not located in the normal memory map of the MCU. Breakpoints are normally set while the target MCU is in active background mode before running the user application program. For additional information about setup and use of the hardware breakpoint logic in the BDC, refer to Section 17.2.4, "BDC Hardware Breakpoint."

17.4.2 System Background Debug Force Reset Register (SBDFR)

This register contains a single write-only control bit. A serial background mode command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.





A.13 Flash and EEPROM

This section provides details about program/erase times and program-erase endurance for the Flash and EEPROM memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, "Memory."

Num	С	Rating	Symbol	Min	Min Typical Max		
1	—	Supply voltage for program/erase	V _{prog/erase}	2.7	2.7 5.5		
2	_	Supply voltage for read operation 0 < f _{Bus} < 8 MHz 0 < f _{Bus} < 20 MHz	V _{Read}	2.7 5.5			V
3	_	Internal FCLK frequency ¹	f _{FCLK}	150	150 200		
4	_	Internal FCLK period (1/FCLK)	t _{Fcyc}	5		6.67	μs
5	_	Byte program time (random location) ⁽²⁾	t _{prog}		t _{Fcyc}		
6	—	Byte program time (burst mode) ⁽²⁾	t _{Burst}		t _{Fcyc}		
7	_	Page erase time ²	t _{Page}		t _{Fcyc}		
8	_	Mass erase time ⁽²⁾	t _{Mass}		t _{Fcyc}		
9	с	Flash Program/erase endurance ³ T _L to T _H = -40° C to + 125°C T = 25°C	N _{FLPE}	10,000	 100,000		cycles
10	С	EEPROM Program/erase endurance ³ T_L to $T_H = -40^{\circ}$ C to + 0°C T_L to $T_H = 0^{\circ}$ C to + 125°C $T = 25^{\circ}$ C	NEEPE	10,000 — — 50,000 — — — 100,000 —		cycles	
11	С	Data retention ⁴	t _{D_ret}	15	100	_	years

Table A-17.	Flash and	EEPROM	Characteristics
	i laon ana		01141 40101 101100

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

³ Typical endurance for Flash and EEPROM is based on the intrinsic bit cell performance. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

⁴ Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*



Appendix B Timer Pulse-Width Modulator (TPMV2)

Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

B.2.1 Timer Status and Control Register (TPMxSC)

TPMxSC contains the overflow status flag and control bits that are used to configure the interrupt enable, TPM configuration, clock source, and prescale divisor. These controls relate to all channels within this timer module.

	7	6	5	4	3	2	1	0	
R	TOF	TOIE	CPWMS	CLKSB	CLKSA	PS2	PS1	PS0	
vv									
Reset	0	0	0	0	0	0	0	0	
	= Unimplemented or Reserved								

Figure B-2. Timer Status and Control Register (TPMxSC)

Field	Description
7 TOF	Timer Overflow Flag — This flag is set when the TPM counter changes to 0x0000 after reaching the modulo value programmed in the TPM counter modulo registers. When the TPM is configured for CPWM, TOF is set after the counter has reached the value in the modulo register, at the transition to the next lower count value. Clear TOF by reading the TPM status and control register when TOF is set and then writing a 0 to TOF. If another TPM overflow occurs before the clearing sequence is complete, the sequence is reset so TOF would remain set after the clear sequence was completed for the earlier TOF. Reset clears TOF. Writing a 1 to TOF has no effect. 0 TPM counter has not reached modulo value or overflow 1 TPM counter has overflowed
6 TOIE	 Timer Overflow Interrupt Enable — This read/write bit enables TPM overflow interrupts. If TOIE is set, an interrupt is generated when TOF equals 1. Reset clears TOIE. 0 TOF interrupts inhibited (use software polling) 1 TOF interrupts enabled
5 CPWMS	 Center-Aligned PWM Select — This read/write bit selects CPWM operating mode. Reset clears this bit so the TPM operates in up-counting mode for input capture, output compare, and edge-aligned PWM functions. Setting CPWMS reconfigures the TPM to operate in up-/down-counting mode for CPWM functions. Reset clears CPWMS. All TPMx channels operate as input capture, output compare, or edge-aligned PWM mode as selected by the MSnB:MSnA control bits in each channel's status and control register All TPMx channels operate in center-aligned PWM mode
4:3 CLKS[B:A]	Clock Source Select — As shown in Table B-2, this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The external source and the XCLK are synchronized to the bus clock by an on-chip synchronization circuit.
2:0 PS[2:0]	Prescale Divisor Select — This 3-bit field selects one of eight divisors for the TPM clock input as shown in Table B-3. This prescaler is located after any clock source synchronization or clock source selection, so it affects whatever clock source is selected to drive the TPM system.