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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Network Processor
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, I²C, IEEE 1284, LCD, PCI/CardBus, SPI, UART, USB
Number of I/O	50
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns9750b-a1-c125

features a PCI/CardBus port as well as a USB port for applications that require WLAN, external storage, or external sensors, imagers, or scanners. Four multi-function serial ports, an I^2C port, and 1284 parallel port provide a standard glueless interface to a variety of external peripherals. The NS9750B-A1 also features up to 50 general purpose I/O (GPIO) pins and highly-configurable power management with sleep mode.

NET+ARM processors are the foundation for the NET+Works® family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, operating systems, networking software, development tools, APIs, and complete development boards.

Using the NS9750B-A1 and associated Net+Works packages allows system designers to achieve dramatic time-to-market reductions with pre-integrated and tested NET+ARM hardware, NET+Works software, and tools. Product unit costs are reduced dramatically with a complete system-on-chip, including Ethernet, display support, a robust peripheral set, and the processing headroom to meet the most demanding applications. Customers save engineering resources, as no network development is required. Companies will reduce their design risk with a fully integrated and tested solution.

A complete NET+Works development package includes ThreadX™ picokernel RTOS, Green Hills™ MULTI® 2000 IDE or Microcross GNU X-Tools™, drivers, networking protocols and services with APIs, NET+ARM-based development board, Digi-supplied utilities, integrated file system, JTAG In Circuit Emulator (ICE), and support for boundary scan description language (BSDL). One year software maintenance and technical support is available.

bist_en_n, pll_test_n, and scan_en_n

Table 9 is a truth/termination table for bist_en_n, pll_test_n, and scan_en_n.

	Normal operation	Arm debug	
pll_test_n	pull up	pull up	10K recommended
bist_en_n	pull down	pull up	10K pullup = debug 2.4K pulldown = normal
scan_en_n	pull down	pull down	2.4K recommended

Table 9: bist_en_n, pll_test_n, & scan_en_n truth/termination table

PCI interface

The PCI interface can be set to PCI host or PCI device (slave) using the pci_central_resource_n pin.

Notes:

- All output drivers for PCI meet the standard PCI driver specification.
- All table notes can be found after Table 11: CardBus IO muxed signals.

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
J24	ad[0][1]		N/A	I/O	PCI time-multiplexed address/data bus
H26	ad[1][1]		N/A	I/O	PCI time-multiplexed address/data bus
J25	ad[2][1]		N/A	I/O	PCI time-multiplexed address/data bus
J26	ad[3][1]		N/A	I/O	PCI time-multiplexed address/data bus
K24	ad[4][1]		N/A	I/O	PCI time-multiplexed address/data bus
K25	ad[5][1]		N/A	I/O	PCI time-multiplexed address/data bus
K26	ad[6][1]		N/A	I/O	PCI time-multiplexed address/data bus
L24	ad[7][1]		N/A	I/O	PCI time-multiplexed address/data bus
L26	ad[8][1]		N/A	I/O	PCI time-multiplexed address/data bus
M24	ad[9][1]		N/A	I/O	PCI time-multiplexed address/data bus
M25	ad[10][1]		N/A	I/O	PCI time-multiplexed address/data bus
M26	ad[11][1]		N/A	I/O	PCI time-multiplexed address/data bus
N24	ad[12][1]		N/A	I/O	PCI time-multiplexed address/data bus
N25	ad[13][1]		N/A	I/O	PCI time-multiplexed address/data bus
N26	ad[14][1]		N/A	I/O	PCI time-multiplexed address/data bus
P26	ad[15][1]		N/A	I/O	PCI time-multiplexed address/data bus
U24	ad[16][1]		N/A	I/O	PCI time-multiplexed address/data bus

Table 10: PCI interface pinout

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
R26	serr_n[2]		N/A	I/O	System error: Input: pci_central_resource_n = 0 Output: pci_central_resource_n = 1
R24	stop_n[2]		N/A	I/O	Stop signal
T25	trdy_n[2]		N/A	I/O	Target ready
AC24	pci_arb_gnt_1_n[6]		N/A	O	PCI channel 1 grant
AD23	pci_arb_gnt_2_n[6]		N/A	O	PCI channel 2 grant
AE24	pci_arb_gnt_3_n[6]		N/A	O	PCI channel 3 grant
AD25	pci_arb_req_1_n[2]		N/A	I	PCI channel 1 request
AB23	pci_arb_req_2_n[2]		N/A	I	PCI channel 2 request
AC22	pci_arb_req_3_n[2]		N/A	I	PCI channel 3 request
AF23	pci_central_resource_n	D	N/A	I	PCI internal central resource enable
AF25	pci_int_a_n[2]		N/A	I/O	PCI interrupt request A, output if external central resource used
AF24	pci_int_b_n[2]		N/A	I/O	PCI interrupt request B, CCLKRUN# for CardBus applications
AE23	pci_int_c_n[2]		N/A	I	PCI interrupt request C
AD22	pci_int_d_n[2]		N/A	I	PCI interrupt request D
AE26	pci_reset_n[3]		N/A	I/O	PCI reset, output if internal central resource enabled
AB24	pci_clk_in	U	N/A	I	PCI clock in. (Connected to pci_clk_out or an externally generated PCI reference clock.)
AA23	pci_clk_out		N/A	O	PCI clock out

Table 10: PCI interface pinout

PCI/CardBus signals

Most of the CardBus signals are the same as the PCI signals. Other CardBus signals are unique and multiplexed with PCI signals for the NS9750B-A1. Table 11 shows these unique signals.

PCI signal	CardBus signal	CardBus type	Description
INTA#	CINT#[4]	Input	CardBus interrupt pin. The INTA2PCI pin in the PCI Miscellaneous Support register must be set to 0.
INTB#	CCLKRUN#[4]	Bidir	CardBus pin used to negotiate with the external CardBus device before stopping the clock. Allows external CardBus device to request that the clock be restarted.

Table 11: CardBus IO muxed signals

PCI signal	CardBus signal	CardBus type	Description
INTC#	CSTSCHG[5]	Input	CardBus status change interrupt signal.
GNT1#	CGNT#[4]	Output	Grant to external CardBus device from NS9750B-A1's internal arbiter.
GNT2#	CVS1	Output	Voltage sense pin. Normally driven low by NS9750B-A1, but toggled during interrogation of the external CardBus device to find voltage requirements. **Note:** Do not connect directly to the CardBus connector. See the diagram "CardBus system connections to NS9750B-A1" in the *NS9750B-A1 Hardware Reference.*
GNT3#	CVS2	Output	Voltage sense pin. Normally driven low by NS9750B-A1, but toggled during interrogation of the external CardBus device to find voltage requirements.
REQ1#	CREQ#[4]	Input	Request from external CardBus device to NS9750B-A1's internal arbiter.
REQ2#	CCD1[4]	Input	Card detect pin. Pulled up when the socket is empty and pulled low when the external CardBus device is in the socket.
REQ3#	CCD2[4]	Input	Card detect pin. Pulled up when the socket is empty and pulled low when the external CardBus device is in the socket.

Table 11: CardBus IO muxed signals

Notes:

1 Add external pulldown resistor or drive with the NS9750B-A1 *only* if the PCI interface is not being used. Figure 6, "NS9750B-A1 unused PCI termination," shows which signals can be driven by the NS9750B-A1 and which signals require pullups or pulldowns.

2 Add external pullup resistors *regardless* of whether the PCI interface is being used.

3 Add external pullup resistor *only* if the PCI interface is not being used.

4 Add external pullup resistor in CardBus mode.

5 Add external pulldown resistor in CardBus mode.

6 Add external pullup only if the PCI interface is being used and this signal is also being used.

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AD16	gpio[6]	U	2	I/O	00 Ser port B RI / SPI port B clk 01 1284 nFault (peripheral-driven)[1] 02 Timer 7 (duplicate) 03 GPIO 6
AE16	gpio[7]	U	2	I/O	00 Ser port B DCD / SPI port B enable 01 DMA ch 1 read enable (duplicate) 02 Ext IRQ 1 03 GPIO 7
AD15	gpio[8][1]	U	2	I/O	00 Ser port A TxData / SPI port A dout 01 Reserved 02 Reserved 03 GPIO 8
AE15	gpio[9]	U	2	I/O	00 Ser port A RxData / SPI port A din 01 Reserved 02 Timer 8 (duplicate) 03 GPIO 9
AF15	gpio[10][1]	U	2	I/O	00 Ser port A RTS 01 Reserved 02 Reserved 03: GPIO 10
AD14	gpio[11]	U	2	I/O	00 Ser port A CTS 01 Ext IRQ2 (duplicate) 02 Timer 0 (duplicate) 03 GPIO 11
AE14	gpio[12][1]	U	2	I/O	00 Ser port A DTR 01 Reserved 02 Reserved 03 GPIO 12
AF14	gpio[13]	U	2	I/O	00 Ser port A DSR 01 Ext IRQ 0 (duplicate) 02 Timer 10 (duplicate) 03 GPIO 13
AF13	gpio[14]	U	2	I/O	00 Ser port A RI / SPI port A clk 01 Timer 1 02 Reserved 03 GPIO 14
AE13	gpio[15]	U	2	I/O	00 Ser port A DCD / Ser port A enable 01 Timer 2 02 Reserved 03 GPIO 15

Table 12: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
AF5	gpio[36]	U	4	I/O	00	Reserved
					01	1284 Data 5 (bidirectional)
					02	LCD data bit 12
					03	GPIO 36
AD6	gpio[37]	U	4	I/O	00	Reserved
					01	1284 Data 6 (bidirectional)
					02	LCD data bit 13
					03	GPIO 37
AE5	gpio[38]	U	4	I/O	00	Reserved
					01	1284 Data 7 (bidirectional)
					02	LCD data bit 14
					03	GPIO 38
AF4	gpio[39]	U	4	I/O	00	Reserved
					01	1284 Data 8 (bidirectional)
					02	LCD data bit 15
					03	GPIO 39
AC6	gpio[40]	U	4	I/O	00	Ser port C TxData / SPI port C dout
					01	Ext IRQ 3
					02	LCD data bit 16
					03	GPIO 40
AD5	gpio[41]	U	4	I/O	00	Ser port C RxData / SPI port C din
					01	Timer 11
					02	LCD data bit 17
					03	GPIO 41
AE4	gpio[42]	U	4	I/O	00	Ser port C RTS
					01	Timer 12
					02	LCD data bit 18
					03	GPIO 42
AF3	gpio[43]	U	4	I/O	00	Ser port C CTS
					01	Timer 13
					02	LCD data bit 19
					03	GPIO 43
AD2	gpio[44][1]	U	4	I/O	00	Ser port D TxData / SPI port D dout
					01	1284 Select (peripheral-driven)
					02	LCD data bit 20
					03	GPIO 44
AE1	gpio[45]	U	4	I/O	00	Ser port D RxData / SPI port D din
					01	1284 nStrobe (host-driven)
					02	LCD data bit 21
					03	GPIO 45

Table 12: GPIO MUX pinout

Reserved pins

Pin#	Description
J1	Tie to ground directly
E2	Tie to ground directly
K3	Tie to ground directly
K2	Tie to ground directly
K1	Tie to ground directly
M2	Tie to ground directly
M1	Tie to ground directly
N1	Tie to ground directly
N2	Tie to ground directly
R1	Tie to ground directly
R2	Tie to ground directly
R3	Tie to ground directly
T1	Tie to ground directly
AD4	Tie to 1.5V core power
AF2	Tie to 3.3V I/O power
AE7	No connect
L3	No connect
B7	No connect
L2	No connect
L1	No connect
M3	No connect
AF6	Tie to ground directly
AC5	Tie to ground directly
AE3	Tie to ground directly
AF22	No connect
AD21	No connect
AE22	No connect

Table 20: Reserved pins

DC electrical characteristics

DC electrical characteristics specify the worst-case DC electrical performance of the I/O buffers that are guaranteed over the specified temperature range.

Inputs

All electrical inputs are 3.3V interface.

Note: V_{SS} = 0V (GND)

Sym	Parameter	Condition	Value		Unit
V_{IH}	High-level input voltage: LVTTL level PCI level		Min	 2.0 $0.5V_{DDA}$	 V V
V_{IL}	Low-level input voltage: LVTTL level PCI level		Max	 0.8 $0.3V_{DDA}$	 V V
I_{IH}	High-level input current (no pulldown) Input buffer with pulldown	$V_{INA}=V_{DDA}$	Min/Max Min/Max[1]	-10/10 10/200	µA µA
I_{IL}	Low-level input current (no pullup) Input buffer with pullup	$V_{INA}=V_{SS}$	Min/Max Min/Max[2]	-10/10 10/200	µA µA
I_{OZ}	High-impedance leakage current	$V_{OUTA}=V_{DDA}$ or V_{SS}	Min/Max	-10/10	µA
I_{DDS}	Quiescent supply current	$V_{INA}=V_{DDA}$ or V_{SS}	Max	TBD	

1. Min current = V_{IN-} or V_{IN} at 0.0V.
2. Min current = V_{IN-} or V_{IN} at 0.0V.

USB DC electrical inputs

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input high level (driven)	2.0	V_{DDA}-0.6	V	
V_{IZ}	Input high level (floating)	2.7	3.6	V	
V_{IL}	Input low level		0.8	V	
V_{DI}	Differential input sensitivity	0.2		V	1
V_{CM}	Differential common mode range	0.8	2.5	V	2

Notes:

1 |(usb_dp) - (usb_dm)|

2 Includes V_{DI} range.

Outputs

All electrical outputs are 3.3V interface.

Sym	Parameter	Value		Unit
V_{OH}	High-level output voltage (LVTTL)	Min	V_{DDA}-0.6	V
V_{OL}	Low-level output voltage (LVTTL)	Max	0.4	V
V_{OH}	PCI high-level output voltage	Min	$0.9V_{DDA}$	V
V_{OL}	PCI low-level output voltage	Max	$0.1V_{DDA}$	V

USB DC electrical outputs

Symbol	Parameter	Min	Max	Units	Notes
V_{OL}	Output low level	0.0	0.3	V	1
V_{OH}	Output high level	2.8	3.6	V	2
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	3

Notes:

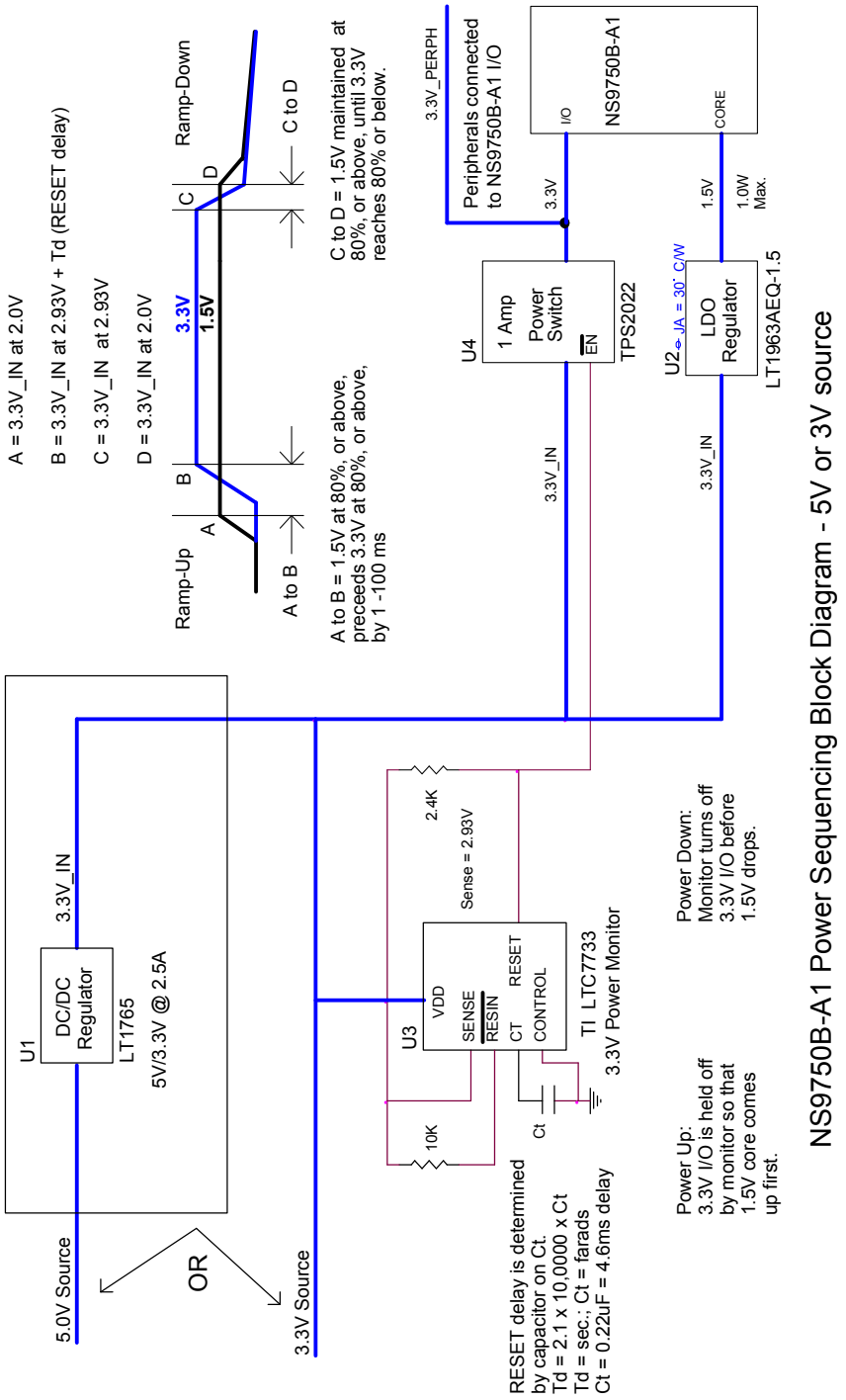
1 Measured with R_L of 1.425k ohm to 3.6V.

2 Measured with R_L of 14.25k ohm to GND.

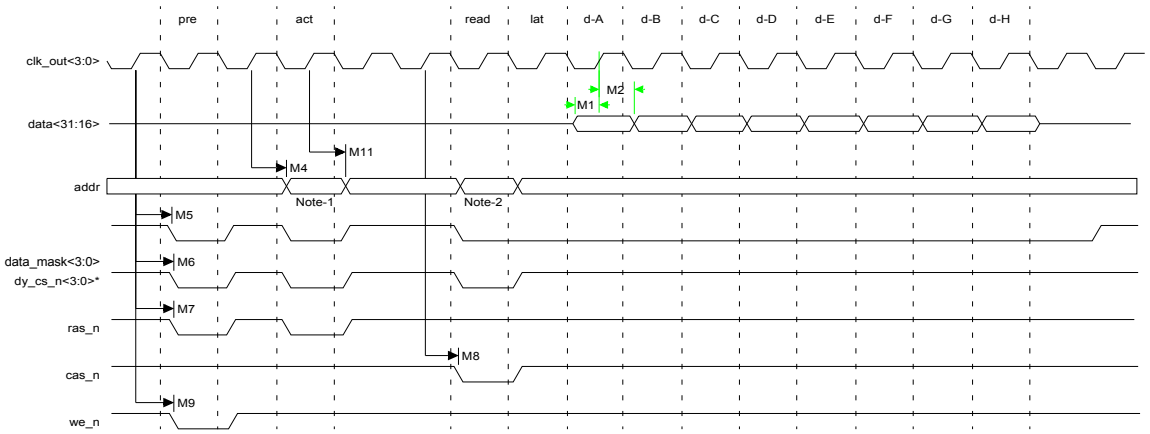
3 Excluding the first transition from the idle state.

Power sequencing

Use these requirements for power sequencing.



SDRAM burst read (16-bit)

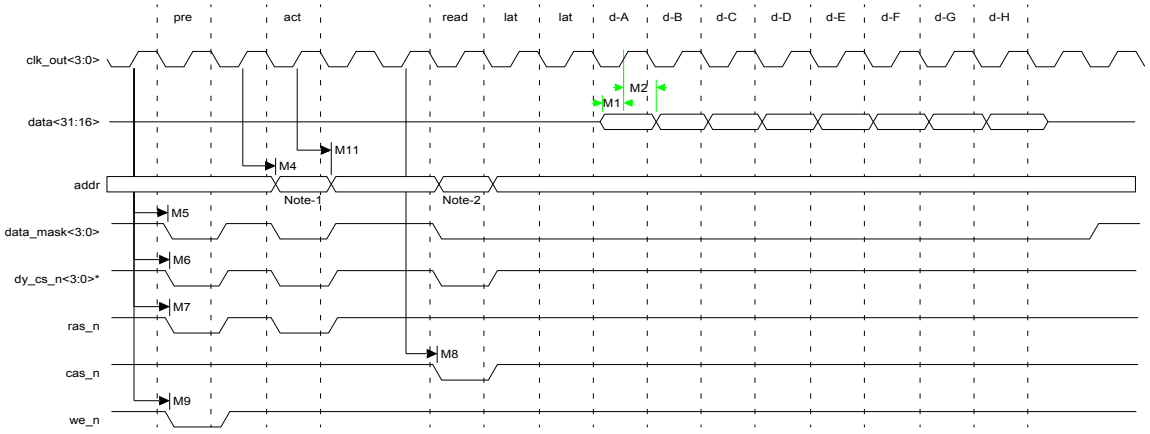


Notes:

1 This is the bank and RAS address.

2 This is the CAS address

SDRAM burst read (16-bit), CAS latency = 3



Notes:

1 This is the bank and RAS address.

2 This is the CAS address

Slow peripheral acknowledge timing

Table 28 describes the values shown in the slow peripheral acknowledge timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M15	clock high to data out valid		+2	ns	
M16	data out hold time from clock high	-2		ns	
M17	clock high to address valid		+2	ns	
M18	address hold time from clock high	-2		ns	
M19	clock high to st_cs_n low		+2	ns	1
M20	clock high to st_cs_n high		+2	ns	1
M21	clock high to we_n low		+2	ns	
M22	clock high to we_n high		+2	ns	
M23	clock high to byte_lanes low		+2	ns	
M24	clock high to byte_lanes high		+2	ns	
M26	data input hold time to rising clk	4.5		ns	
M27	clock high to oe_n low		+2	ns	
M28	clock high to oe_n high		+2	ns	
M29	address/chip select valid to ta_strb high	2		CPU cycles	
M30	ta_strb pulse width	4	8	CPU cycles	
M31	ta_strb rising to chip select/address change	4	10	CPU cycles	
M32	data setup to ta_strb rising	0		ns	

Table 28: Slow peripheral acknowledge

Note:

1 Only one of the four st_cs_n signals is used. The diagrams show the active low configuration, which can be reversed (active high) with the PC field.

Ethernet timing

Ethernet AC characteristics are measured with 10pF, unless otherwise noted.

Table 29 describes the values shown in the Ethernet timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
E1	MII tx_clk to txd, tx_en, tx_er	3	11	ns	2
E2	MII rxd, rx_dv, rx_er setup to rx_clk rising	3		ns	
E3	MII rxd, rx_dv, rx_er hold from rx_clk rising	1		ns	
E4	mdio (input) setup to mdc rising	10		ns	
E5	mdio (input) hold from mdc rising	0		ns	
E6	mdc to mdio (output)	18	38	ns	1, 2
E7	mdc period	80		ns	
E8	RMII ref_clk to txd, tx_en	3	12	ns	2
E9	RMII rxd, crs, rx_er setup to ref_clk rising	3		ns	
E10	RMII rxd, crs, rx_er hold from ref_clk rising	1		ns	
E11	MII rx_clk to cam_req	3	10	ns	
E12	MII cam_reject setup to rx_clk rising	N/A		ns	3
E13	MII cam_reject hold from rx_clk rising	N/A		ns	3

Table 29: Ethernet timing characteristics

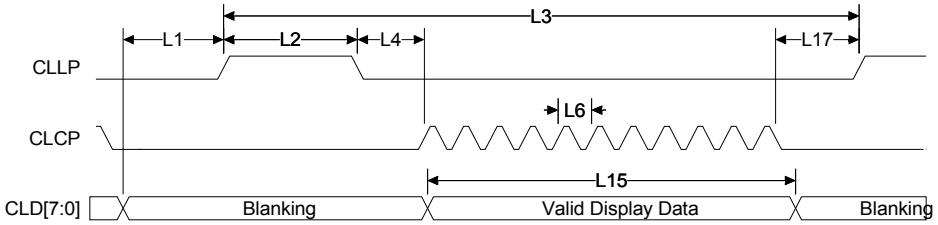
Notes:

1 Minimum specification is for fastest AHB bus clock of 100 MHz. Maximum specification is for slowest AHB bus clock of 50 MHz.

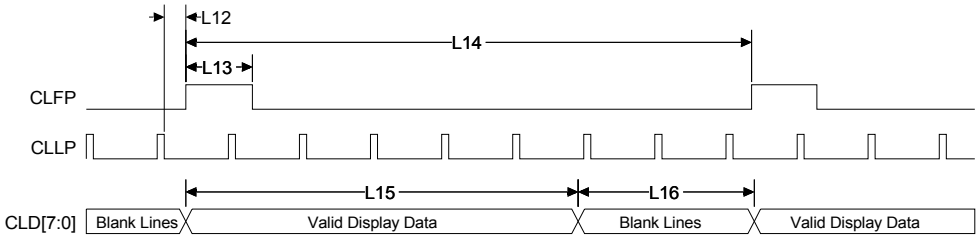
2 C_{load} = 10pF for all outputs and bidirects.

3 No setup and hold requirements for cam_reject because it is an asynchronous input. This is also true for RMII PHY applications.

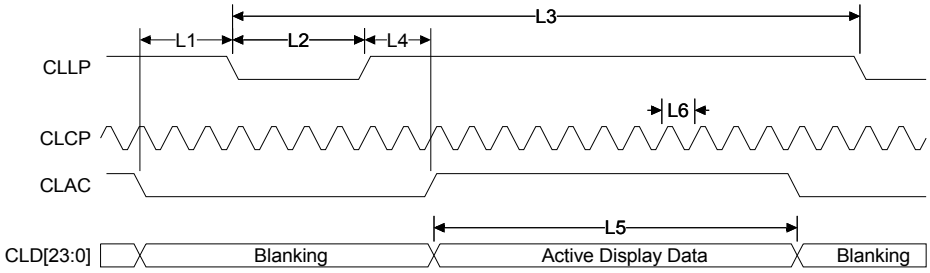
Horizontal timing for STN displays



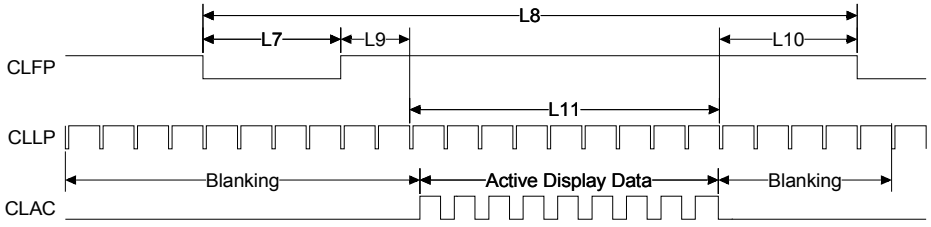
Vertical timing for STN displays



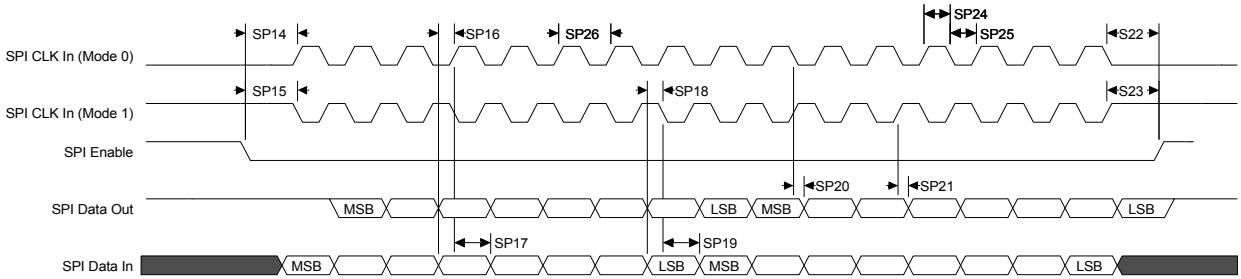
Horizontal timing for TFT displays



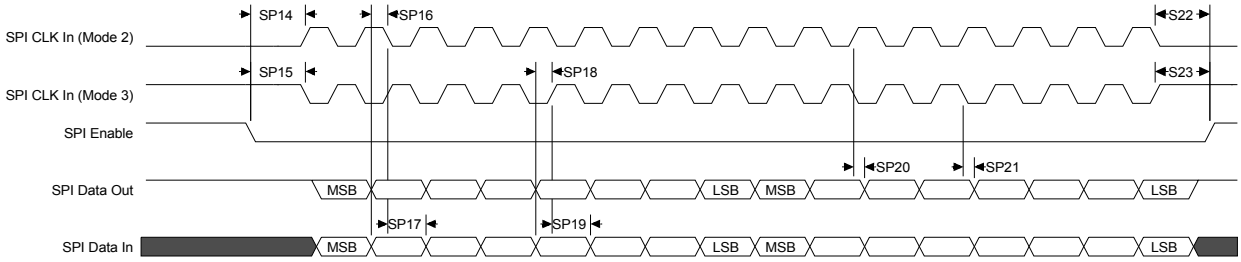
Vertical timing for TFT displays



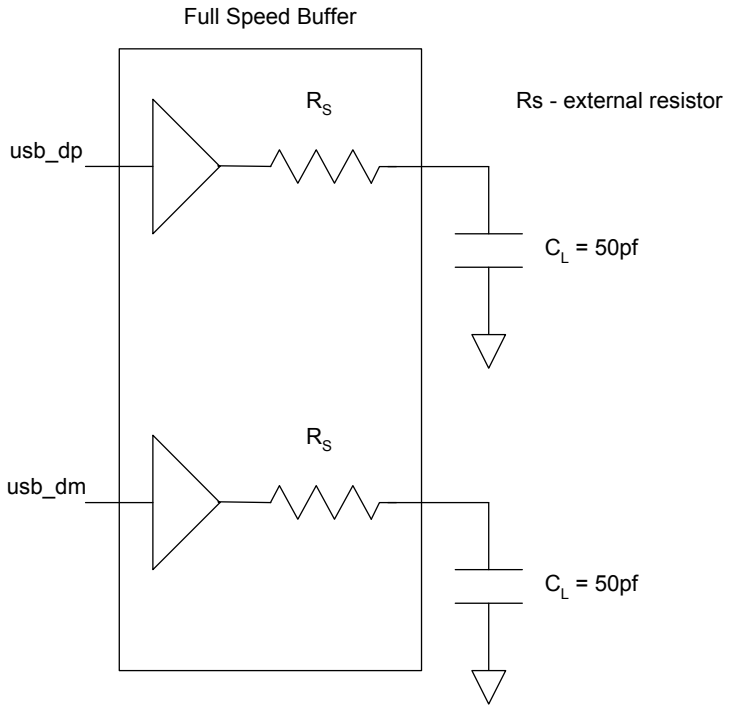
SPI slave mode 0 and 1: 2-byte transfer (see note 7)



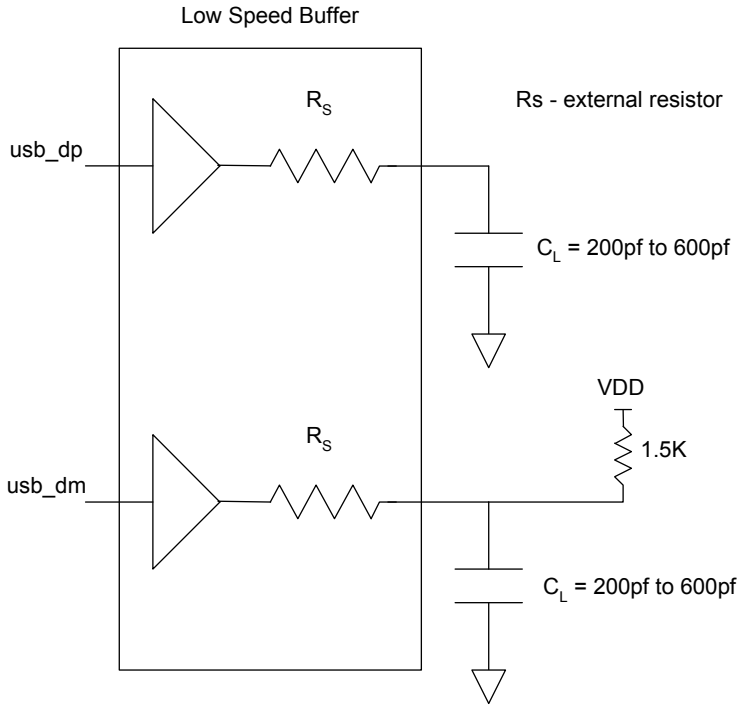
SPI slave mode 2 and 3: 2-byte transfer (see note 7)



USB full speed load



USB low speed load



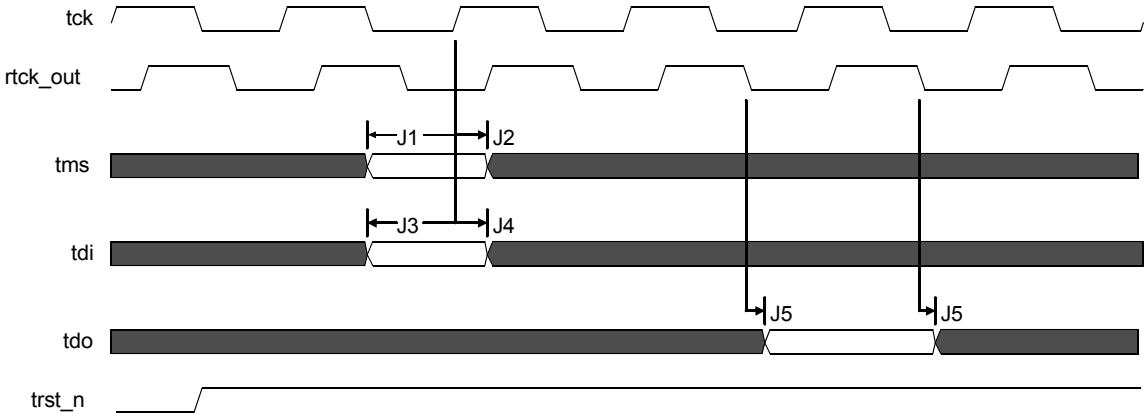
JTAG timing

JTAG AC characteristics are measured with 10pF, unless otherwise noted.

Table 39 describes the values shown in the JTAG timing diagram.

Parameter	Description	Min	Max	Unit
J1	tms (input) setup to tck rising	5		ns
J2	tms (input) hold to tck rising	2		ns
J3	tdi (input) setup to tck rising	5		ns
J4	tdi (input) hold to tck rising	2		ns
J5	tdo (output) to tck falling	2.5	10	ns

Table 39: JTAG timing parameters



Notes:

1 Maximum tck rate is 10 MHz.

2 rtck_out is an asynchronous output, driven off of the CPU clock.

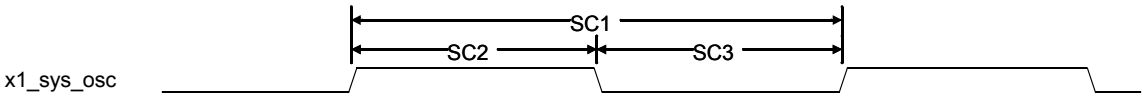
3 trst_n is an asynchronous input.

System PLL reference clock timing

Table 42 describes the values shown in the system PLL reference clock timing diagram.

Parameter	Description	Min	Max	Unit
SC1	x1_sys_osc cycle time	25	50	ns
SC2	x1_sys_osc high time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns
SC3	x1_sys_osc low time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns

Table 42: System PLL reference clock timing parameters



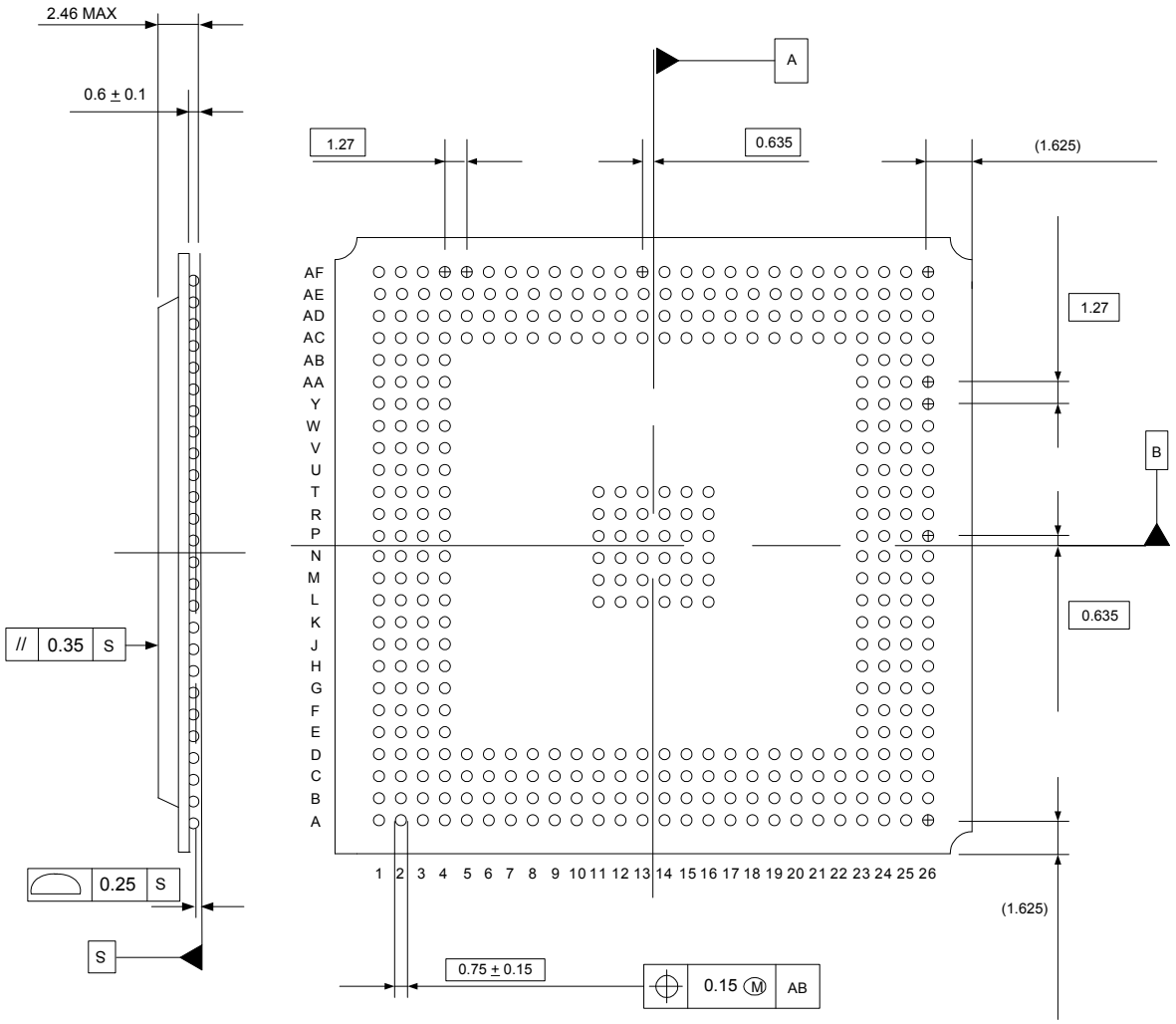


Figure 9: NS9750B-A1 bottom and side view