Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, I²C, IEEE 1284, LCD, PCI/CardBus, SPI, UART, USB
Number of I/O	50
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	388-BBGA
Supplier Device Package	388-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns9750b-a1-c200

4 The memory controller settings are read from the serial EEPROM and used to initialize the memory controller.

5 The BBus-to-AHB bridge loads the boot program into the SDRAM, starting at address 0.

6 The reset signal going to the CPU is released once the boot program is loaded. RESET_DONE is now set to 1.

7 The CPU begins to execute code from address 0x0000 0000.

You can use one of these software resets to reset the NS9750B-A1. Select the reset by setting the appropriate bit in the appropriate register:

- Watchdog timer can issue reset upon Watchdog timer expiration.
- Software reset can reset individual internal modules or all modules except memory and CPU.
- The system is reset whenever software sets the PLL SW change bit to 1.

Hardware reset duration is 4ms for PLL to stabilize. Software reset duration depends on speed grade, as shown in Table 3.

Speed grade	CPU clock cycles	Duration
200 MHz	128	640 ns
162 MHz	128	790 ns
125 MHz	128	1024 ns

Table 3: Software reset duration

The minimum reset pulse width is 10 crystal clocks.

System Clock

The system clock reference is provided to the NS9750B-A1 by an external oscillator; Table 4 shows sample clock frequency settings for each chip speed grade.

Speed	cpu_clk	hclk (main bus)	bbus_clk
200 MHz	200 (199.0656)	99.5328	49.7664
162 MHz	162.2016	81.1008	40.5504
125 MHz	125.3376	62.6688	31.3344

Table 4: Sample clock frequency settings with 29.4912 MHz oscillator

The oscillator must be connected to the x1_sys_osc input (C8 pin) on the NS9750B-A1, as shown in Figure 2.

Pin #	Signal Name	U/D	OD (mA)	I/O	Description
F4	byte_lane_sel_n[1]		8	O	Static memory byte_lane_enable[1] or write_enable_n[1] for byte-wide device signals
D1	byte_lane_sel_n[2]		8	O	Static memory byte_lane_enable[2] or write_enable_n[2] for byte-wide device signals
F3	byte_lane_sel_n[3]		8	O	Static memory byte_lane_enable[3] or write_enable_n[3] for byte-wide device signals
B5	cas_n		8	O	SDRAM column address strobe
A8	dy_cs_n[0]		8	O	SDRAM chip select signal
B8	dy_cs_n[1]		8	O	SDRAM chip select signal
A6	dy_cs_n[2]		8	O	SDRAM chip select signal
C7	dy_cs_n[3]		8	O	SDRAM chip select signal
C6	st_oe_n		8	O	Static memory output enable
D6	ras_n		8	O	SDRAM row address strobe
H1	dy_pwr_n		8	O	SyncFlash power down
B10	st_cs_n[0]		8	O	Static memory chip select signal
C10	st_cs_n[1]		8	O	Static memory chip select signal
B9	st_cs_n[2]		8	O	Static memory chip select signal
C9	st_cs_n[3]		8	O	Static memory chip select signal
B6	we_n		8	O	SDRAM write enable. Used for static and SDRAM devices.
J3	ta_strb	U		I	Slow peripheral transfer acknowledge

Table 5: System Memory interface pinout

Clock generation/system pins

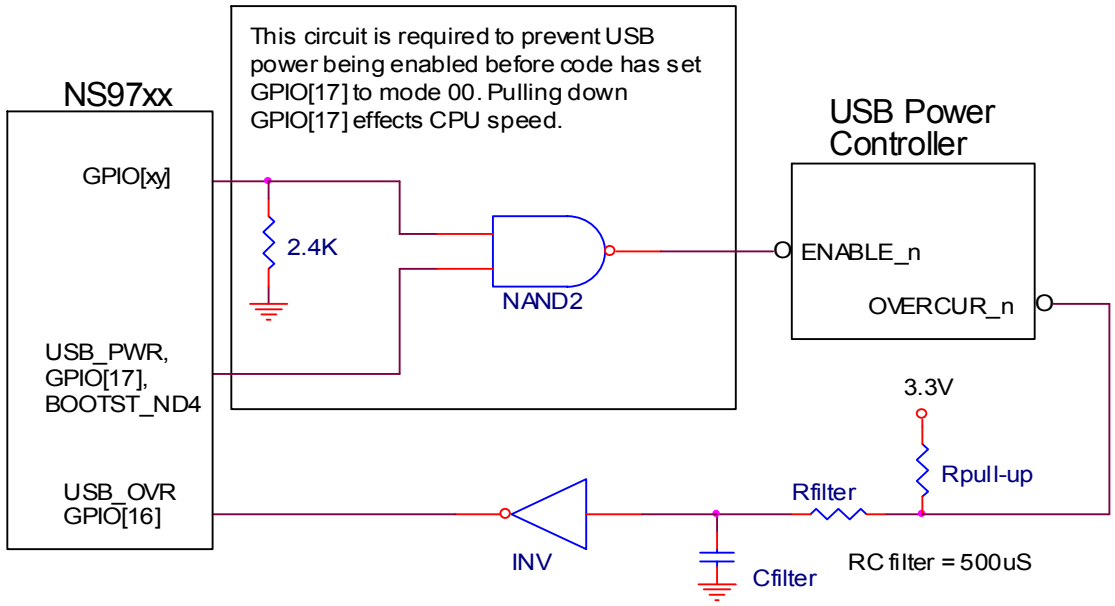
Pin #	Signal name	U/D	OD (mA)	I/O	Description
C8	x1_sys_osc			I	System clock oscillator circuit input
D9	x1_usb_osc			I	USB clock crystal oscillator circuit input. (Connect to GND if USB is not used.)
A7	x2_usb_osc			O	USB clock crystal oscillator circuit output
AC21	reset_done	U	2	I/O	CPU is enabled once the boot program is loaded. Reset_done is set to 1.
H25	reset_n	U		I	System reset input signal.
AD20	bist_en_n			I	Enable internal BIST operation
AF21	pll_test_n			I	Enable PLL testing
AE21	scan_en_n			I	Enable internal scan testing
B18	sys_pll_dvdd				System clock PLL 1.5V digital power
A18	sys_pll_dvss				System clock PLL digital ground
B17	sys_pll_avdd				System clock PLL 3.3V analog power
C17	sys_pll_avss				System clock PLL analog ground
J2	lcdclk	U		I	External LCD clock input
D2	sreset_n			I	System reset. sreset_n is the same as reset, but does not reset the system PLL.
E3	sreset_n_enable			I	■ Tie to 3.3V to enable the sreset_n input. ■ Tie to ground to disable the sreset_n input.
T2	boot_strap[0]	U	2	I/O	Chip select 1 static memory byte_lane_enable_n, or write_enable_n for byte-wide devices bootstrap select
N3	boot_strap[1]	U	2	I/O	CardBus mode bootstrap select
P1	boot_strap[2]	U	2	I/O	Memory interface read mode bootstrap select
P2	boot_strap[3]	U	2	I/O	Chip select 1 data width bootstrap select
P3	boot_strap[4]	U	2	I/O	Chip select 1 data width bootstrap select

Table 8: Clock generation/system pins pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
AD16	gpio[6]	U	2	I/O	00 Ser port B RI / SPI port B clk 01 1284 nFault (peripheral-driven)[1] 02 Timer 7 (duplicate) 03 GPIO 6
AE16	gpio[7]	U	2	I/O	00 Ser port B DCD / SPI port B enable 01 DMA ch 1 read enable (duplicate) 02 Ext IRQ 1 03 GPIO 7
AD15	gpio[8][1]	U	2	I/O	00 Ser port A TxData / SPI port A dout 01 Reserved 02 Reserved 03 GPIO 8
AE15	gpio[9]	U	2	I/O	00 Ser port A RxData / SPI port A din 01 Reserved 02 Timer 8 (duplicate) 03 GPIO 9
AF15	gpio[10][1]	U	2	I/O	00 Ser port A RTS 01 Reserved 02 Reserved 03: GPIO 10
AD14	gpio[11]	U	2	I/O	00 Ser port A CTS 01 Ext IRQ2 (duplicate) 02 Timer 0 (duplicate) 03 GPIO 11
AE14	gpio[12][1]	U	2	I/O	00 Ser port A DTR 01 Reserved 02 Reserved 03 GPIO 12
AF14	gpio[13]	U	2	I/O	00 Ser port A DSR 01 Ext IRQ 0 (duplicate) 02 Timer 10 (duplicate) 03 GPIO 13
AF13	gpio[14]	U	2	I/O	00 Ser port A RI / SPI port A clk 01 Timer 1 02 Reserved 03 GPIO 14
AE13	gpio[15]	U	2	I/O	00 Ser port A DCD / Ser port A enable 01 Timer 2 02 Reserved 03 GPIO 15

Table 12: GPIO MUX pinout

Example: Implementing gpio[16] and gpio[17]



LCD module signals

The LCD module signals are multiplexed with GPIO pins. They include seven control signals and up to 24 data signals. Table 13 describes the control signals. Table 14 and Table 15 provide details for the data signals.

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN) / horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN) / vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLD[23:0]	Output	LCD panel data (see Table 14 and Table 15)
CLLE	Output	Line end signal

Table 13: LCD module signal descriptions

The CLD[23:0] signal has eight modes of operation:

- TFT 24-bit interface
- TFT 18-bit interface
- Color STN single panel
- Color STN dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel

Table 14 shows which CLD[23:0] pins provide the pixel data to the STN panel for each mode of operation.

Legend:

- Ext pin = External pin
- CUSTN = Color upper panel STN, dual and/or single panel
- CLSTN = Color lower panel STN, single
- MUSTN = Mono upper panel STN, dual and/or single panel
- MLSTN = Mono lower panel STN, single
- N/A = not used
- 01 and 02 = The option number/position in the Description field of the GPIO mux pinout. See “GPIO MUX” on page 26 for more information.

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[23]	AA4=LCD data bit 23 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[22]	AB3=LCD data bit 22 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[21]	AE1=LCD data bit 21 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[20]	AD2=LCD data bit 20 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[19]	AF3=LCD data bit 19 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[18]	AE4=LCD data bit 18 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[17]	AD5=LCD data bit 17 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[16]	AC6=LCD data bit16 (O2)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[15]	AF4=LCD data bit 15 (O2)	N/A	CLSTN[0][1]	N/A	N/A	N/A	MLSTN[0][1]
CLD[14]	AE5=LCD data bit 14 (O2)	N/A	CLSTN[1]	N/A	N/A	N/A	MLSTN[1]
CLD[13]	AD6=LCD data bit 13 (O2)	N/A	CLSTN[2]	N/A	N/A	N/A	MLSTN[2]
CLD[12]	AF5=LCD data bit 12 (O2)	N/A	CLSTN[3]	N/A	N/A	N/A	MLSTN[3]

Table 14: CLD[23:0] pin descriptions for STN display

External pin	TFT 24 bit	TFT 15 bit
CLD[15]	GREEN[7]	BLUE[2]
CLD[14]	GREEN[6]	BLUE[1]
CLD[13]	GREEN[5]	BLUE[0]
CLD[12]	GREEN[4]	Intensity bit
CLD[11]	GREEN[3]	GREEN[4]
CLD[10]	GREEN[2]	GREEN[3]
CLD[9]	GREEN[1]	GREEN[2]
CLD[8]	GREEN[0]	GREEN[1]
CLD[7]	RED[7]	GREEN[0]
CLD[6]	RED[6]	Intensity bit
CLD[5]	RED[5]	RED[4]
CLD[4]	RED[4]	RED[3]
CLD[3]	RED[3]	RED[2]
CLD[2]	RED[2]	RED[1]
CLD[1]	RED[1]	RED[0]
CLD[0]	RED[0]	Intensity bit

Table 15: CLD[23:0] pin descriptions for TFT display

This LCD TFT panel signal multiplexing table shows the RGB alignment to a 15-bit TFT with the intensity bit not used. The intensity bit, if used, should be connected to the LSB (that is, RED[0], GREEN[0], BLUE[0]) input of an 18-bit LCD TFT panel as shown in the next table.

	4	3	2	1	0	Intensity
18-bit TFT	5	4	3	2	1	0
15-bit TFT	4	3	2	1	0	x
12-bit TFT	3	2	1	0	x	x
9-bit TFT	2	1	0	x	x	x

Table 16: RGB bit alignment according to TFT interface size (one color shown)

If you want reduced resolution, the least significant color bits can be dropped, starting with Red[0], Green[0], and Blue[0].

Reserved pins

Pin#	Description
J1	Tie to ground directly
E2	Tie to ground directly
K3	Tie to ground directly
K2	Tie to ground directly
K1	Tie to ground directly
M2	Tie to ground directly
M1	Tie to ground directly
N1	Tie to ground directly
N2	Tie to ground directly
R1	Tie to ground directly
R2	Tie to ground directly
R3	Tie to ground directly
T1	Tie to ground directly
AD4	Tie to 1.5V core power
AF2	Tie to 3.3V I/O power
AE7	No connect
L3	No connect
B7	No connect
L2	No connect
L1	No connect
M3	No connect
AF6	Tie to ground directly
AC5	Tie to ground directly
AE3	Tie to ground directly
AF22	No connect
AD21	No connect
AE22	No connect

Table 20: Reserved pins

Electrical characteristics

The NS9750B-A1 operates at a 1.5V core, with 3.3V I/O ring voltages.

Absolute maximum ratings

Permanent device damage can occur if the absolute maximum ratings are exceeded even for an instant.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +3.9	V
DC input voltage	V_{INA}	-0.3 to V_{DDA}+0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA}+0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	-40 to +125	^{o}C

† V_{DDA}, V_{INA}, V_{OUTA}: Ratings of I/O cells for 3.3V interface

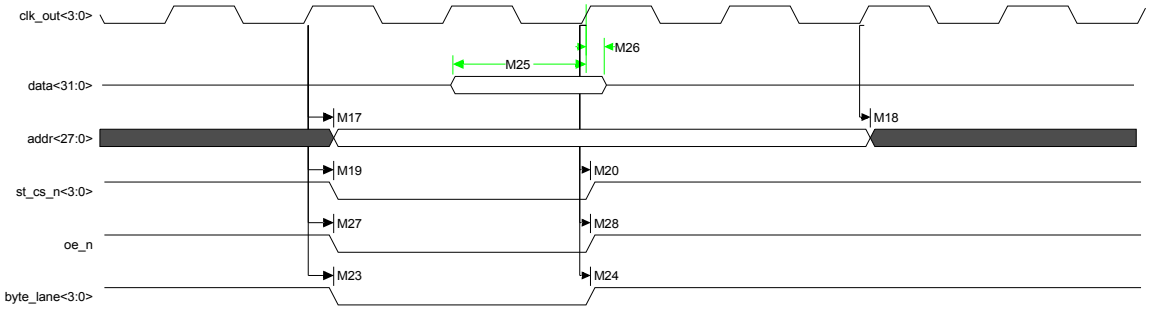
Recommended operating conditions

Recommended operating conditions specify voltage and temperature ranges over which a circuit's correct logic function is guaranteed. The specified DC electrical characteristics (see "DC electrical characteristics" on page 43) are satisfied over these ranges.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	3.0 to 3.6	V
	V_{DDC} (core)	1.4 to 1.6	V
	V_{DDC} (PLL)	1.425 to 1.575	V
Maximum junction temperature	T_J	125	^{o}C

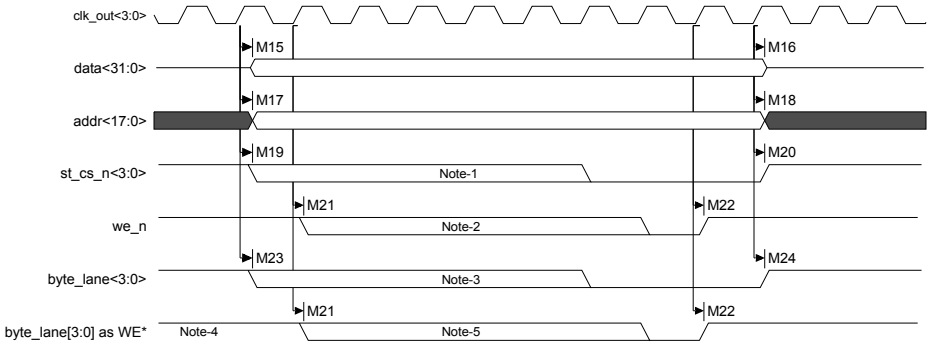
† V_{DDA}: Ratings of I/O cells for 3.3V interface
V_{DDC}: Ratings of internal cells

Static RAM read cycles with 1 wait state



- WTRD = 1
  WOEN = 0
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the byte_lane signal will always be high.

Static write cycle with configurable wait states



- WTWR = from 0 to 15
  WWEN = from 0 to 15
- The WTWR field determines the length on the write cycle.
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Notes:

1 Timing of the st_cs_n signal is determined with a combination of the WTWR and WWEN fields. The st_cs_n signal will always go low at least one clock before we_n goes low, and will go high one clock after we_n goes high.

2 Timing of the we_n signal is determined with a combination of the WTWR and WWEN fields.

3 Timing of the byte_lane signals is determined with a combination of the WTWR and WWEN fields. The byte_lane signals will always go low one clock before we_n goes low, and will go one clock high after we_n goes high.

4 If the PB field is set to 0, the byte_lane signals will function as the write enable signals and the we_n signal will always be high.

5 If the PB field is set to 0, the timing for the byte_lane signals is set with the WTWR and WWEN fields.

Slow peripheral acknowledge timing

Table 28 describes the values shown in the slow peripheral acknowledge timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M15	clock high to data out valid		+2	ns	
M16	data out hold time from clock high	-2		ns	
M17	clock high to address valid		+2	ns	
M18	address hold time from clock high	-2		ns	
M19	clock high to st_cs_n low		+2	ns	1
M20	clock high to st_cs_n high		+2	ns	1
M21	clock high to we_n low		+2	ns	
M22	clock high to we_n high		+2	ns	
M23	clock high to byte_lanes low		+2	ns	
M24	clock high to byte_lanes high		+2	ns	
M26	data input hold time to rising clk	4.5		ns	
M27	clock high to oe_n low		+2	ns	
M28	clock high to oe_n high		+2	ns	
M29	address/chip select valid to ta_strb high	2		CPU cycles	
M30	ta_strb pulse width	4	8	CPU cycles	
M31	ta_strb rising to chip select/address change	4	10	CPU cycles	
M32	data setup to ta_strb rising	0		ns	

Table 28: Slow peripheral acknowledge

Note:

1 Only one of the four st_cs_n signals is used. The diagrams show the active low configuration, which can be reversed (active high) with the PC field.

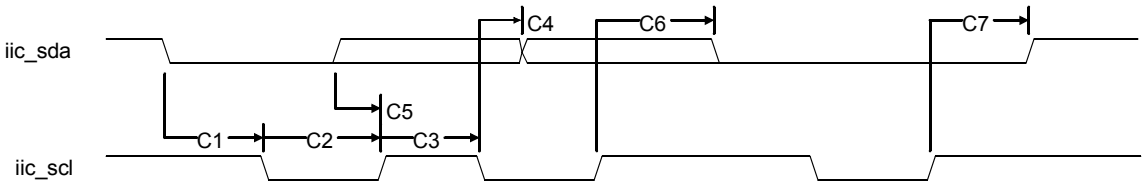
I²C timing

I²C AC characteristics are measured with 10pF, unless otherwise noted.

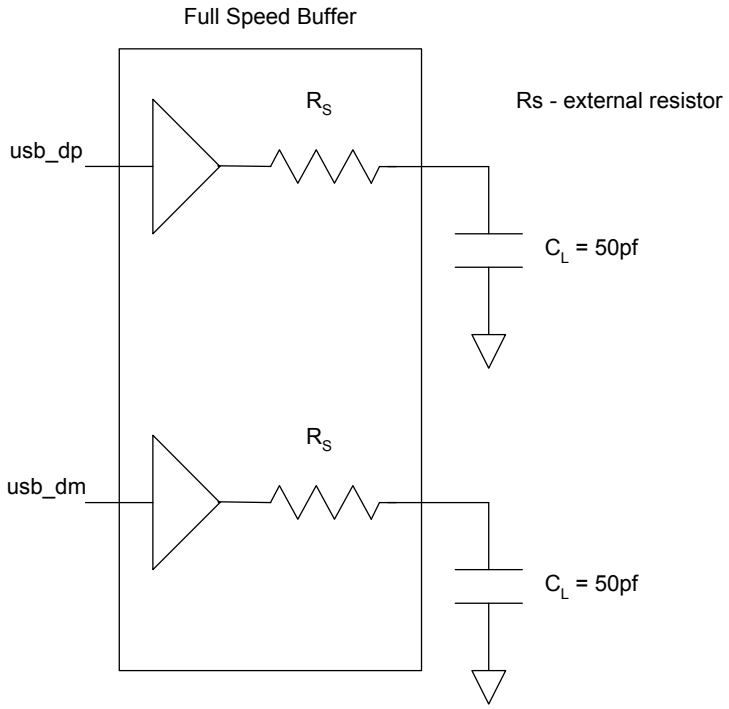
Table 32 describes the values shown in the I²C timing diagram.

		Standard mode		Fast mode		
Parm	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
C1	iic_sda to iic_scl START hold time	4.0		0.6		µs
C2	iic_scl low period	4.7		1.3		µs
C3	iic_scl high period	4.7		1.3		µs
C4	iic_scl to iic_sda DATA hold time	0		0		µs
C5	iic_sda to iic_scl DATA setup time	250		100		ns
C6	iic_scl to iic_sda START setup time	4.7		0.6		µs
C7	iic_scl to iic_sda STOP setup time	4.0		0.6		µs

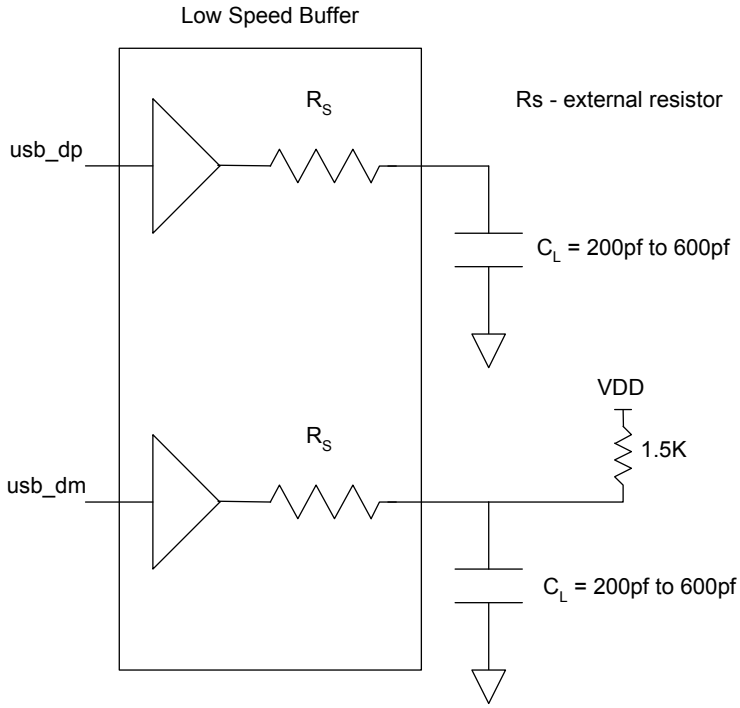
Table 32: I²C timing parameters



USB full speed load



USB low speed load



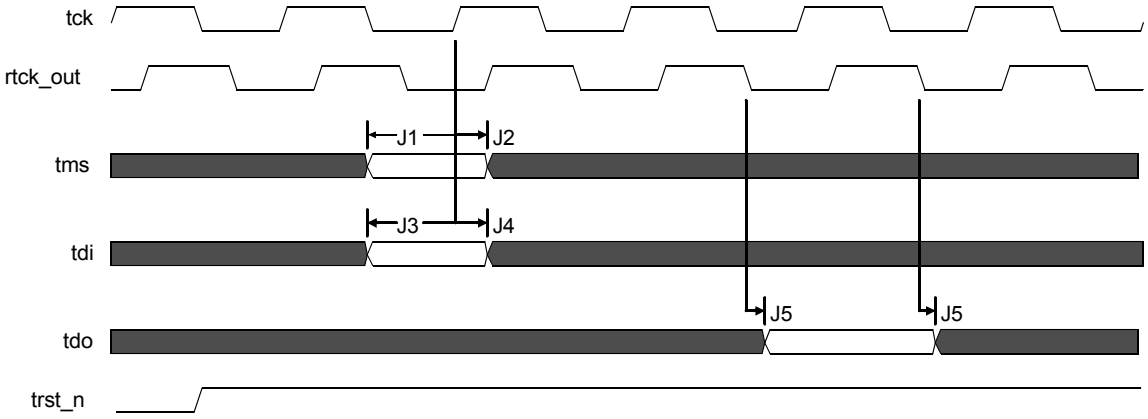
JTAG timing

JTAG AC characteristics are measured with 10pF, unless otherwise noted.

Table 39 describes the values shown in the JTAG timing diagram.

Parameter	Description	Min	Max	Unit
J1	tms (input) setup to tck rising	5		ns
J2	tms (input) hold to tck rising	2		ns
J3	tdi (input) setup to tck rising	5		ns
J4	tdi (input) hold to tck rising	2		ns
J5	tdo (output) to tck falling	2.5	10	ns

Table 39: JTAG timing parameters



Notes:

1 Maximum tck rate is 10 MHz.

2 rtck_out is an asynchronous output, driven off of the CPU clock.

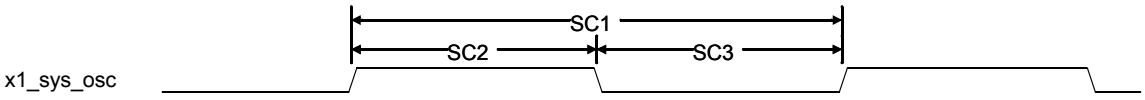
3 trst_n is an asynchronous input.

System PLL reference clock timing

Table 42 describes the values shown in the system PLL reference clock timing diagram.

Parameter	Description	Min	Max	Unit
SC1	x1_sys_osc cycle time	25	50	ns
SC2	x1_sys_osc high time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns
SC3	x1_sys_osc low time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns

Table 42: System PLL reference clock timing parameters



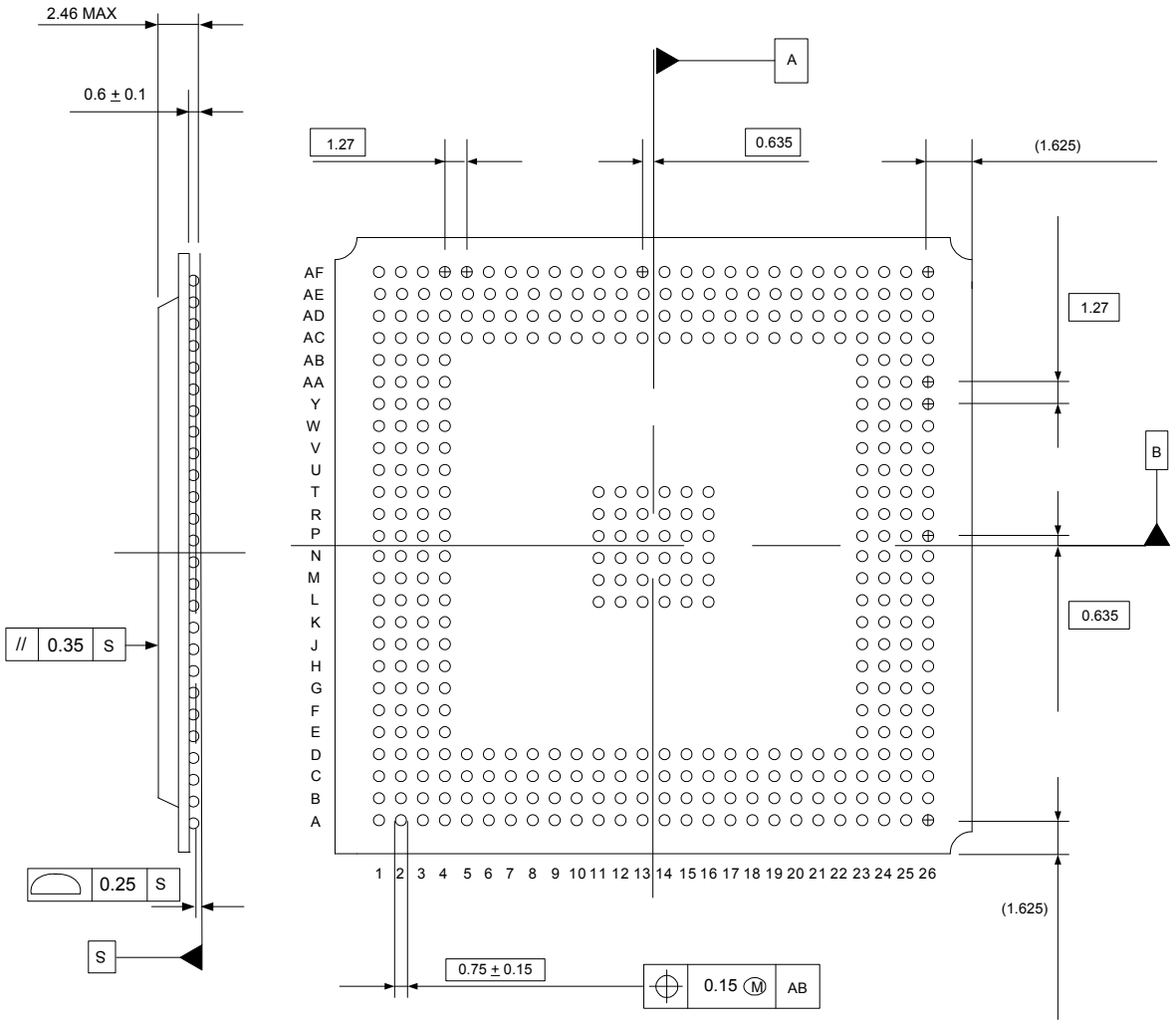


Figure 9: NS9750B-A1 bottom and side view

Product specifications

These tables provide additional information about the NS9750B-A1.

ROHS substance	PPM level
Lead	0
Mercury	0
Cadmium	0
Hexavalent Chromium	0
Polybrominated biphenyls	0
Polybrominated diphenyl ethers	0

Table 43: RoHS specifications

Component	Weight [mg]	Material		Weight [mg]	Weight [%]
		CAS no.	Name		
Chip	27.037	7440-21-3	Si	27.0370	0.61
Frame	1841.616	223769-10-6	Epoxy resin	865.5600	19.71
		7440-50-8	Cu	736.6500	16.77
		7440-02-0	Ni	9.2100	0.21
		7440-57-5	Au	1.8400	0.04
			Other	228.3560	5.20
Bonding wire	6.990	7440-57-5	Au	6.9900	0.16
Ag paste	3.400	7440-22-4	Ag	2.6200	0.06
			Epoxy, other	0.7800	0.02
Epoxy resin	1920.177	60676-86-0	Silica (SiO2)	1747.3570	39.79
			Epoxy, other	86.4100	1.97
			Phenol Resin	86.4100	1.97
		CAS no.	Name		
Solder ball	592.400	7440-31-5	Sn	571.6700	13.02
		7440-22-4	Ag	17.7700	0.40
		7440-50-8	Cu	2.9600	0.07
Total weight	4985.021				

Digi International
11001 Bren Road East
Minnetonka, MN 55343 U.S.A.
United States: +1 877 912-3444
Other locations: +1 952 912-3444
Fax: +1 952 912-4960
www.digi.com/support
www.digi.com

P/N: 91001324_B

Release date: March 2006