Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	50MHz
Connectivity	EBI/EMI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10r172lt1

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Symbol	Pin Number (TQFP)	Input (I) Output (O)	Kind[1)]	Function		
P5.10	98-100	I	5S	6-bit input-only port with Schmitt-Trigger characteristics. Port 5 pins also serve as timer inputs:		
–P5.15	1- 3	I	5S			
	98	I	5S	P5.10	T6EUD	GPT2 Timer T6 Ext.Up/Down Ctrl.Input
	99	I	5S	P5.11	T5EUD	GPT2 Timer T5 Ext.Up/Down Ctrl.Input
	100	I	5S	P5.12	T6IN	GPT2 Timer T6 Count Input
	1	I	5S	P5.13	T5IN	GPT2 Timer T5 Count Input
	2	I	5S	P5.14	T4EUD	GPT1 Timer T4 Ext.Up/Down Ctrl.Input
	3	I	5S	P5.15	T2EUD	GPT1 Timer T2 Ext.Up/Down Ctrl.Input
XTAL1	5	I	3T	XTAL1:	Input to the oscillator amplifier and internal clock generator	
XTAL2	6	O	3T	XTAL2:	Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Observe minimum and maximum high/low and rise/fall times specified in the AC Characteristics.	

Table 1 Pin definitions

Symbol	Pin Number (TQFP)	Input (I) Output (O)	Kind[1)]	Function		
P4.0–P4.7	23-26 29-32-	I/O	5T	An 8-bit bidirectional I/O port. Port 8 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines for external bus configuration.		
	23	O	5T	P4.0	A16	Least Significant Segment Addr. Line
	...	...	...	...	...	...
	26	O	5T	P4.3	A19	Segment Address Line
	29	O	5T	P4.4	A20	Segment Address Line
		O	5T		SSPCE1	Chip Enable Line 1
	30	O	5T	P4.5	A21	Segment Address Line
		O	5T		SSPCE0	SSPChip Enable Line 0
	31	O	5T	P4.6	A22	Segment Address Line
		I/O	5T		SSPDAT	SSP Data Input/Output Line
	32	O	5T	P4.7	A23	Most Significant Segment Addr. Line
		O	5T		SSPCLK	SSP Clock Output Line
$\overline{RD}$	33	O	5T	External Memory Read Strobe. RD is activated for every external instruction or data read access.		
$\overline{WR}$/ $\overline{WRL}$	34	O	5T	External Memory Write Strobe. In WR-mode, this pin is activated for every external data write access. In WRL-mode, this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection.		
$\overline{READY}$/ $\overline{READY}$	35	I	5T	Ready Input. Active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level. Polarity is programmable.		

Table 1 Pin definitions

5 INTERRUPT AND TRAP FUNCTIONS

The architecture of the ST10R172L supports several mechanisms for fast and flexible response to the service requests that can be generated from various sources, internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced, either by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt service routine is performed. For a PEC service, just one cycle is ‘stolen’ from the current CPU activity. A PEC service is a single, byte or word data transfer between any two memory locations, with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are very well suited, for example, to the transmission or reception of blocks of data. The ST10R172L has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher priority service request. For standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

of external memory space, the address space can be restricted to 1 MByte, 256 KByte or to 64 KByte.

8 PWM MODULE

A 1-channel Pulse Width Modulation (PWM) Module operates on channel 3. The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. The table below shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Mode 0 edge aligned	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU clock/1	20ns	195.3 KHz	48.83KHz	12.21KHz	3.052KHz	762.9Hz
CPU clock/64	1.28ns	3.052KHz	762.9Hz	190.7Hz	47.68Hz	11.92Hz
Mode 1 center aligned	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU clock/1	20ns	97.66KHz	24.41KHz	6.104KHz	1.525KHz	381.5Hz
CPU clock/64	1.28ns	1.525Hz	381.5 Hz	95.37Hz	23.84Hz	0Hz

Table 4 PWM unit frequencies and resolution at 50MHz CPU clock

F_{CPU}=50MHz	Timer input selection							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Prescaler Factor	8	16	32	64	128	256	512	1024
Input Frequency	6.25 MHz	3.125 MHz	1.5625 MHz	781 KHz	391 KHz	195 KHz	97.5 KHz	48.83 KHz
Resolution	160ns	320ns	640ns	1.28 us	2.56 us	5.12 us	10.24 us	20.48 us
Period	10.49ms	20.97ms	41.94ms	83.88ms	168ms	336ms	672ms	1.342s

Table 5 GPT1 timer input frequencies, resolution and periods

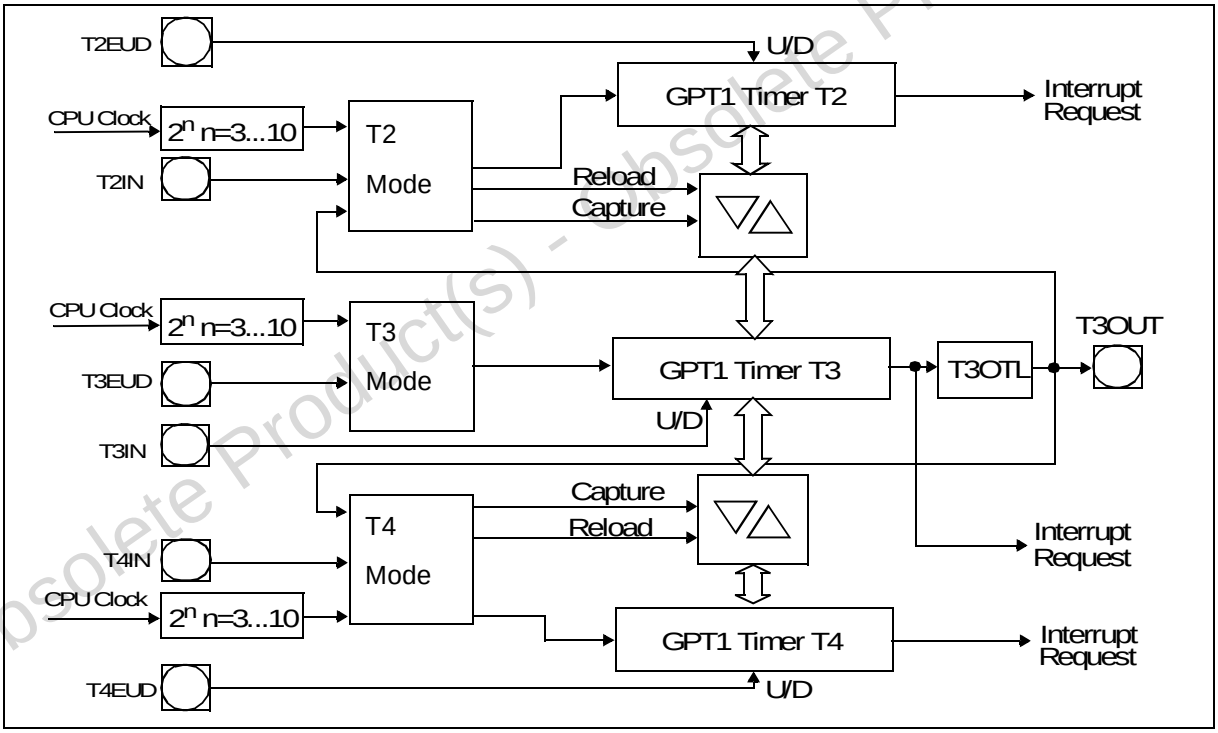


Figure 5 GPT1 block diagram

various commonly used baud rates together with the required reload values and the deviation errors compared to the intended baudrate.

S0BRS = '0', f_{CPU} = 50MHz				S0BRS = '1', f_{CPU} = 50MHz			
Baud Rate (Baud)	**Deviation Error**		**Reload Value**	**Baud Rate (Baud)**	**Deviation Error**		**Reload Value**
1562500	0.0%	/ 0.0%	0000_H / 0000_H	1041666	0.0%	/ 0.0%	0000_H / 0000_H
56000	+3.3%	/ -0.4%	$001A_H$ / $001B_H$	56000	+3.3%	/ -2.1%	0011_H / 0012_H
38400	+1.7%	/ -0.8%	0027_H / 0028_H	38400	+0.5%	/ -3.1%	$001A_H$ / $001B_H$
19200	+0.5%	/ -0.8%	0050_H / 0051_H	19200	+0.5%	/-1.4%	0035_H / 0036_H
9600	+0.5%	/ -0.1%	$00A1_H$/ $00A2_H$	9600	+0.5%	/ -0.5%	$006B_H$ / $006C_H$
4800	+0.2%	/ -0.1%	0144_H / 0145_H	4800	0.0%	/ -0.5%	$00D8_H$ / $00D9_H$
2400	0.0%	/ -0.1%	$028A_H$ / $028B_H$	2400	0.0%	/ -0.2%	$01B1_H$ / $01B2_H$
1200	0.0%	/ -0.1%	0515_H / 0516_H	1200	0.0%	/ -0.1%	0363_H / 0364_H
600	0.0%	/ 0.0%	$0A2B_H$ / $0A2C_H$	600	0.0%	/ -0.1%	$06C7_H$ / $06C8_H$
190	+0.4%	/+0.4%	$1FFF_H$ / $1FFF_H$	75	0.0%	/ 0.0%	$363F_H$ / 3640_H
				127	+0.1%	/ +0.1%	$1FFF_H$ / $1FFF_H$

Table 7 Commonly used baud rates, required reload values and deviation errors

SSP transmits 1...3 bytes or receives 1 byte after sending 1...3 bytes synchronously to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB and is used to select shifting and latching clock edges, and clock polarity. Up to two chip select lines may be activated in order to direct data transfers to one or both of two peripheral devices.

When the SSP is enabled, the four upper pins of Port4 can not be used as general purpose IO. Note that the segment address selection done via the system start-up configuration during reset has priority and overrides the SSP functions on these pins.

SSPCKS Value		Synchronous baud rate
000	SSP clock = CPU clock divided by 2	25 MBit/s
001	SSP clock = CPU clock divided by 4	12.5 MBit/s
010	SSP clock = CPU clock divided by 8	6.25 MBit/s

Table 8 Synchronous baud rate and SSPCKS reload values

SSPCKS Value		Synchronous baud rate
011	SSP clock = CPU clock divided by 16	3.13 MBit/s
100	SSP clock = CPU clock divided by 32	1.56 MBit/s
101	SSP clock = CPU clock divided by 64	781 KBit/s
110	SSP clock = CPU clock divided by 128	391 KBit/s
111	SSP clock = CPU clock divided by 256	195 KBit/s

Table 8 Synchronous baud rate and SSPCKS reload values

11 WATCHDOG TIMER

The Watchdog Timer is a fail-safe mechanism which limits the malfunction time of the controller. The Watchdog Timer is always enabled after device reset and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. In this way, the chip's start-up procedure is always monitored. The software must be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to maintain the Watchdog Timer, it will overflow generating an internal hardware reset and pulling the $\overline{\text{RSTOUT}}$ pin low to reset external hardware components.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. The table below shows the watchdog time range which for a 50MHz CPU clock rounded to 3 significant figures.

Reload value in WDTREL	Prescaler for f_{CPU}	
	2 (WDTIN = '0')	128 (WDTIN = '1')
FF_H	10.24 µs	655 µs
00_H	2.62 ms	168 ms

Table 9 Watchdog timer range

15 ELECTRICAL CHARACTERISTICS

15.1 Absolute Maximum Ratings

- Ambient temperature under bias (T_A): .....-40°C to +85 °C
- Storage temperature (T_{ST}): ..... – 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): ..... – 0.5 to +4.0 V
- Voltage on any pin with respect to ground (V_{SS}): ..... –0.5 to V_{DD} +0.5 V
- Voltage on any 5V tolerant pin with respect to ground (V_{SS}): .....–0.5 to 5.5 V
- Voltage on any 5V fail-safe pin with respect to ground (V_{SS}): .....–0.5 to 5.5 V
- Input current on any pin during overload condition: .....–10 to +10 mA
- Absolute sum of all input currents during overload condition: .....|100 mA|
- Power dissipation:.....1.0 W

Note *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.*

The parameters listed in this section represent both the ST10R172L controller characteristics and the system requirements. To aid parameters interpretation in design evaluation, the a symbol column is marked:

CC for **C**ontroller **C**haracteristics:	The ST10R172L logic provides signals with the respective timing characteristics.
SR for System Requirement:	The external system must provide signals with the respective timing characteristics to the ST10R172L.

15.2 DC Characteristics

V_{DD} = 3.3V ± 0.3V V_{SS} = 0 V Reset active T_A = -40°C to +85 °C°

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage	V_{IL}	SR	– 0.3	0.8	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	V_{IH}	SR	2.0	V_{DD} + 0.3	V	–
Input high voltage $\overline{RSTIN}$, RPD	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.3	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.3	V	–
Output low voltage (ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTIN}$,$\overline{RSTOUT}$, $\overline{CSX}$)	V_{OL}	CC	–	0.4	V	I_{OL} = 4 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.4	V	I_{OL1} = 2 mA
Output high voltage ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTIN}$,$\overline{RSTOUT}$, $\overline{CSX}$)	V_{OH}	CC	2.4	–	V	I_{OH} = –4 mA
Output high voltage[1] (all other outputs)	V_{OH1}	CC	2.4	–	V	I_{OH} = – 2mA
Input leakage current (3T pins)	I_{OZ}	CC	–	±10	µA	0 V<V_{IN}<V_{DD}
Input leakage current (5T, 5S pins)	I_{OZ1}	CC	–	±10 ±100[7]	µA µA	0 V<V_{IN}<V_{DD} V_{DD}<V_{IN}<5.0V[7]
$\overline{RSTIN}$ pull-up resistor [2]	R_{RST}	CC	20	300	kΩ	V_{IN} = 0 V
Read/Write pullup current[3]	I_{RWH} [4]		–	-40	µA	V_{OUT} = 2.4 V
Read/Write pullup current[3]	I_{RWL} [5]		-500	–	µA	V_{OUT} = 0.4 V
ALE pulldown current[3]	I_{ALEL} [4]		40	–	µA	V_{OUT} = 0.4 V
ALE pulldown current[3]	I_{ALEH} [5]		–	500	µA	V_{OUT} = 2.4 V
Port 6 ($\overline{CS}$) pullup current[3]	I_{P6H} [4]		–	-40	µA	V_{OUT} = 2.4 V
Port 6 ($\overline{CS}$) pullup current[3]	I_{P6L} [5]		-500	–	µA	V_{OUT} = 0.4 V

Table 11 DC characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
PORT0 configuration current[3]	I_{P0H}[4]	–	-4	µA	$V_{IN} = V_{IHmin}$
	I_{P0L}[5]	-50	–	µA	$V_{IN} = V_{ILmax}$
RPD pulldown current[2]	I_{RPD}[5]	100	500	µA	$V_{OUT} = V_{DD}$
XTAL1 input current	I_{IL} CC	–	±20	µA	$0\ V < V_{IN} < V_{DD}$
Pin capacitance[6)] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	15 + 2.5 * f_{CPU}	mA	f_{CPU} in [MHz] [7)]
Idle mode supply current	I_{ID}	–	10 + 0.9 * f_{CPU}	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] [7]
Power-down mode supply current	I_{PD} [8]	–	200	µA	V_{DD} = 3.6 V [9]

Table 11 DC characteristics

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the resulting voltage comes from the external circuitry.
2) This specification is only valid during reset, or interruptible power-down mode, after reception of an external interrupt signal that will wake up the CPU.
3) This specification is only valid during reset, hold or adapt-mode. Port 6 pins are only affected if they are used for $\overline{CS}$ output and the open drain function is not enabled.
4) The maximum current may be drawn while the signal line remains inactive.
5) The minimum current must be drawn in order to drive the signal line active.
6) Not 100% tested, guaranteed by design characterization.
7) Supply current is a function of operating frequency as illustrated in Figure 7 on page 35. This parameter is tested at V_{DD}max and 50 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} with an infinite execution of NOP instruction fetched from external memory (16-bit demux bus mode, no waitstates, no memory tri-state waitstates, normal ALE).
8) Typical value at 25°C = 20µA.
9) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

15.3 AC Characteristics

Test conditions

- Input pulse levels: ..... 0 to +3.0 V
- Input rise and fall times (10%-90%): ..... 2.5 ns
- Input timing reference levels: ..... +1.5 V
- Output timing reference levels: ..... +1.5 V
- Output load: ..... see Figure 9

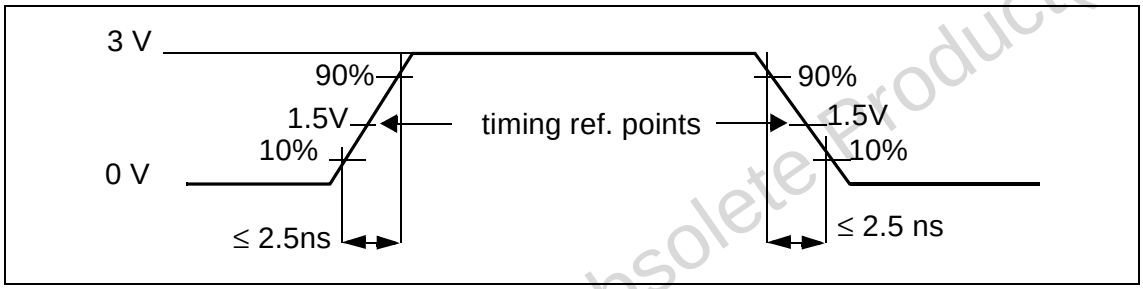


Figure 8 Input waveforms

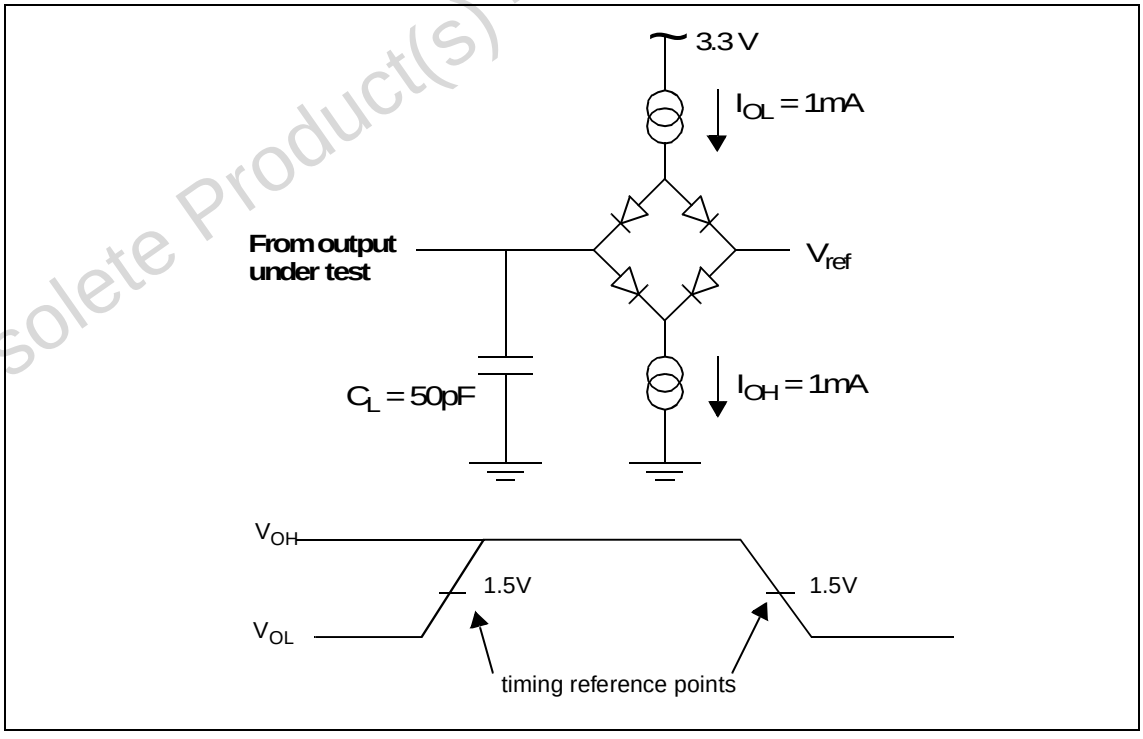


Figure 9 Output load circuit waveform

15.3.1 Cpu Clock Generation Mechanisms

ST10R172L internal operation is controlled by the CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations. The external timing (AC Characteristics) specification therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

The CPU clock signal can be generated by different mechanisms. The duration of TCLs and their variation (and also the external timing) depends on the f_{CPU} generation mechanism. This must be considered when calculating ST10R172L timing.

The CPU clock generation mechanism is set during reset by the logic levels on pins P0.15-13 (P0H.7-5).

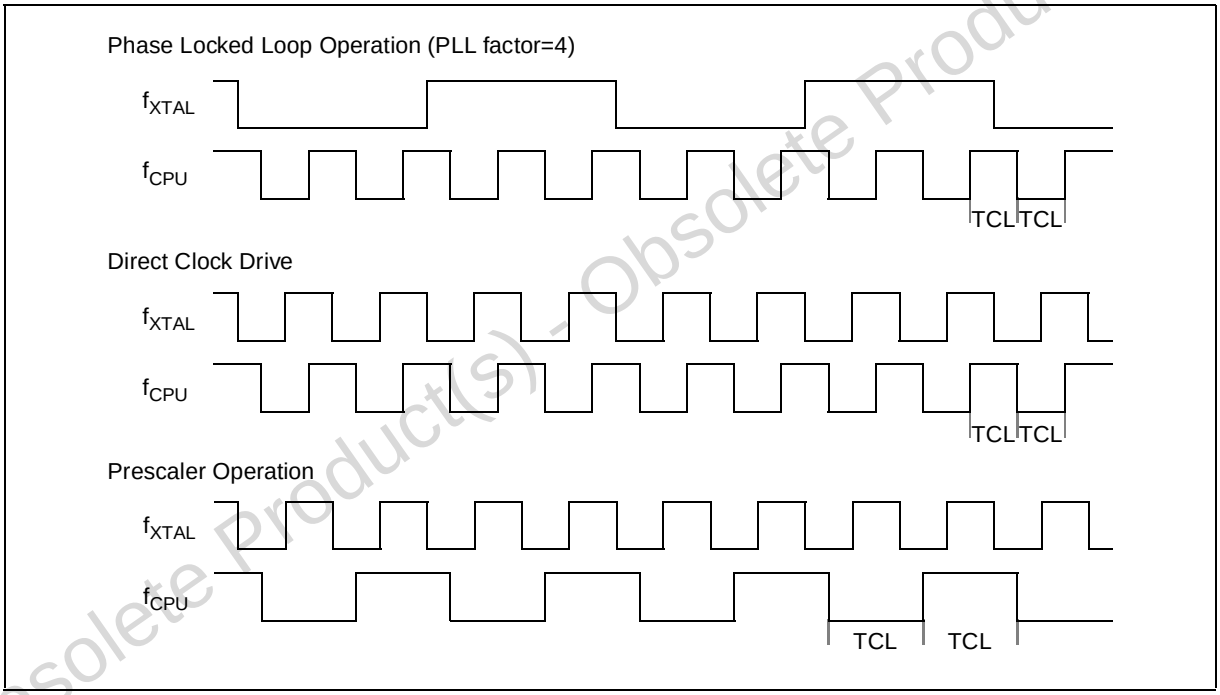


Figure 11 CPU clock generation mechanisms

P0.15-13 (P0H.7-5)			CPU frequency $f_{CPU} = f_{XTAL} * F$	External clock input range 10-50MHz	Notes
1	1	1	$F_{XTAL} * 4$	2.5 to 12.5 MHz	Default configuration
1	1	0	$F_{XTAL} * 3$	3.33 to 16.66 MHz	
1	0	1	$F_{XTAL} * 2$	5 to 25 MHz	

Table 12 CPU clock generation mechanisms

Note *The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use* $TCL_{max} = 1/f_{XTAL} \times DC_{max}$ *instead of* TCL_{min}.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

Oscillator Watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows:

After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, set bit 4 of SYSCON register OWDDIS.

When the OWD is enabled, the PLL runs on its free-running frequency and increments the Oscillator Watchdog counter. On each transition of the XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

Phase locked loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock. The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{XTAL} * F$). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. In this way, f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which affects individual TCL duration.Therefore, AC characteristics that refer to TCLs must be calculated using the minimum possible TCL.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL constantly adjusts its output frequency, it corresponds to the applied input frequency (crystal or oscillator). The relative deviation for periods of more than one TCL is lower than for one single TCL. For a period of *N* * TCL the minimum value is computed using the corresponding deviation D_N:

$$TCL_{min} = TCL_{NOM} \times (1 - |D_N| / 100)$$

$$D_N = \pm(4 - N/15)[\%]$$

15.3.3 Multiplexed Bus

V_{DD} = 3.3 V ± 0.3 V V_{SS} = 0 V T_A = -40°C to +85 °C C_L = 50 pF

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (60 ns at 50-MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 50 MHz		Variable CPU Clock 1/2TCL = 1 to 50 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	7 + t_A	–	TCL - 3 + t_A	–	ns
Address (P1, P4), $\overline{BHE}$ setup to ALE	t_6	CC	3 + t_A	–	TCL - 7 + t_A	–	ns
Address (P0) setup to ALE	t_{6m}	CC	5 + t_A	–	TCL - 5 + t_A	–	ns
Address hold after ALE	t_7	CC	5 + t_A	–	TCL - 5 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	5 + t_A	–	TCL - 5 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-5 + t_A	–	-5 + t_A	–	ns
Address float after $\overline{RD}$, (with RW-delay)[1)]	t_{10}	CC	–	5[1]	–	5[1]	ns
Address float after $\overline{RD}$, (no RW-delay)[1]	t_{11}	CC	–	15[1]	–	TCL + 5[1]	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	13 + t_C	–	2TCL - 7+ t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	23 + t_C	–	3TCL - 7 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	5 + t_C	–	2TCL - 15 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	15 + t_C	–	3TCL - 15 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	15 + t_A + t_C	–	3TCL - 15 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	20 + $2t_A$ + t_C	–	4TCL - 20 + $2t_A$ + t_C	ns

Table 14 Multiplexed bus

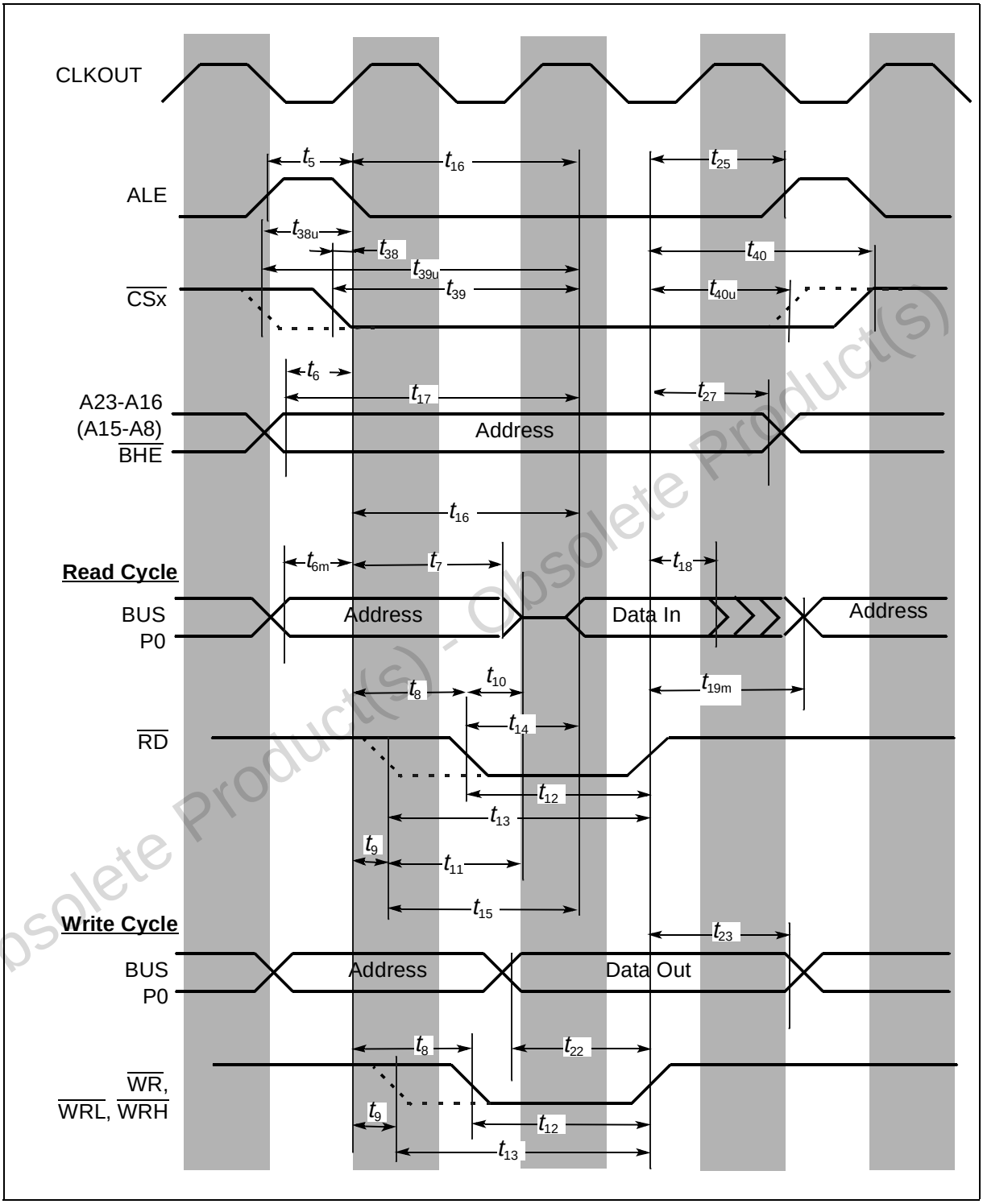


Figure 13 External memory cycle:
multiplexed bus, with/without read/write delay, normal ALE

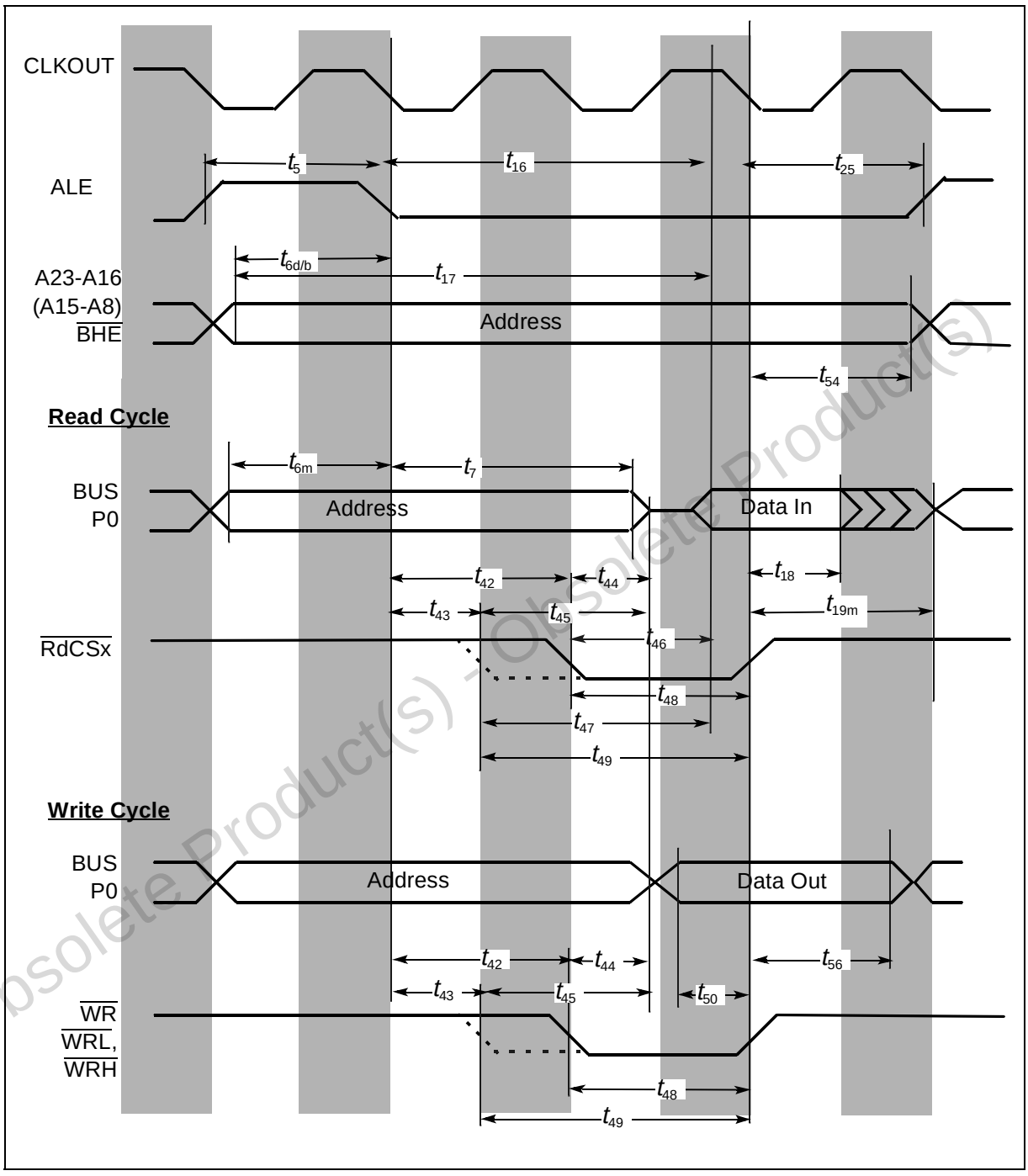


Figure 16 External memory cycle:
multiplexed bus, with/without read/write delay, extended ale, read/write chip select

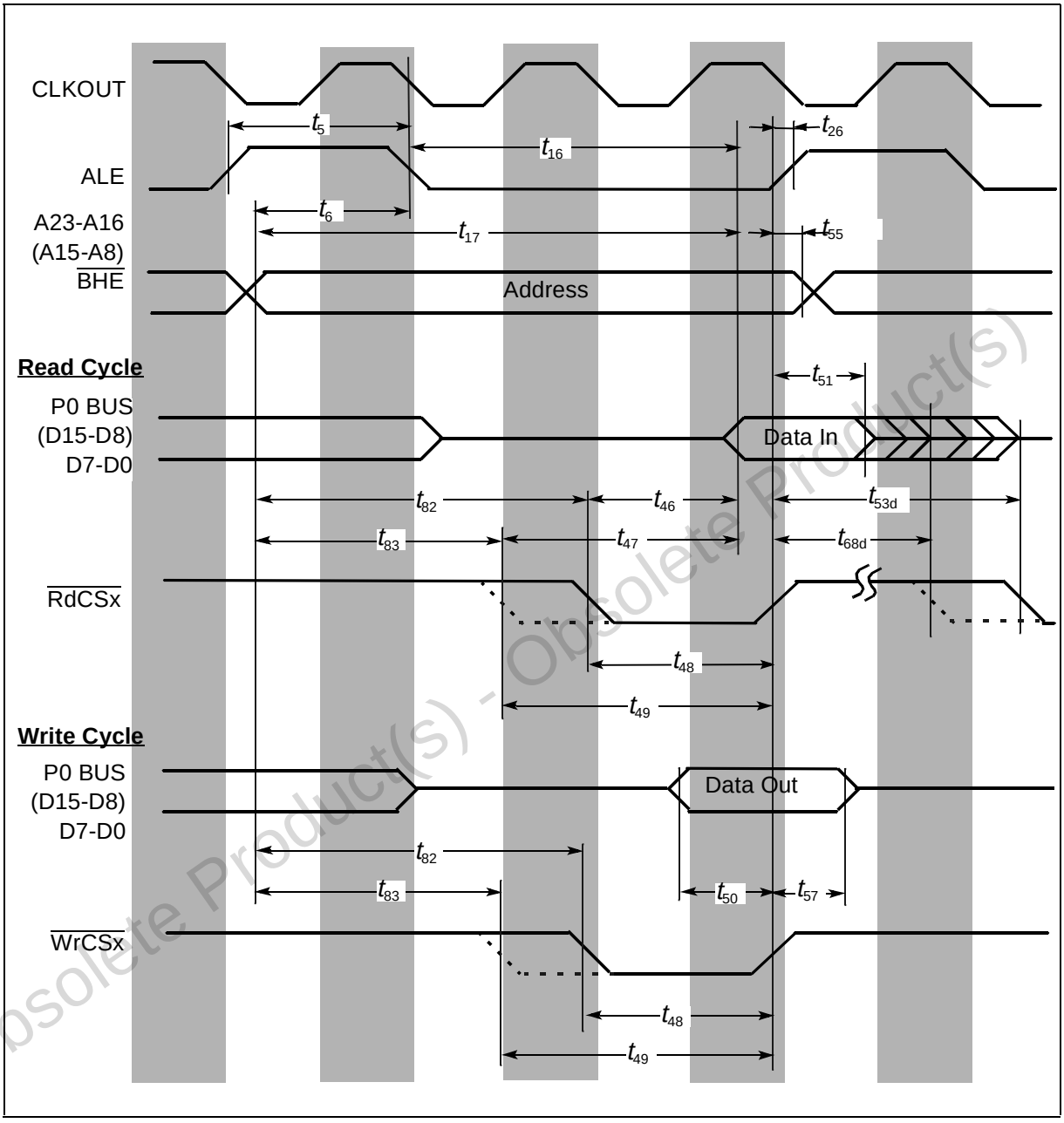


Figure 20 External memory cycle:
demultiplexed bus, no read/write delay, extended ALE, read/write chip select

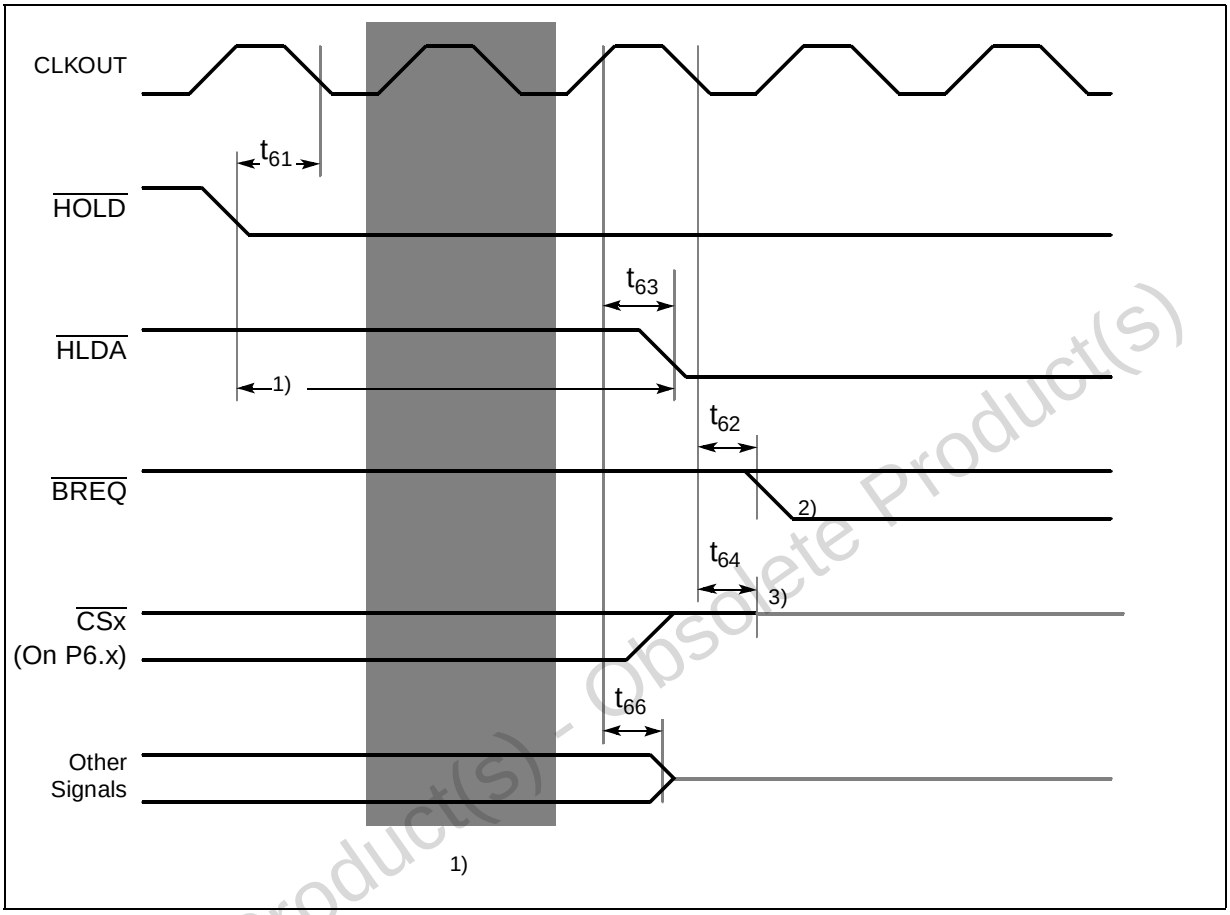


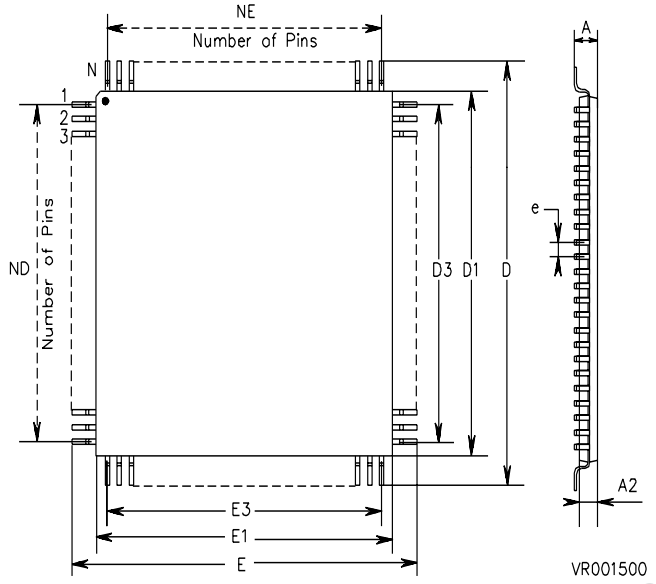
Figure 22 External bus arbitration, releasing the bus

1 The ST10R172L will complete the running bus cycle before granting bus access.

2 This is the first opportunity for $\overline{BREQ}$ to become active.

3 The $\overline{CS}$ outputs will be resistive high (pullup) after t_{64}.

16 PACKAGE MECHANICAL DATA



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.50			0.020	
Number of Pins						
ND	25					
NE	25					
N	100					

Figure 28 Package outline TQFP100 (14 x 14 mm)

17 ORDERING INFORMATION

Sales type	Temperature range	Package
ST10R172LT1	0°C to 70°C	TQFP100 (14x 14)
ST10R172LT6	-40°C to +85 °C	