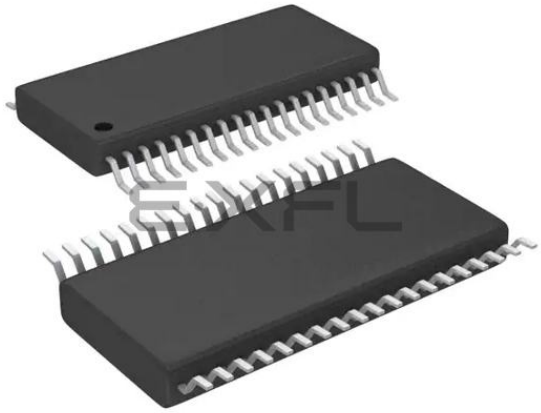
Infineon Technologies - SAA-XC866L-2FRA 5V BE Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	27
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 140°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saa-xc866l-2fra-5v-be

Figure 6 illustrates the memory address spaces of the SAA-XC866-4FR devices.

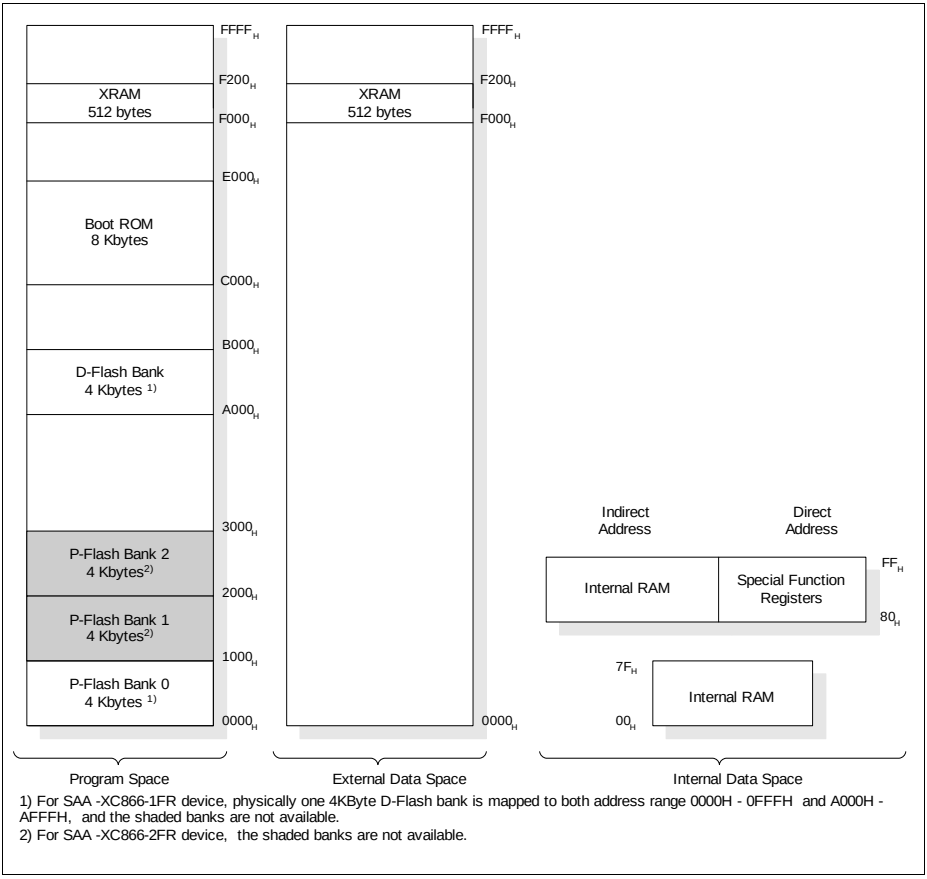


Figure 6 Memory Map of SAA-XC866 Flash Devices

3.2.1 Memory Protection Strategy

The SAA-XC866 memory protection strategy includes:

- Read-out protection: The Flash Memory can be enabled for read-out protection and ROM memory is always protected.
- Program and erase protection: The Flash memory in all devices can be enabled for program and erase protection.

Flash memory protection is available in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 3**.

Table 3 Flash Protection Modes

Mode	0	1
Activation	Program a valid password via BSL mode 6	
Selection	MSB of password = 0	MSB of password = 1
P-Flash contents can be read by	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
P-Flash program and erase	Not possible	Not possible
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash
D-Flash program	Possible	Not possible
D-Flash erase	Possible, on the condition that bit DFLASHEN in register MISC_CON is set to 1 prior to each erase operation	Not possible

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. A password match triggers an automatic erase of the read-protected Flash contents, see **Table 4** and **Table 5**, and the programmed password is erased. The Flash protection is then disabled upon the next reset.

For XC866-2FR and XC866-4FR devices:

The selection of protection type is summarized in **Table 4**.

In order to access a register located in a page different from the actual one, the current page must be left. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and finally, the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value
  (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or
- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
  (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

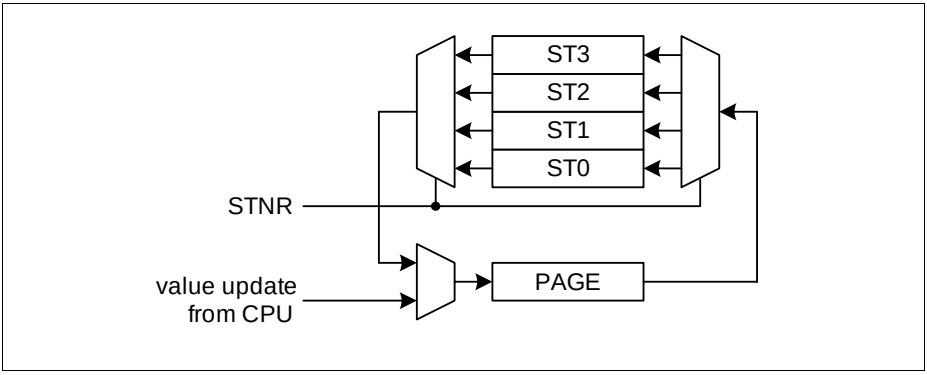


Figure 10 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The SAA-XC866 supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

Table 9 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B1_H$	**P3_ALTSEL1** **Reset: 00_H** P3 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, Page 3										
80_H	**P0_OD** **Reset: 00_H** P0 Open Drain Control Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_OD** **Reset: 00_H** P1 Open Drain Control Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$B0_H$	**P3_OD** **Reset: 00_H** P3 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 ADC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$D1_H$	**ADC_PAGE** **Reset: 00_H** Page Register for ADC	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, Page 0										
CA_H	**ADC_GLOBCTR** **Reset: 30_H** Global Control Register	Bit Field	ANON	DW	CTC		0			
		Type	rw	rw	rw		r			
CB_H	**ADC_GLOBSTR** **Reset: 00_H** Global Status Register	Bit Field	0		CHNR			0	SAMPLE	BUSY
		Type	r		rh			r	rh	rh
CC_H	**ADC_PRAR** **Reset: 00_H** Priority and Arbitration Register	Bit Field	ASEN1	ASEN0	0	ARBM	CSM1	PRIO1	CSM0	PRIO0
		Type	rw	rw	r	rw	rw	rw	rw	rw
CD_H	**ADC_LCBR** **Reset: $B7_H$** Limit Check Boundary Register	Bit Field	BOUND1				BOUND0			
		Type	rw				rw			
CE_H	**ADC_INPCR0** **Reset: 00_H** Input Class Register 0	Bit Field	STC							
		Type	rw							
CF_H	**ADC_ETRCR** **Reset: 00_H** External Trigger Control Register	Bit Field	SYNEN1	SYNEN0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, Page 1										
CA_H	**ADC_CHCTR0** **Reset: 00_H** Channel Control Register 0	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CB_H	**ADC_CHCTR1** **Reset: 00_H** Channel Control Register 1	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CC_H	**ADC_CHCTR2** **Reset: 00_H** Channel Control Register 2	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CD_H	**ADC_CHCTR3** **Reset: 00_H** Channel Control Register 3	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CE_H	**ADC_CHCTR4** **Reset: 00_H** Channel Control Register 4	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CF_H	**ADC_CHCTR5** **Reset: 00_H** Channel Control Register 5	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
$D2_H$	**ADC_CHCTR6** **Reset: 00_H** Channel Control Register 6	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
$D3_H$	**ADC_CHCTR7** **Reset: 00_H** Channel Control Register 7	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
RMAP = 0, Page 2										

3.3.1 Flash Bank Sectorization

The SAA-XC866 product family offers four Flash devices with either 8 Kbytes or 16 Kbytes of embedded Flash memory. These Flash memory sizes are made up of two or four 4-Kbyte Flash banks, respectively. Each Flash device consists of Program Flash (P-Flash) bank(s) and a single Data Flash (D-Flash) bank with different sectorization shown in **Figure 11**. Both types can be used for code and data storage. The label “Data” neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different Flash bank sectorizations.

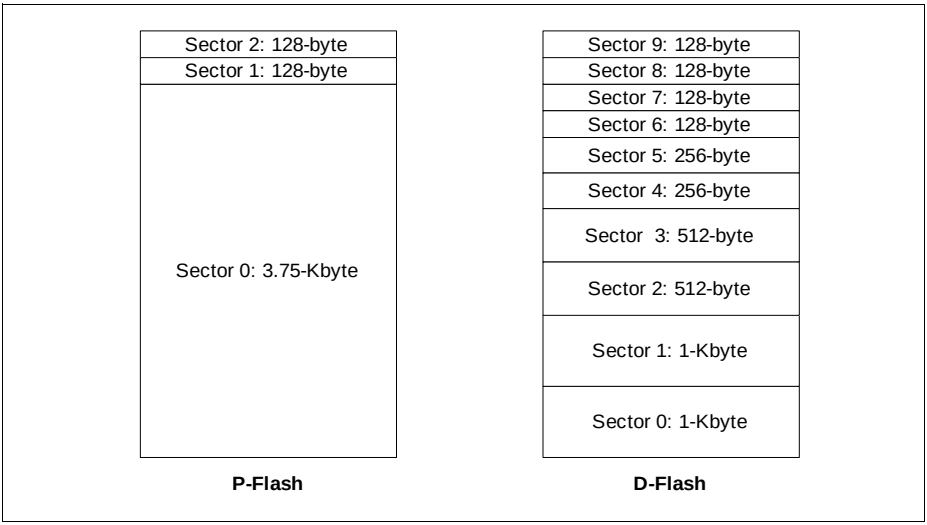


Figure 11 Flash Bank Sectorization

The internal structure of each Flash bank represents a sector architecture for flexible erase capability. The minimum erase width is always a complete sector, and sectors can be erased separately or in parallel. Contrary to standard EPROMs, erased Flash memory cells contain 0s.

The D-Flash bank is divided into more physical sectors for extended erasing and reprogramming capability; even numbers for each sector size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

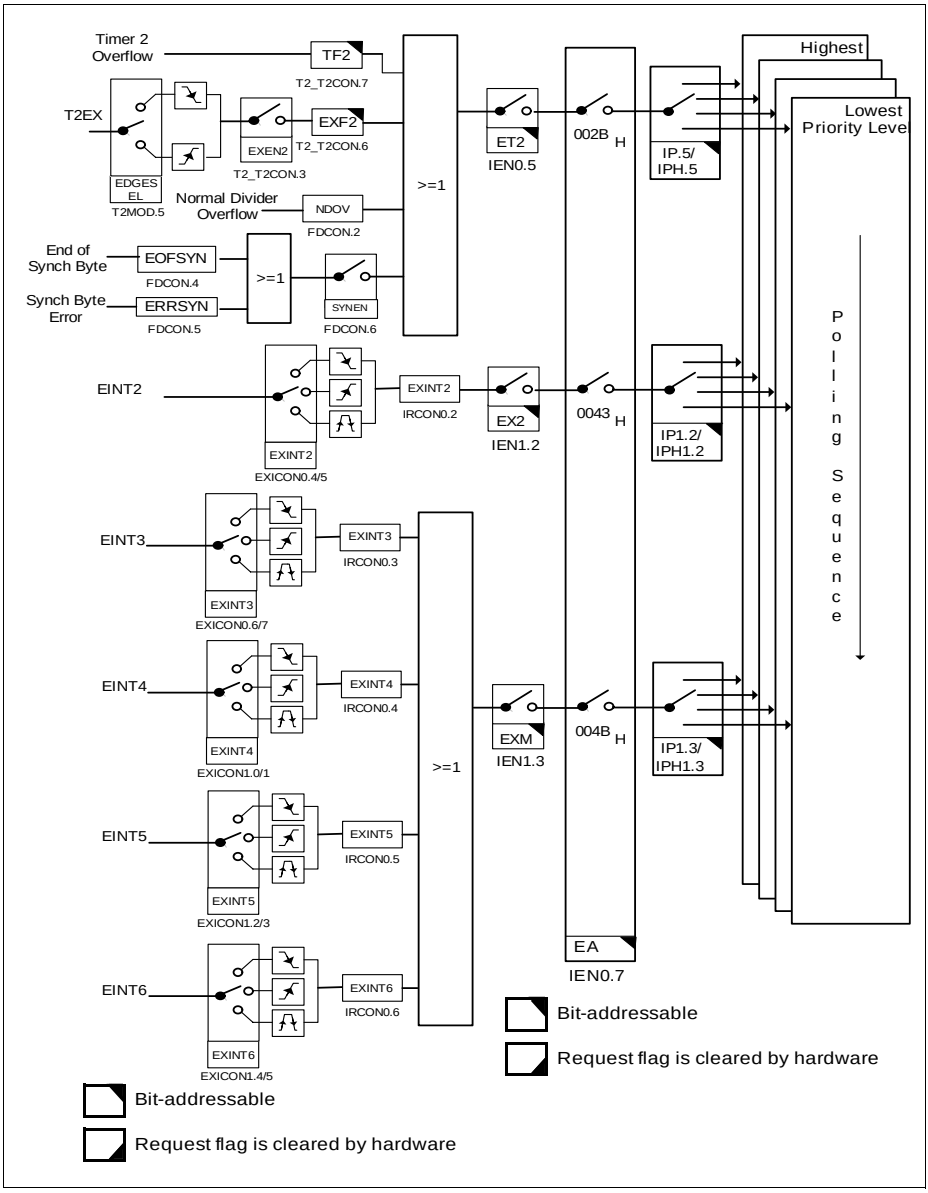


Figure 15 Interrupt Request Sources (Part 2)

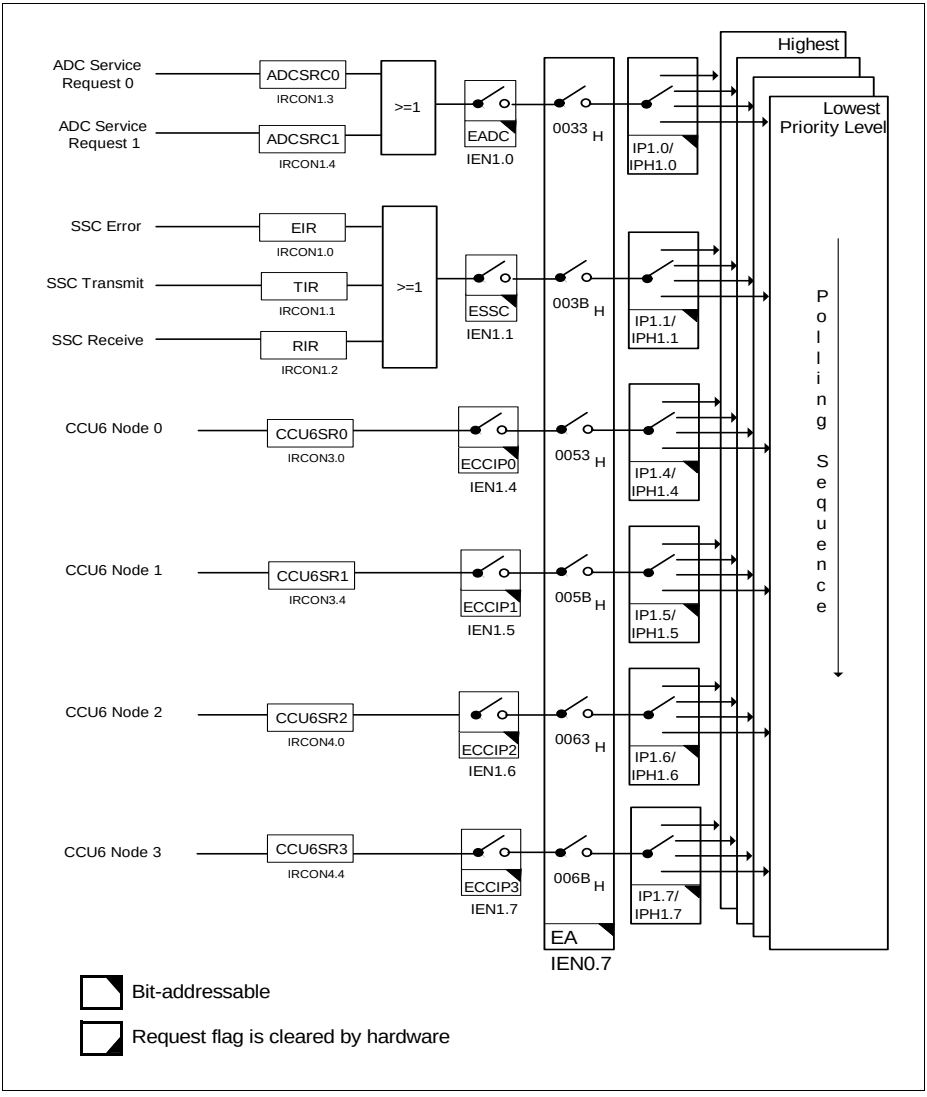


Figure 16 Interrupt Request Sources (Part 3)

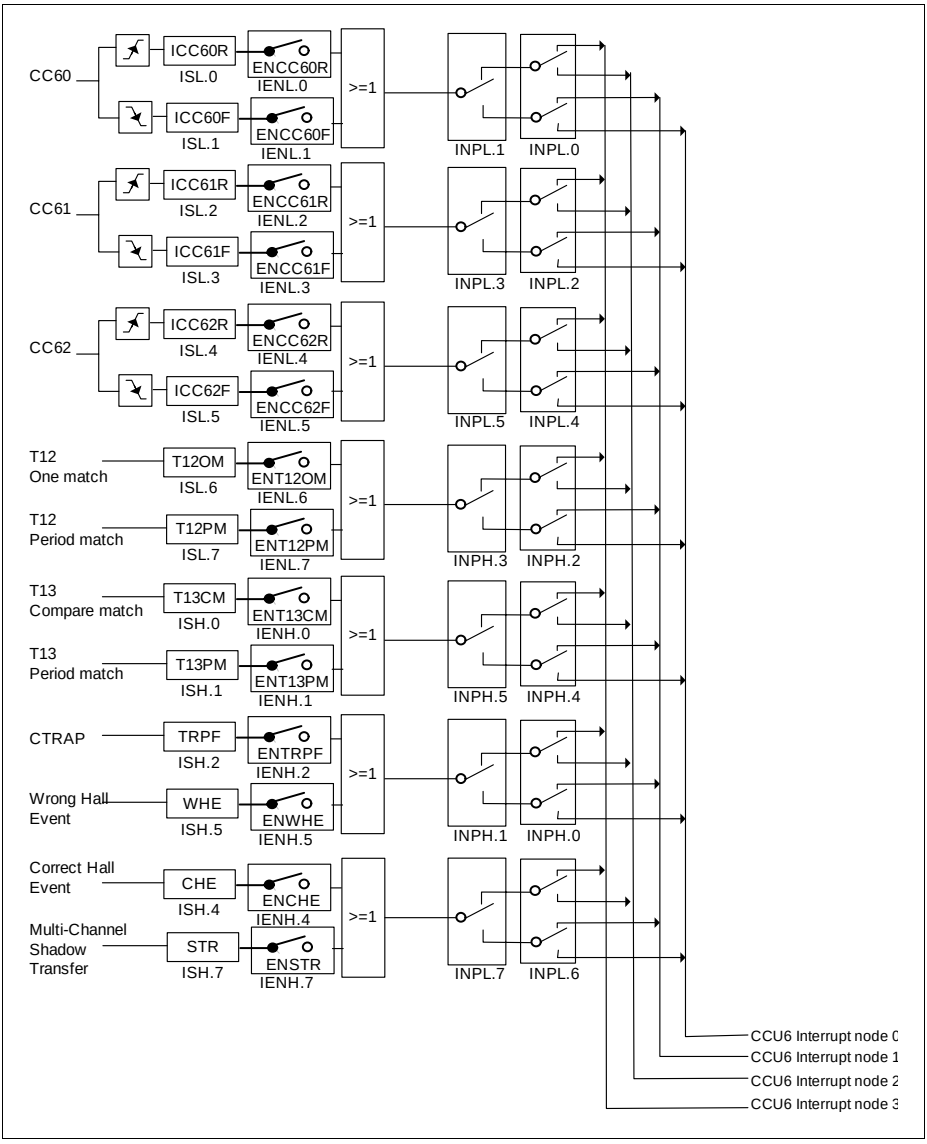


Figure 17 Interrupt Request Sources (Part 4)

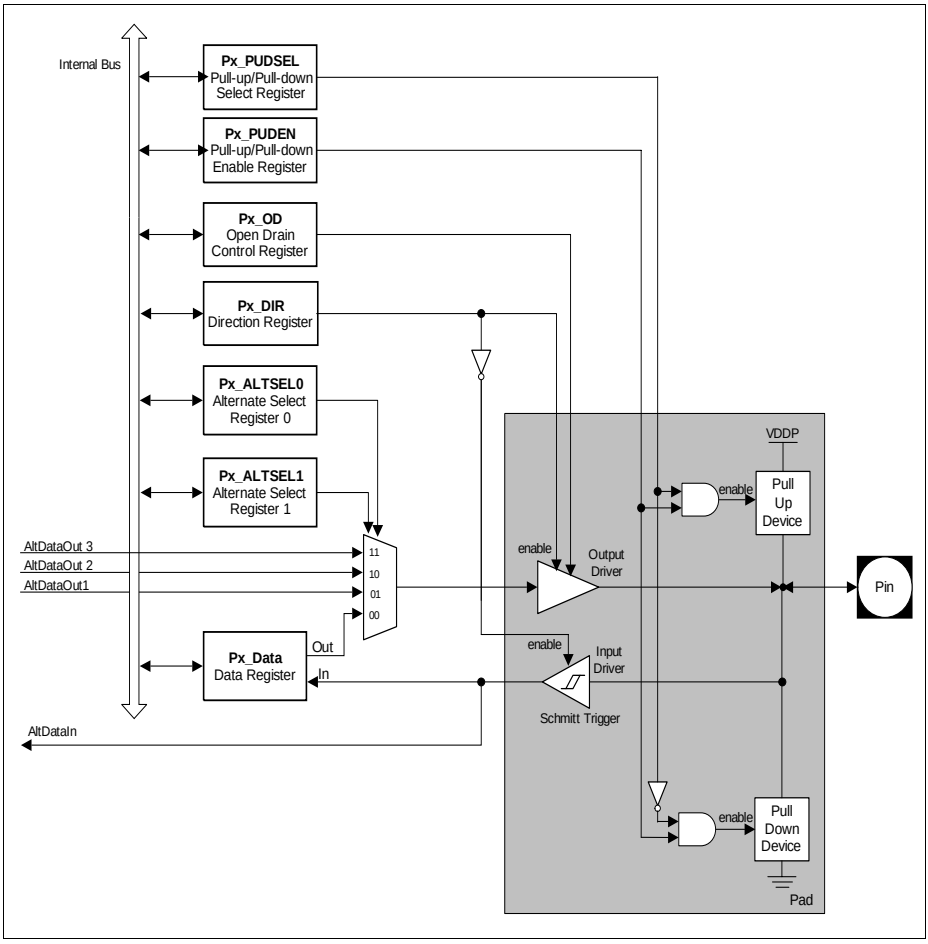


Figure 18 General Structure of Bidirectional Port

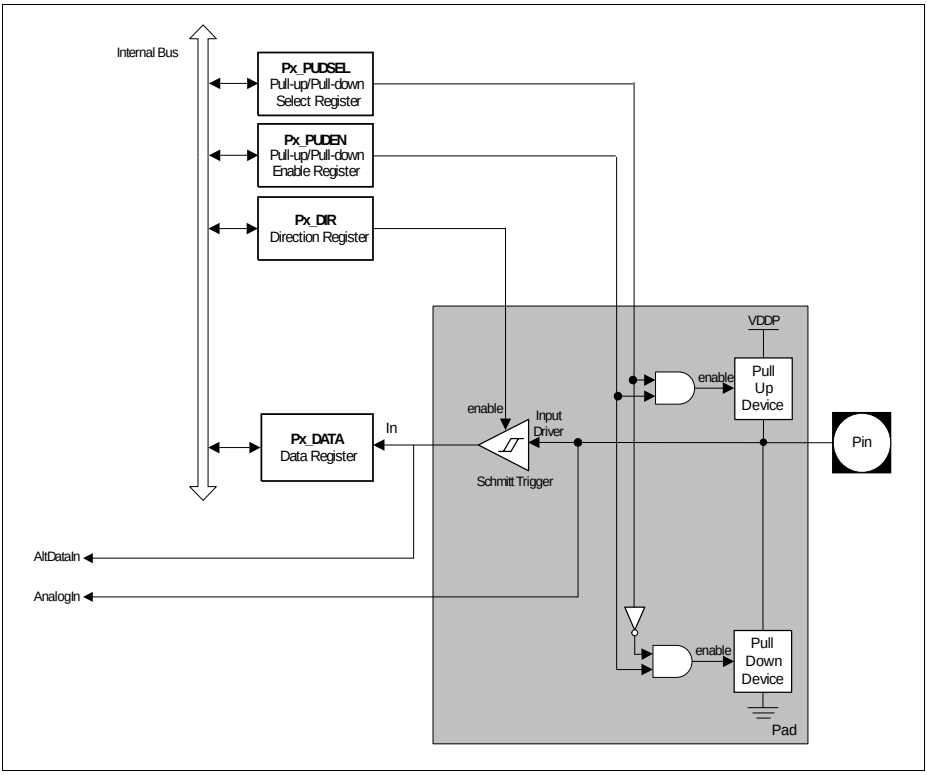


Figure 19 General Structure of Input Port

3.6 Power Supply System with Embedded Voltage Regulator

The SAA-XC866 microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 20 shows the SAA-XC866 power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

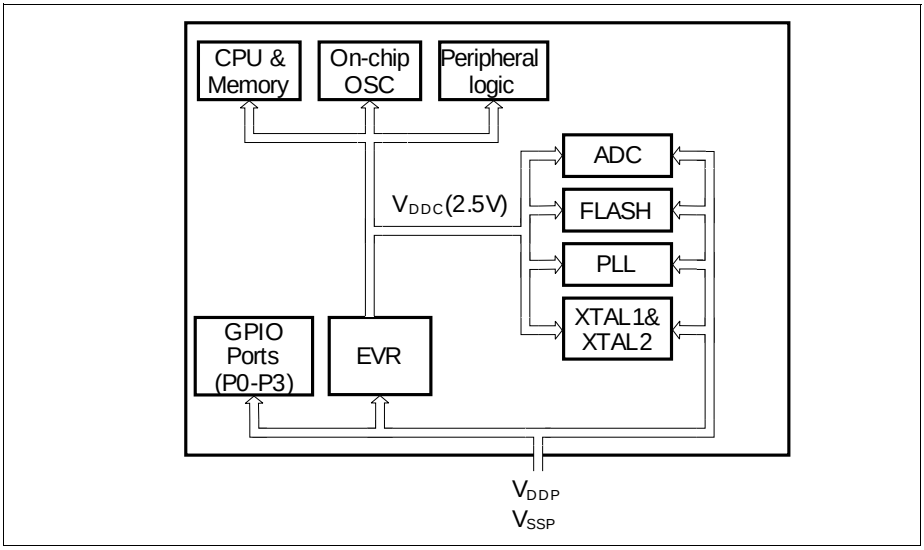


Figure 20 SAA-XC866 Power Supply System

EVR Features:

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDC} and V_{DDP} prewarning detection
- V_{DDC} brownout detection

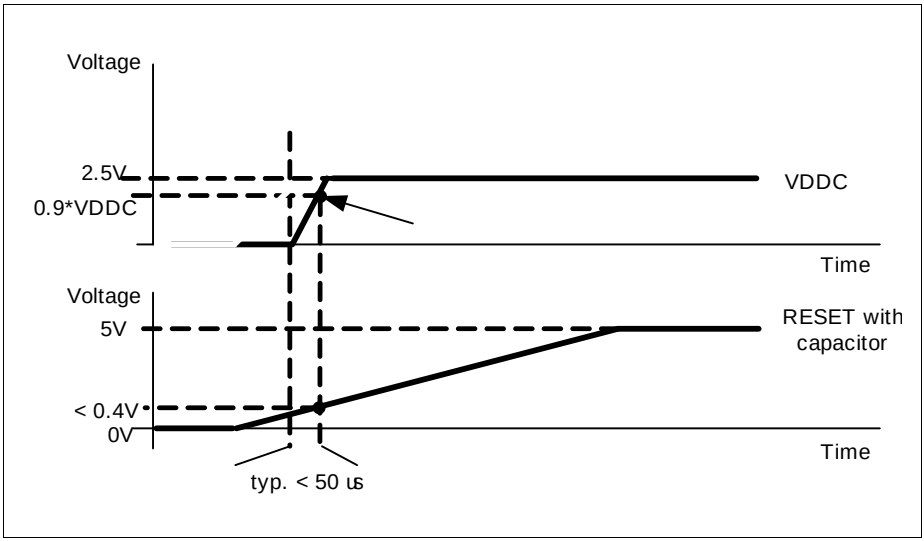
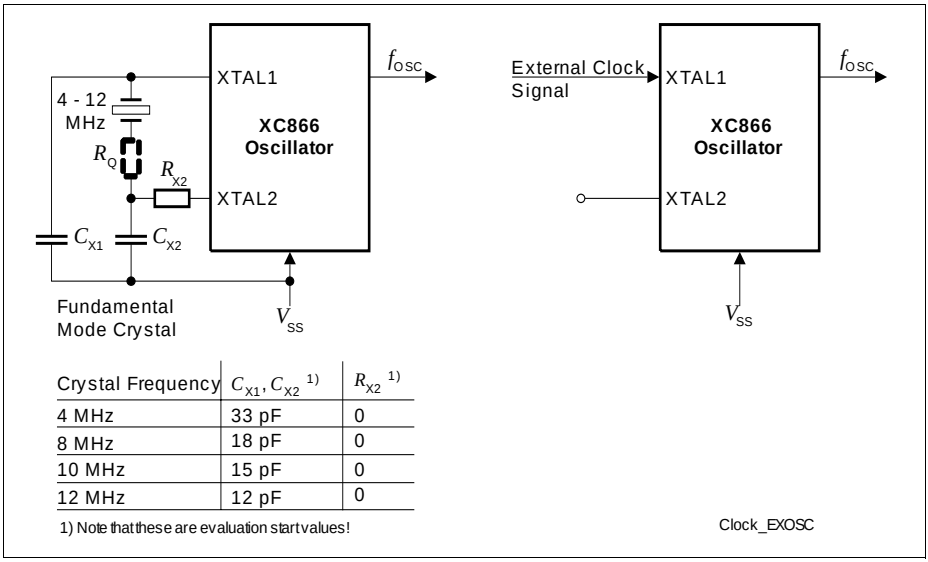


Figure 22 V_{DDP}, V_{DDC} and V_{RESET} during Power-on Reset

The second type of reset in SAA-XC866 is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin $\overline{\text{RESET}}$ is provided for the hardware reset. To ensure the recognition of the hardware reset, pin $\overline{\text{RESET}}$ must be held low for at least 100 ns.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.



Crystal Frequency	C_{X1}, C_{X2} 1)	R_{X2} 1)
4 MHz	33 pF	0
8 MHz	18 pF	0
10 MHz	15 pF	0
12 MHz	12 pF	0

1) Note that these are evaluation start values!

Figure 24 External Oscillator Circuitries

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

3.11 Universal Asynchronous Receiver/Transmitter

The Universal Asynchronous Receiver/Transmitter (UART) provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features:

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART can operate in four asynchronous modes as shown in **Table 25**. Data is transmitted on TXD and received on RXD.

Table 25 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$
Mode 3: 9-bit shift UART	Variable

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. The variable baud rate is set by either the underflow rate on the dedicated baud-rate generator, or by the overflow rate on Timer 1.

Table 27 Deviation Error for UART with Fractional Divider enabled

f_{PCLK}	Prescaling Factor (2^{BRPRE})	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
26.67 MHz	1	10 (A_H)	177 ($B1_H$)	+0.03 %
13.33 MHz	1	7 (7_H)	248 ($F8_H$)	+0.11 %
6.67 MHz	1	3 (3_H)	212 ($D4_H$)	-0.16 %

3.11.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

[3.1]

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times f_{PCLK}}{32 \times 2 \times (256 - TH1)}$$

3.12 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 29**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV}, where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

[3.2]

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP}$$

The block diagram of the CCU6 module is shown in **Figure 32**.

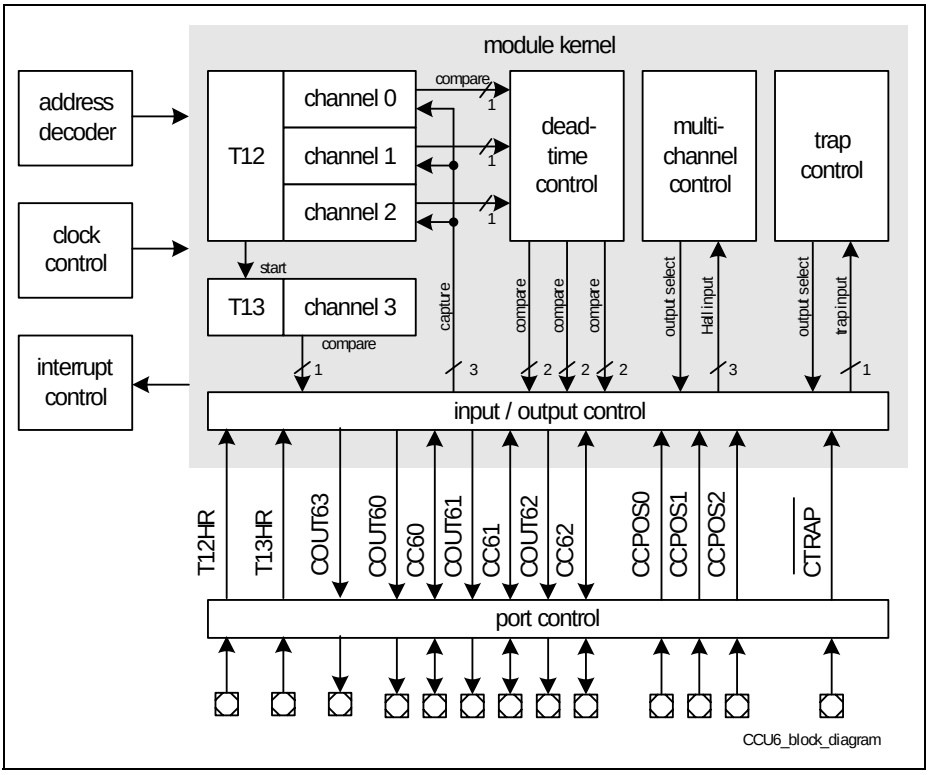


Figure 32 CCU6 Block Diagram

3.18.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

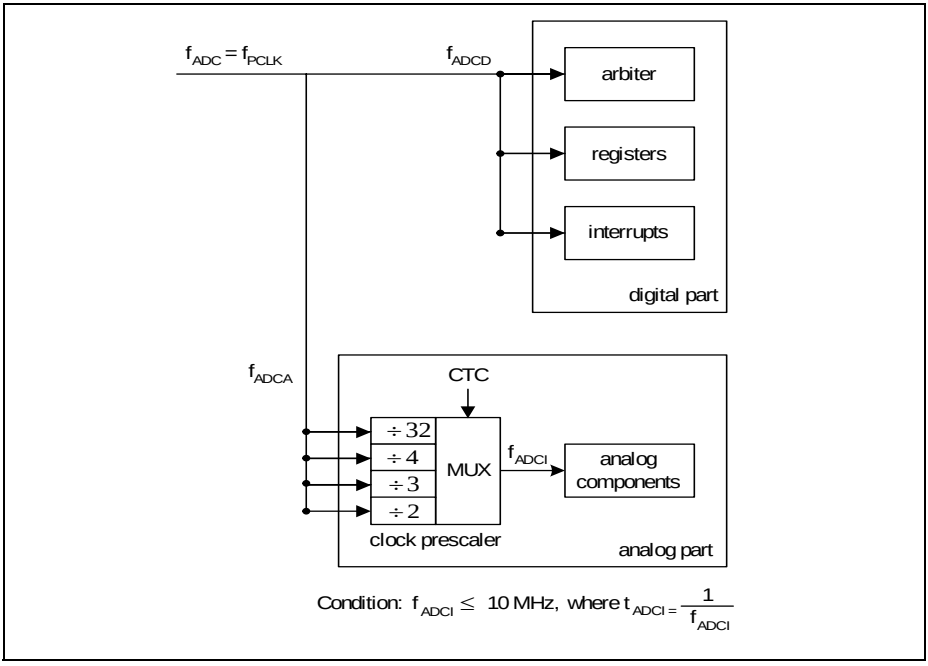


Figure 33 ADC Clocking Scheme

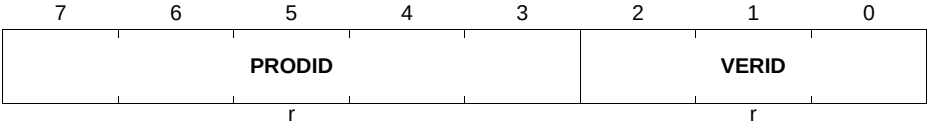
Table 31 JTAG ID Summary

ROM	SAA-XC866L-4RRA	1013 9083$_H$
	SAA-XC866-4RRA	1013 9083$_H$
	SAA-XC866L-2RRA	1013 9083$_H$
	SAA-XC866-2RRA	1013 9083$_H$

3.20 Identification Register

The SAA-XC866 identity register is located at Page 1 of address B3$_H$.

ID
Identity Register **Reset Value: 0000 0010$_B$**



Field	Bits	Type	Description
VERID	[2:0]	r	**Version ID** 010$_B$
PRODID	[7:3]	r	**Product ID** 00000$_B$

4.3 AC Parameters

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 38**, **Figure 39** and **Figure 40**.

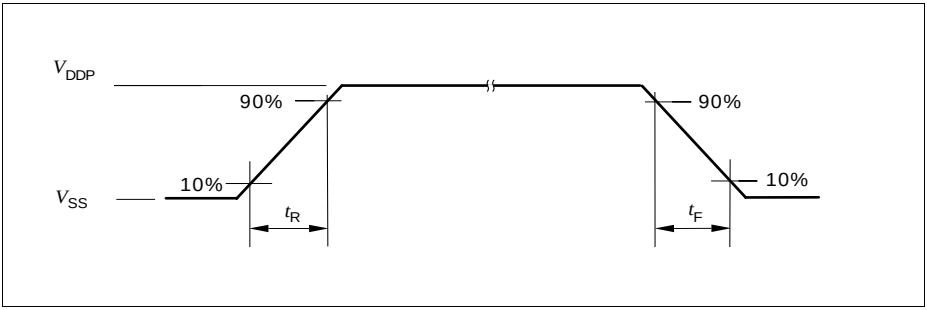


Figure 38 Rise/Fall Time Parameters

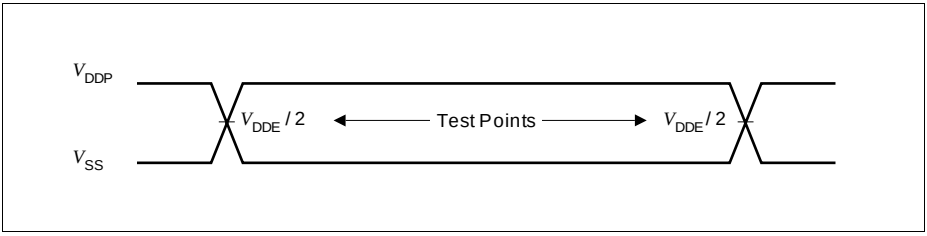


Figure 39 Testing Waveform, Output Delay

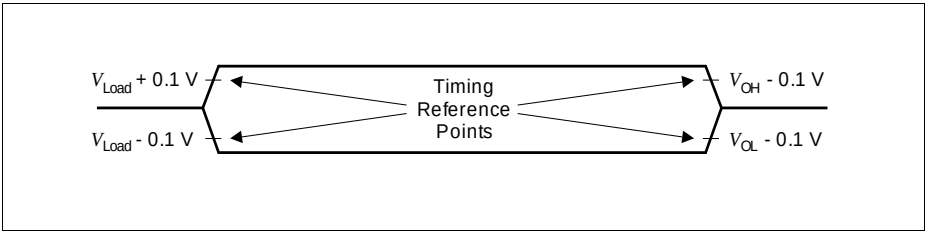


Figure 40 Testing Waveform, Output High Impedance