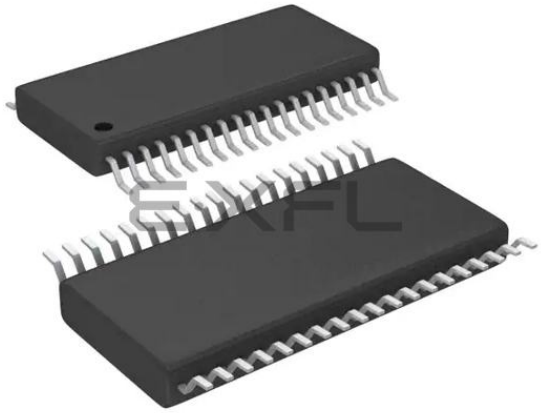
# Infineon Technologies - SAA-XC866L-4FRA BE Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 86MHz |
| Connectivity | LINbus, SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 140°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 38-TFSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-38 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saa-xc866l-4fra-be |

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**Figure 6** illustrates the memory address spaces of the SAA-XC866-4FR devices.

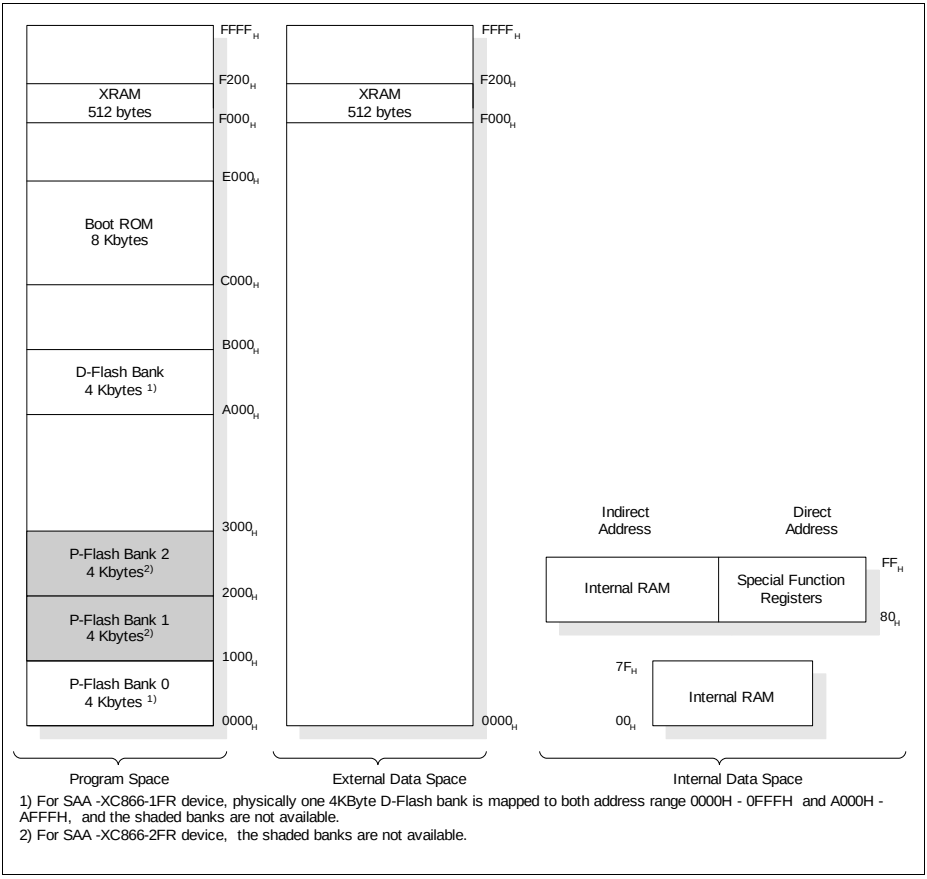



**Figure 6 Memory Map of SAA-XC866 Flash Devices**

*Note: The RMAP bit must be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.*

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

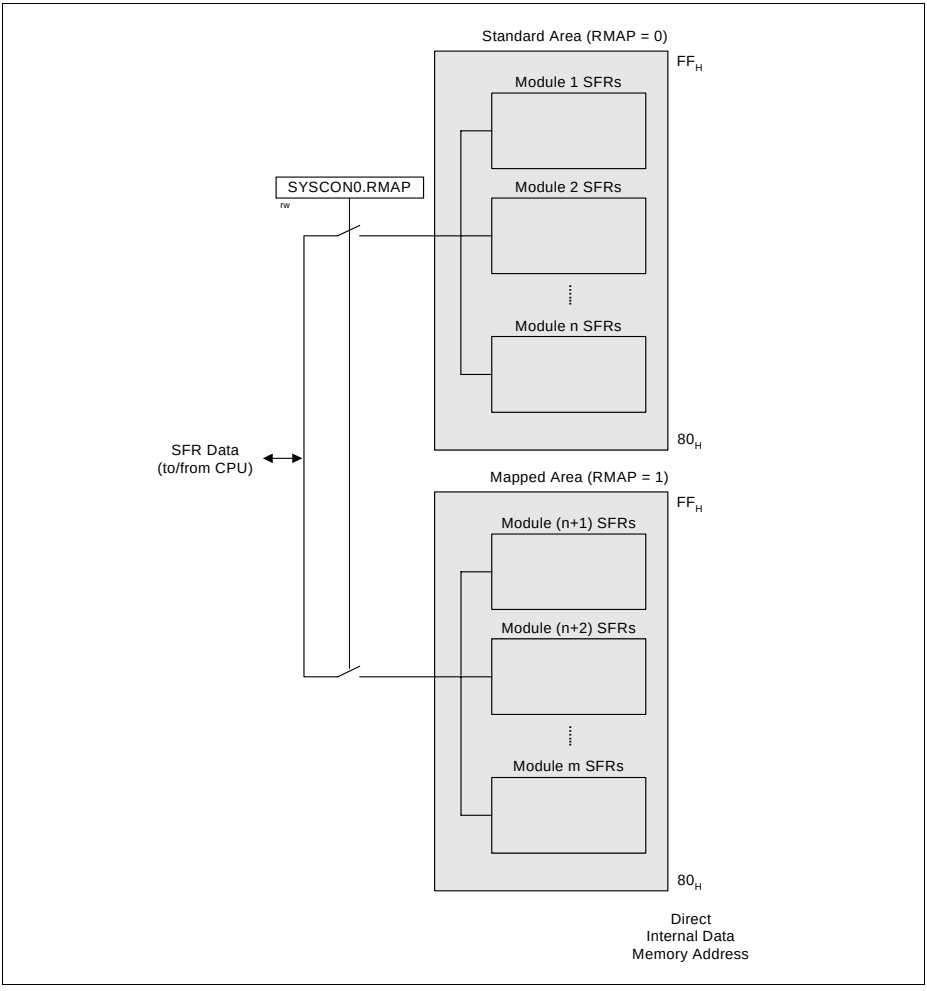



**Figure 8 Address Extension by Mapping**

In order to access a register located in a page different from the actual one, the current page must be left. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and finally, the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value
  (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or
- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
  (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

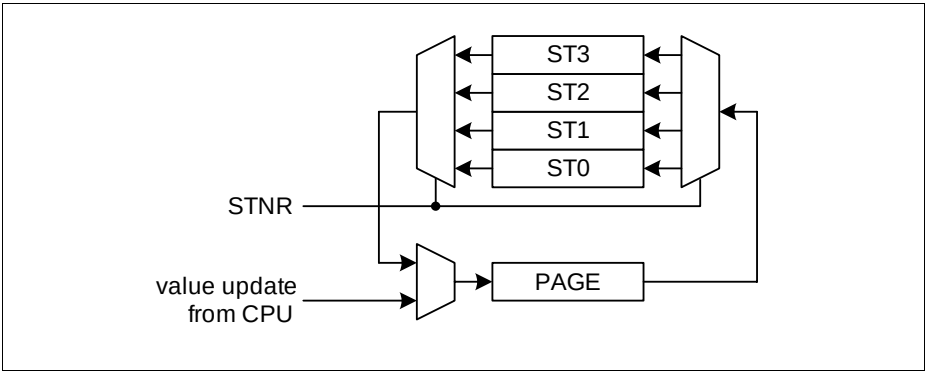



**Figure 10 Storage Elements for Paging**

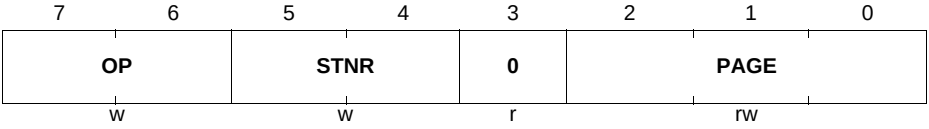
With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The SAA-XC866 supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

The page register has the following definition:

**MOD_PAGE**
**Page Register for module MOD** **Reset Value: $00_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| **PAGE** | [2:0] | rw | **Page Bits**<br>When written, the value indicates the new page.<br>When read, the value indicates the currently active page. |
| **STNR** | [5:4] | w | **Storage Number**<br>This number indicates which storage bit field is the target of the operation defined by bit field OP.<br>If OP = $10_B$,<br>the contents of PAGE are saved in STx before being overwritten with the new value.<br>If OP = $11_B$,<br>the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored.<br><br>00 ST0 is selected.<br>01 ST1 is selected.<br>10 ST2 is selected.<br>11 ST3 is selected. |

**Table 7 System Control Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $B3_H$ | **ID** **Reset: $01_H$**<br>Identity Register | Bit Field | PRODID | | | | | VERID | | |
| | | Type | r | | | | | r | | |
| $B4_H$ | **PMCON0** **Reset: $00_H$**<br>Power Mode Control Register 0 | Bit Field | 0 | WDT RST | WKRS | WK SEL | SD | PD | WS | |
| | | Type | r | rwh | rwh | rw | rw | rwh | rw | |
| $B5_H$ | **PMCON1** **Reset: $00_H$**<br>Power Mode Control Register 1 | Bit Field | 0 | | | | T2_DIS | CCU _DIS | SSC _DIS | ADC _DIS |
| | | Type | r | | | | rw | rw | rw | rw |
| $B6_H$ | **OSC_CON** **Reset: $08_H$**<br>OSC Control Register | Bit Field | 0 | | | OSC PD | XPD | OSC SS | ORD RES | OSCR |
| | | Type | r | | | rw | rw | rw | rwh | rh |
| $B7_H$ | **PLL_CON** **Reset: $20_H$**<br>PLL Control Register | Bit Field | NDIV | | | | VCO BYP | OSC DISC | RESLD | LOCK |
| | | Type | rw | | | | rw | rw | rwh | rh |
| $BA_H$ | **CMCON** **Reset: $00_H$**<br>Clock Control Register | Bit Field | VCO SEL | 0 | | | CLKREL | | | |
| | | Type | rw | r | | | rw | | | |
| $BB_H$ | **PASSWD** **Reset: $07_H$**<br>Password Register | Bit Field | PASS | | | | | PROTE CT_S | MODE | |
| | | Type | w | | | | | rh | rw | |
| $BC_H$ | **FEAL** **Reset: $00_H$**<br>Flash Error Address Register Low | Bit Field | ECCERRADDR[7:0] | | | | | | | |
| | | Type | rh | | | | | | | |
| $BD_H$ | **FEAH** **Reset: $00_H$**<br>Flash Error Address Register High | Bit Field | ECCERRADDR[15:8] | | | | | | | |
| | | Type | rh | | | | | | | |
| $BE_H$ | **COCON** **Reset: $00_H$**<br>Clock Output Control Register | Bit Field | 0 | | TLEN | COUT S | COREL | | | |
| | | Type | r | | rw | rw | rw | | | |
| $E9_H$ | **MISC_CON** **Reset: $00_H$**<br>Miscellaneous Control Register | Bit Field | 0 | | | | | | | DFLAS HEN |
| | | Type | r | | | | | | | rwh |
| RMAP = 0, Page 3 | | | | | | | | | | |
| $B3_H$ | **XADDRH** **Reset: $F0_H$**<br>On-Chip XRAM Address Higher Order | Bit Field | ADDRH | | | | | | | |
| | | Type | rw | | | | | | | |

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

**Table 8 WDT Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 1 | | | | | | | | | | |
| $BB_H$ | **WDTCON** **Reset: $00_H$**<br>Watchdog Timer Control Register | Bit Field | 0 | | WINB EN | WDT PR | 0 | WDT EN | WDT RS | WDT IN |
| | | Type | r | | rw | rh | r | rw | rwh | rw |
| $BC_H$ | **WDTREL** **Reset: $00_H$**<br>Watchdog Timer Reload Register | Bit Field | WDTREL | | | | | | | |
| | | Type | rw | | | | | | | |
| $BD_H$ | **WDTWINB** **Reset: $00_H$**<br>Watchdog Window-Boundary Count Register | Bit Field | WDTWINB | | | | | | | |
| | | Type | rw | | | | | | | |
| $BE_H$ | **WDTL** **Reset: $00_H$**<br>Watchdog Timer Register Low | Bit Field | WDT[7:0] | | | | | | | |
| | | Type | rh | | | | | | | |
| $BF_H$ | **WDTH** **Reset: $00_H$**<br>Watchdog Timer Register High | Bit Field | WDT[15:8] | | | | | | | |
| | | Type | rh | | | | | | | |

## 3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC866 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

### 3.4.1 Interrupt Source

**Figure 13** to **Figure 17** give a general overview of the interrupt sources and illustrates the request and control flags.

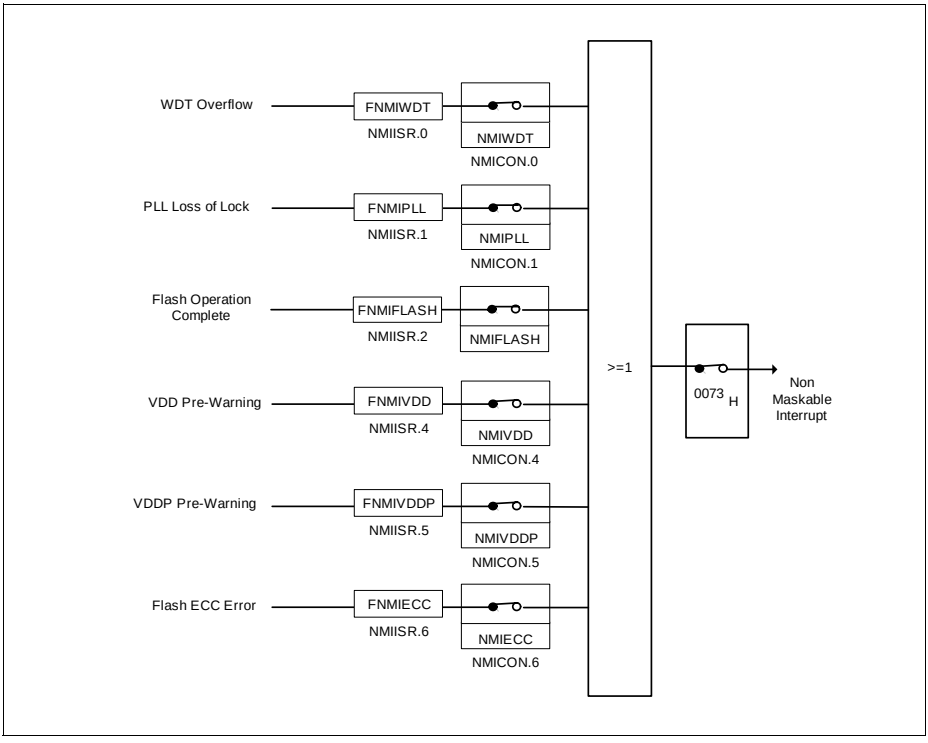



**Figure 13 Non-Maskable Interrupt Request Sources**

## 3.6 Power Supply System with Embedded Voltage Regulator

The SAA-XC866 microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

**Figure 20** shows the SAA-XC866 power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

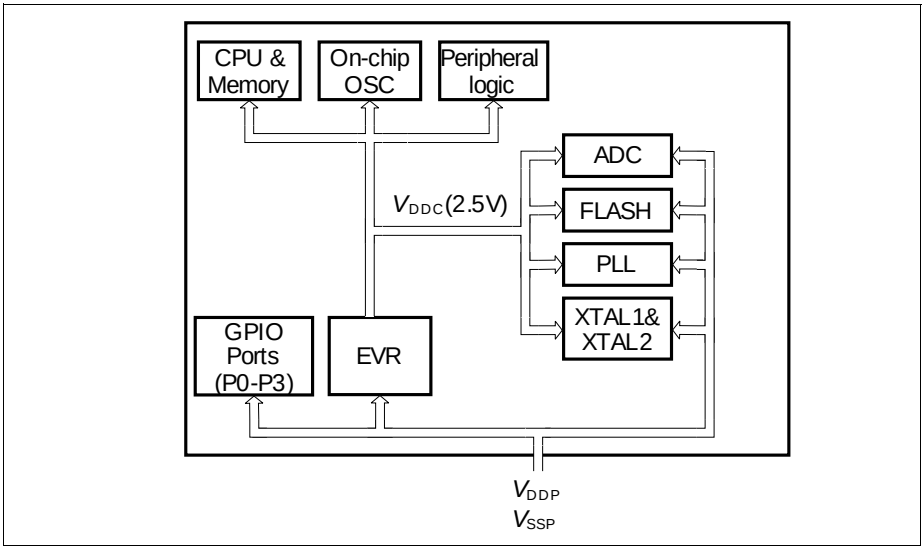



**Figure 20 SAA-XC866 Power Supply System**

**EVR Features:**

- Input voltage ($V_{DDP}$): 3.3 V/5.0 V
- Output voltage ($V_{DDC}$): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- $V_{DDC}$ and $V_{DDP}$ prewarning detection
- $V_{DDC}$ brownout detection

## 3.7 Reset Control

The SAA-XC866 has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the SAA-XC866 is first powered up, the status of certain pins (see **Table 19**) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

In order to power up the system properly, the external reset pin $\overline{\text{RESET}}$ must be asserted until $V_{DDC}$ reaches 0.9*$V_{DDC}$. The delay of external reset can be realized by an external capacitor at $\overline{\text{RESET}}$ pin. This capacitor value must be selected so that $V_{RESET}$ reaches 0.4 V, but not before $V_{DDC}$ reaches 0.9* $V_{DDC}$.

A typical application example is shown in **Figure 21**. $V_{DDP}$ capacitor value is 300 nF. $V_{DDC}$ capacitor value is 220 nF. The capacitor connected to $\overline{\text{RESET}}$ pin is 100 nF.

Typically, the time taken for $V_{DDC}$ to reach 0.9*$V_{DDC}$ is less than 50 µs once $V_{DDP}$ reaches 2.3V. Hence, based on the condition that 10% to 90% $V_{DDP}$ (slew rate) is less than 500 µs, the $\overline{\text{RESET}}$ pin should be held low for 500 µs typically. See **Figure 22**.

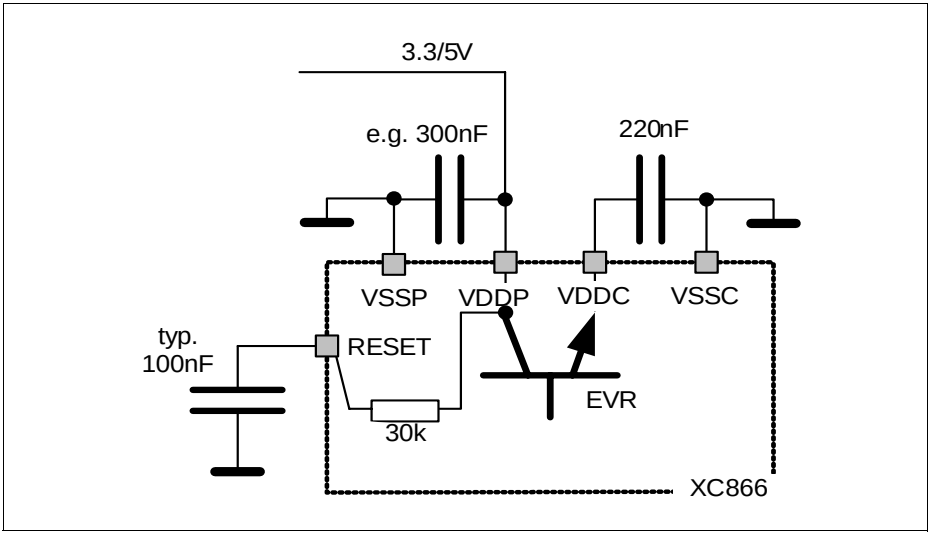



**Figure 21 Reset Circuitry**

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert WDTTO) and the reset prewarning is entered. The prewarning period lasts for $30_H$ count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from $0000_H$ to the value obtained from the concatenation of WDTWINB and $00_H$.

After being serviced, the WDT continues counting up from the value (<WDTREL> * $2^8$). The time period for an overflow of the WDT is programmable in two ways:

- the input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- the reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, $P_{WDT}$, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period $P_{WDT}$ between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 28**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB should not be smaller than WDTREL.

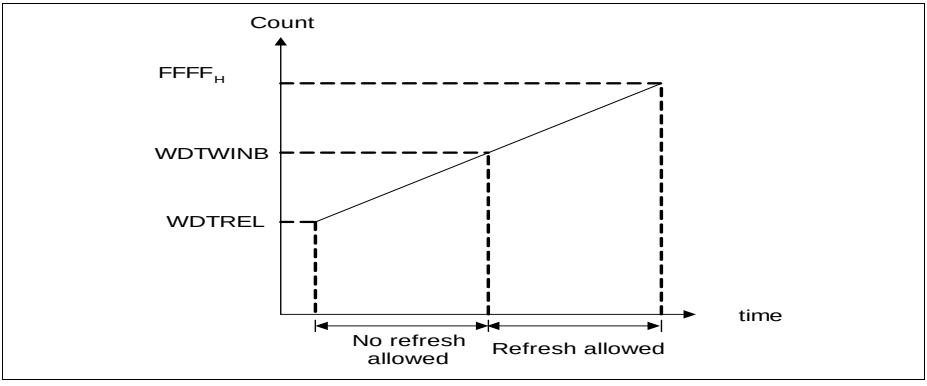



**Figure 28 WDT Timing Diagram**

- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

The following formulas calculate the final baud rate without and with the fractional divider respectively:

$$\text{baud rate} = \frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (\text{BR\_VALUE} + 1)} \quad \text{where} \quad 2^{BRPRE} \times (\text{BR\_VALUE} + 1) > 1$$

$$\text{baud rate} = \frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (\text{BR\_VALUE} + 1)} \times \frac{STEP}{256}$$

The maximum baud rate that can be generated is limited to $f_{PCLK}/32$. Hence, for a module clock of 26.7 MHz, the maximum achievable baud rate is 0.83 MBaud.

Standard LIN protocol can support a maximum baud rate of 20kHz, the baud rate accuracy is not critical and the fractional divider can be disabled. Only the prescaler is used for auto baud rate calculation. For LIN fast mode, which supports the baud rate of 20kHz to 115.2kHz, the higher baud rates require the use of the fractional divider for greater accuracy.

**Table 26** lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 26.7 MHz is used.

**Table 26 Typical Baud rates for UART with Fractional Divider disabled**

| Baud rate | Prescaling Factor ($2^{BRPRE}$) | Reload Value (BR_VALUE + 1) | Deviation Error |
|---|---|---|---|
| 19.2 kBaud | 1 (BRPRE=$000_B$) | 87 ($57_H$) | -0.22 % |
| 9600 Baud | 1 (BRPRE=$000_B$) | 174 ($AE_H$) | -0.22 % |
| 4800 Baud | 2 (BRPRE=$001_B$) | 174 ($AE_H$) | -0.22 % |
| 2400 Baud | 4 (BRPRE=$010_B$) | 174 ($AE_H$) | -0.22 % |

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. **Table 27** lists the resulting deviation errors from generating a baud rate of 115.2 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

### 3.11.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

[3.1]

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times f_{PCLK}}{32 \times 2 \times (256 - TH1)}$$

## 3.12 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 29**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock $f_{MOD}$ that is 1/n of the input clock $f_{DIV}$, where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

[3.2]

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP}$$

## 3.13 LIN Protocol

The UART can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in **Figure 30**. The frame consists of the:

- header, which comprises a Break (13-bit time low), Synch Byte ($55_H$), and ID field
- response time
- data bytes (according to UART protocol)
- checksum

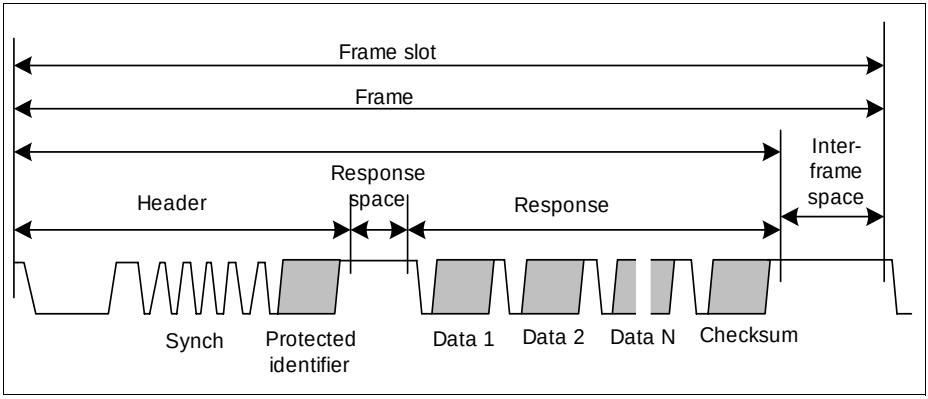



**Figure 30 Structure of LIN Frame**

### 3.13.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data.

The break must contain a dominant value of 13 bits or more to ensure proper synchronization of slave nodes.

In the LIN communication, a slave task is required to be synchronized at the beginning of the protected identifier field of frame. For this purpose, every frame starts with a sequence consisting of a break field followed by a synch byte field. This sequence is unique and provides enough information for any slave task to detect the beginning of a new frame and be synchronized at the start of the identifier field.

Upon entering LIN communication, a connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

STEP 1: Initialize interface for reception and timer for baud rate measurement

STEP 2: Wait for an incoming LIN frame from host

STEP 3: Synchronize the baud rate to the host

STEP 4: Enter for Master Request Frame or for Slave Response Frame

*Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header LIN frame.*

## 3.15 Timer 0 and Timer 1

Timers 0 and 1 are count-up timers which are incremented every machine cycle, or in terms of the input clock, every 2 PCLK cycles. They are fully compatible and can be configured in four different operating modes for use in a variety of applications, see **Table 28**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

**Table 28 Timer 0 and Timer 1 Modes**

| Mode | Operation |
|---|---|
| **0** | **13-bit timer**<br>The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices. |
| **1** | **16-bit timer**<br>The timer registers, TLx and THx, are concatenated to form a 16-bit counter. |
| **2** | **8-bit timer with auto-reload**<br>The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow. |
| **3** | **Timer 0 operates as two 8-bit timers**<br>The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled. |

### 4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the SAA-XC866 can be subjected to without permanent damage.

**Table 32 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Ambient temperature | $T_A$ | -40 | 140 | °C | under bias |
| Storage temperature | $T_{ST}$ | -65 | 150 | °C | 1) |
| Junction temperature | $T_J$ | -40 | 150 | °C | under bias1) |
| Voltage on power supply pin with respect to $V_{SS}$ | $V_{DDP}$ | -0.5 | 6 | V | 1) |
| Voltage on core supply pin with respect to $V_{SS}$ | $V_{DDC}$ | -0.5 | 3.25 | V | 1) |
| Voltage on any pin with respect to $V_{SS}$ | $V_{IN}$ | -0.5 | $V_{DDP}$ + 0.5 or max. 6 | V | Whichever is lower1) |
| Input current on any pin during overload condition | $I_{IN}$ | -10 | 10 | mA | 1) |
| Absolute sum of all input currents during overload condition | $\Sigma\|I_{IN}\|$ | – | 50 | mA | 1) |

1) Not subjected to production test, verified by design/characterization.

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DDP}$ pin with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.*

**Table 34 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Input low voltage at XTAL1 | $V_{ILX}$ | SR | $V_{SS}$ - 0.5 | 0.3 × $V_{DDC}$ | V | |
| Input high voltage at XTAL1 | $V_{IHX}$ | SR | 0.7 × $V_{DDC}$ | $V_{DDC}$ + 0.5 | V | |
| Pull-up current | $I_{PU}$ | SR | – | -10 | µA | $V_{IH,min}$ |
| | | | -150 | – | µA | $V_{IL,max}$ |
| Pull-down current | $I_{PD}$ | SR | – | 10 | µA | $V_{IL,max}$ |
| | | | 150 | – | µA | $V_{IH,min}$ |
| Input leakage current[2)] | $I_{OZ1}$ | CC | -2 | 2 | µA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 140°C$ |
| Input current at XTAL1 | $I_{ILX}$ | CC | -10 | 10 | µA | |
| Overload current on any pin | $I_{OV}$ | SR | -5 | 5 | mA | [3)] |
| Absolute sum of overload currents | $\Sigma\|I_{OV}\|$ | SR | – | 25 | mA | [3)] |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | [4)] |
| Maximum current per pin (excluding $V_{DDP}$ and $V_{SS}$) | $I_M$ | SR | – | 15 | mA | |
| Maximum current for all pins (excluding $V_{DDP}$ and $V_{SS}$) | $\Sigma\|I_M\|$ | SR | – | 60 | mA | |
| Maximum current into $V_{DDP}$ | $I_{MVDDP}$ | SR | – | 80 | mA | [3)] |
| Maximum current out of $V_{SS}$ | $I_{MVSS}$ | SR | – | 80 | mA | [3)] |

### 4.2.2 Supply Threshold Characteristics

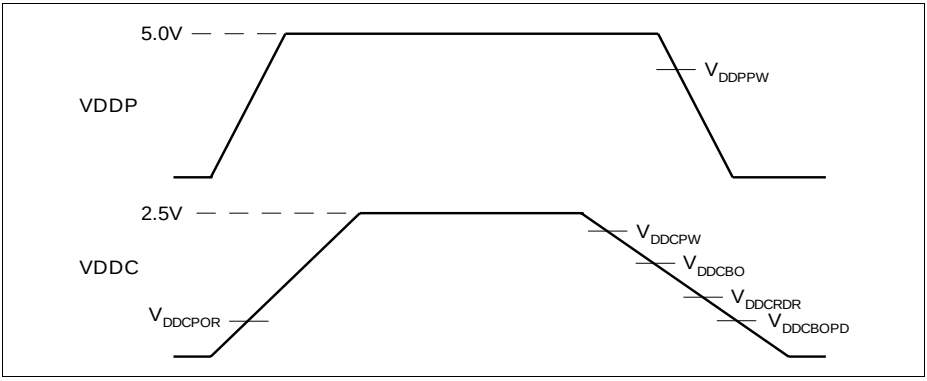



**Figure 36 Supply Threshold Parameters**

**Table 35 Supply Threshold Parameters (Operating Conditions apply)**

| Parameters | Symbol | | Limit Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| $V_{DDC}$ prewarning voltage[1] | $V_{DDCPW}$ | CC | 2.2 | 2.3 | 2.4 | V |
| $V_{DDC}$ brownout voltage in active mode[1] | $V_{DDCBO}$ | CC | 2.0 | 2.1 | 2.2 | V |
| RAM data retention voltage | $V_{DDCRDR}$ | CC | 0.9 | 1.0 | 1.1 | V |
| $V_{DDC}$ brownout voltage in power-down mode[2] | $V_{DDCBOPD}$ | CC | 1.3 | 1.5 | 1.7 | V |
| $V_{DDP}$ prewarning voltage[3] | $V_{DDPPW}$ | CC | 3.3 | 4.0 | 4.65 | V |
| Power-on reset voltage[2][4] | $V_{DDCPOR}$ | CC | 1.3 | 1.5 | 1.7 | V |

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

3) Detection is enabled for external power supply of 5.0V
Detection must be disabled for external power supply of 3.3V.

4) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.

**Table 38 Power Down Current (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | typ.[1] | max.[2] | | |
| Power-Down Mode[3] | $I_{PDP}$ | 1 | 10 | µA | $T_A$ = + 25 °C.[4] |
| | | - | 30 | µA | $T_A$ = + 85 °C.[4][5] |

1) The typical $I_{PDP}$ values are measured at $V_{DDP}$ = 5.0 V.

2) The maximum $I_{PDP}$ values are measured at $V_{DDP}$ = 5.5 V.

3) $I_{PDP}$ (power-down mode) has a maximum value of 400 µA at $T_A$ = + 140 °C.

4) $I_{PDP}$ (power-down mode) is measured with: $\overline{\text{RESET}}$ = $V_{DDP}$, $V_{AGND}$= $V_{SS}$, RXD/INT0 = $V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subject to production test, verified by design/characterization.

## 5.3 Quality Declaration

Table 46 shows the characteristics of the quality parameters in the SAA-XC866.

**Table 46 Quality Parameters**

| Parameter | Symbol | Limit Values | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation Lifetime when the device is used at the four stated $T_A$ [1)2)] | $t_{OP}$ | – | – | 1500 | hours | $T_A$= 140°C |
| | | – | – | 2000 | hours | $T_A$= 125°C |
| | | – | – | 10000 | hours | $T_A$= 85°C |
| | | – | – | 1500 | hours | $T_A$= -40°C |
| Operation Lifetime when the device is used at the two stated $T_A$ [1)2)] | $t_{OP2}$ | – | – | 18000 | hours | $T_A$= 108°C |
| | | – | – | 130000 | hours | $T_A$= 27°C |
| Weighted Average Temperature [2)3)] | $T_{WA}$ | – | 106 | – | °C | for 15000 hours |
| ESD susceptibility according to Human Body Model (HBM) for all pins (except $V_{DDC}$) [2)] | $V_{HBM}$ | – | – | 2000 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Human Body Model (HBM) for $V_{DDC}$ [2)] | $V_{HBMC}$ | – | – | 600 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) pins [2)] | $V_{CDM}$ | – | – | 750 | V | Conforming to JESD22-C101-C |

1) This lifetime refers only to the time when the device is powered-on.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) This parameter is derived based on the Arrhenius model.