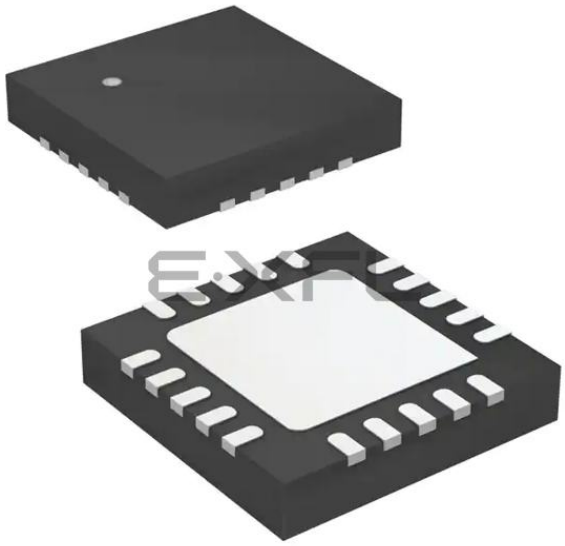

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	12
Program Memory Size	2KB (1K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN-EP (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny24a-mu

4 Flash programmable memory

4.1 Introduction

The ST7 single voltage extended Flash (XFlash) is a non-volatile memory that can be electrically erased and programmed either on a byte-by-byte basis or up to 32 bytes in parallel.

The XFlash devices can be programmed off-board (plugged in a programming tool) or on-board using In-Circuit Programming or In-Application Programming.

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Sector 0 size configurable by option byte
- Read-out and write protection

4.3 Programming modes

The ST7 can be programmed in three different ways:

- Insertion in a programming tool. In this mode, Flash sectors 0 and 1, option byte row can be programmed or erased.
- In-Circuit Programming. In this mode, Flash sectors 0 and 1, option byte row can be programmed or erased without removing the device from the application board.
- In-Application Programming. In this mode, sector 1 can be programmed or erased without removing the device from the application board and while the application is running.

4.3.1 In-Circuit Programming (ICP)

ICP uses a protocol called ICC (In-Circuit Communication) which allows an ST7 plugged on a printed circuit board (PCB) to communicate with an external programming device connected via cable. ICP is performed in three steps:

Switch the ST7 to ICC mode (In-Circuit Communications). This is done by driving a specific signal sequence on the ICCCLK/DATA pins while the $\overline{\text{RESET}}$ pin is pulled low. When the ST7 enters ICC mode, it fetches a specific Reset vector which points to the ST7 System Memory containing the ICC protocol routine. This routine enables the ST7 to receive bytes from the ICC interface.

- Download ICP Driver code in RAM from the ICCDATA pin
- Execute ICP Driver code in RAM to program the Flash memory

4.7 Description of Flash Control/Status register (FCSR)

This register controls the XFlash erasing and programming using ICP, IAP or other programming methods.

1st RASS Key: 0101 0110 (56h)

2nd RASS Key: 1010 1110 (AEh)

When an EPB or another programming tool is used (in socket or ICP mode), the RASS keys are sent automatically.

Reset value: 000 0000 (00h)

7							0
0	0	0	0	0	OPT	LAT	PGM
Read/write							

Table 5. Flash register mapping and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0034	FCSR Reset Value	- 0	- 0	- 0	- 0	- 0	OPT 0	LAT 0	PGM 0

6.2.1 External clock source

In this external clock mode, a clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC1 pin while the OSC2 pin is tied to ground.

Note: When the Multi-Oscillator is not used OSCI1 and OSCI2 must be tied to ground, and PB1 is selected by default as the external clock.

6.2.2 Crystal/ceramic oscillators

In this mode, with a self-controlled gain feature, oscillator of any frequency from 1 to 16 MHz can be placed on OSC1 and OSC2 pins. This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator start-up phase.

6.2.3 Internal RC oscillator

In this mode, the tunable RC oscillator is used as main clock source. The two oscillator pins have to be tied to ground.

The calibration is done through the RCCRH[7:0] and RCCRL[6:5] registers.

Table 8. ST7 clock sources

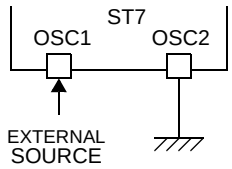
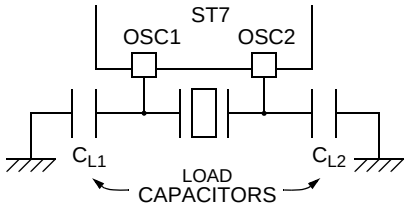
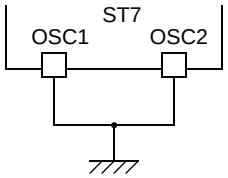
	Hardware configuration
External Clock	

Table 8. ST7 clock sources

	Hardware configuration
Crystal/Ceramic Resonators	
Internal RC Oscillator	

6.3 Reset sequence manager (RSM)

6.3.1 Introduction

The reset sequence manager includes three RESET sources as shown in *Figure 14*:

- External $\overline{\text{RESET}}$ source pulse
- Internal LVD RESET (Low Voltage Detection)
- Internal WATCHDOG RESET

Note: A reset can also be triggered following the detection of an illegal opcode or prebyte code. Refer to Section 11.2.1 on page 184 for further details.

These sources act on the $\overline{\text{RESET}}$ pin and it is always kept low during the delay phase.

The RESET service routine vector is fixed at addresses FFFEh-FFFFh in the ST7 memory mapping.

The basic RESET sequence consists of 3 phases as shown in *Figure 13*:

- Active Phase depending on the RESET source
- 256 or 4096 CPU clock cycle delay (see *Table 13*)

Caution: When the ST7 is unprogrammed or fully erased, the Flash is blank and the Reset vector is not programmed. For this reason, it is recommended to keep the $\overline{\text{RESET}}$ pin in low state until programming mode is entered, in order to avoid unwanted behavior.

The 256 or 4096 CPU clock cycle delay allows the oscillator to stabilize and ensures that recovery has taken place from the Reset state. The shorter or longer clock cycle delay is automatically selected depending on the clock source chosen by option byte.

The Reset vector fetch phase duration is 2 clock cycles.

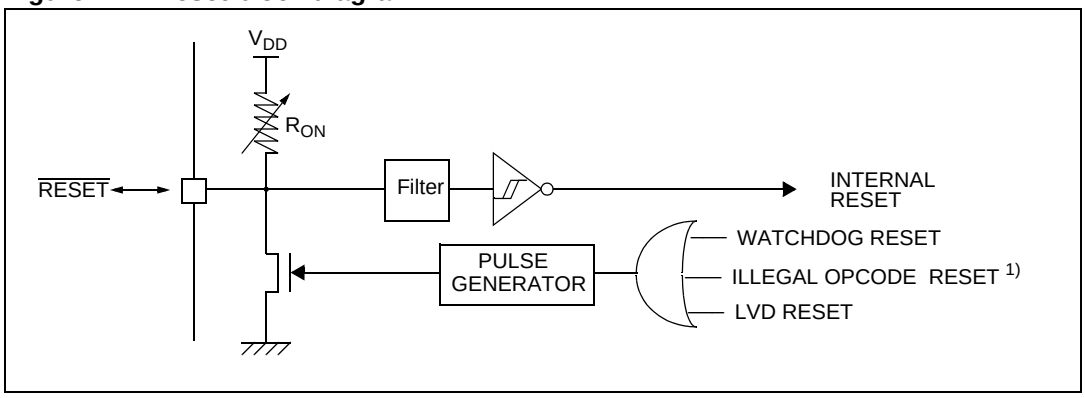
6.3.2 Asynchronous external $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ pin is both an input and an open-drain output with integrated R_{ON} weak pull-up resistor. This pull-up has no fixed value but varies in accordance with the input voltage. It can be pulled low by external circuitry to reset the device. See Electrical Characteristic section for more details.

A RESET signal originating from an external source must have a duration of at least $t_{h(RSTL)in}$ in order to be recognized (see *Figure 15: Reset sequences*). This detection is asynchronous and therefore the MCU can enter reset state even in Halt mode.

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

Figure 14. Reset block diagram



1. See *Section 11.2.1: Illegal opcode reset on page 184* for more details on illegal opcode reset conditions.

6.3.3 External power-on reset

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

6.3.4 Internal Low Voltage Detector (LVD) reset

Two different Reset sequences caused by the internal LVD circuitry can be distinguished:

- Power-On reset
- Voltage Drop reset

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when V_{DD} is lower than V_{IT+} (rising edge) or V_{DD} lower than V_{IT-} (falling edge) as shown in *Figure 15.*

The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

Table 18. ST7FOXK2 interrupt mapping

Number	Source block	Description	Register label	Priority order	Exit from HALT or AWUFH (1)	Address vector
	RESET	Reset	N/A	Highest Priority	yes	FFFEh-FFFFh
	TRAP	Software interrupt			no	FFFCh-FFFDh
0	AWU	Auto Wake Up interrupt	AWUCSR		yes (2)	FFFAh-FFFBh
1	Reserved				-	FFF8h-FFF9h
2	Reserved				-	FFF6h-FFF7h
3	Reserved				-	FFF4h-FFF5h
4	ei0	External interrupt 0 (Port A)	N/A		yes	FFF2h-FFF3h
5	ei1	External interrupt 1 (Port B)				FFF0h-FFF1h
6	ei2	External interrupt 2 (Port C)				FFEEh-FFEFh
7	AT TIMER	AT timer input Capture/Output Compare interrupt	ATCSR		no	FFECh-FFEDh
8(3)		AT timer overflow 1 interrupt			no	FFEAh-FFEBh
9		AT timer Overflow 2 interrupt			no	FFE8h-FFE9h
10	I^2C	I^2C interrupt	I2CSR1/ I2CSR2		no	FFE6h-FFE7h
11	SPI	SPI interrupt	SPICSR	Lowest Priority	no	FFE4h-FFE5h
12	TIM16	16-bit timer peripheral interrupt	TACSR		no	FFE2h-FFE3h
13(3)	LITE TIMER	Lite timer RTC/IC/RTC2 interrupt	LTCSR2		yes	FFE0h-FFE1h

1. For an interrupt, all events do not have the same capability to wake up the MCU from Halt, Active-Halt or Auto-wakeup from Halt modes. Refer to the description of interrupt events for more details.
2. This interrupt exits the MCU from Auto-wakeup from Halt mode only.
3. These interrupts exit the MCU from Active-Halt mode only.

7.5.3 External Interrupt Control register (EICR)

Reset value: 0000 0000 (00h)

7							0
0	0	IS21	IS20	IS11	IS10	IS01	IS00
Read/write							

Bits 7:6 = Reserved, must be kept cleared.

Bits 5:4 = **IS2[1:0]** *ei2 sensitivity bits*

These bits define the interrupt sensitivity for ei2 (Port C) according to *Table 19*.

Bits 3:2 = **IS1[1:0]** *ei1 sensitivity bits*

These bits define the interrupt sensitivity for ei1 (Port B) according to *Table 19*.

Bits 1:0 = **IS0[1:0]** *ei0 sensitivity bits*

These bits define the interrupt sensitivity for ei0 (Port A) according to *Table 19*.

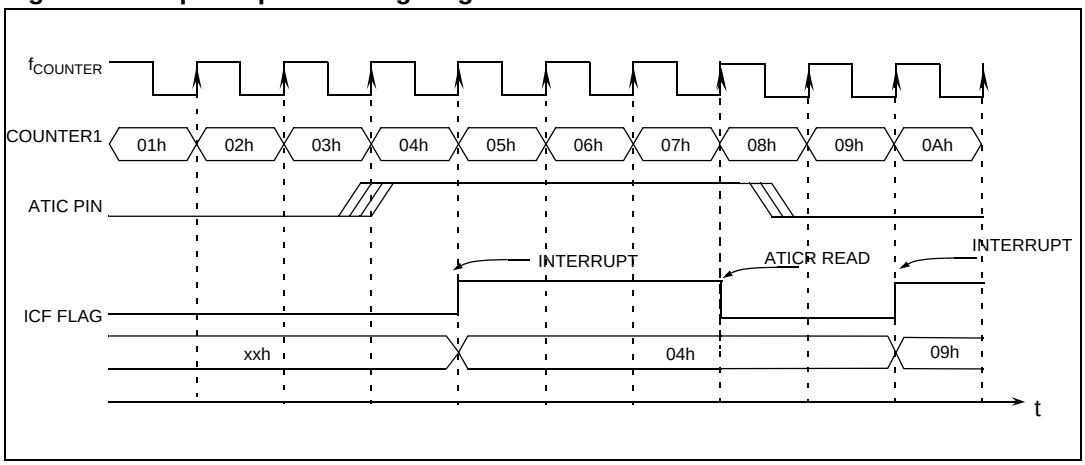
Note: 1 These 8 bits can be written only when the I bit in the CC register is set.

2 Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts. Refer to Section : External interrupt function.

Table 19. Interrupt sensitivity bits

ISx1	ISx0	External interrupt sensitivity
0	0	Falling edge & low level
0	1	Rising edge only
1	0	Falling edge only
1	1	Rising and falling edge

Figure 45. Input capture timing diagram



Long range input capture

Pulses that last more than 8 µs can be measured with an accuracy of 4 µs if f_{OSC} equals 8 MHz in the following conditions:

- The 12-bit AT4 timer is clocked by the Lite timer (RTC pulse: CK[1:0] = 01 in the ATCSR register)
- The ICS bit in the ATCSR2 register is set so that the LTIC pin is used to trigger the AT4 timer capture.
- The signal to be captured is connected to LTIC pin
- Input Capture registers LTICR, ATICRH and ATICRL are read

This configuration allows to cascade the Lite timer and the 12-bit AT4 timer to get a 20-bit Input Capture value. Refer to *Figure 46*.

Figure 46. Long range input capture block diagram

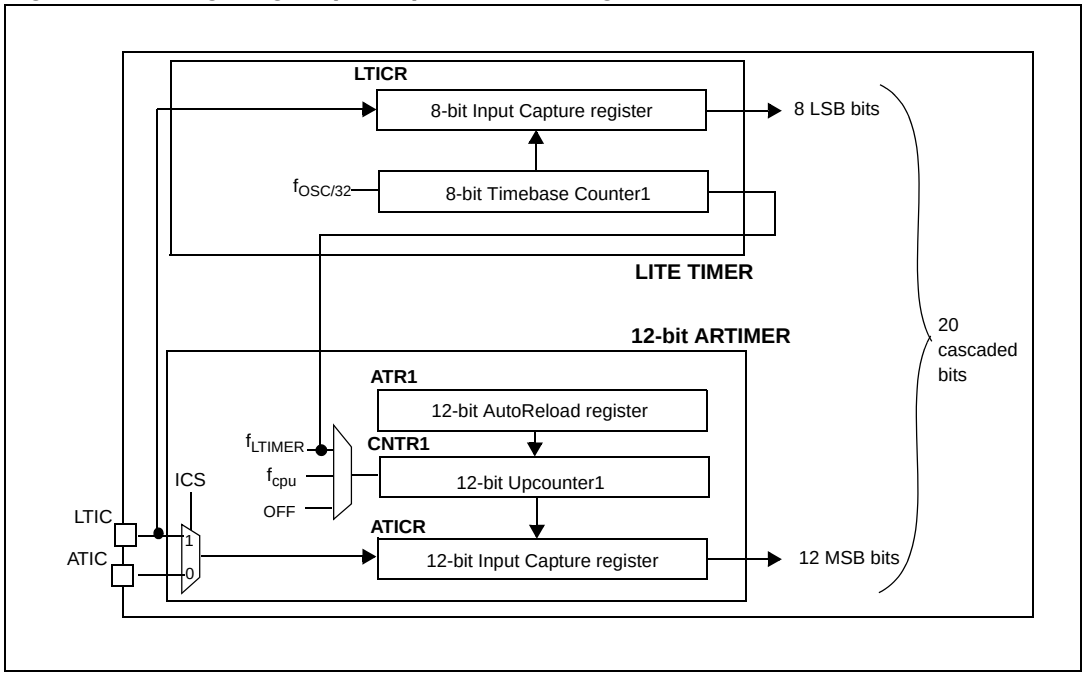


Figure 47. Long range input capture timing diagram

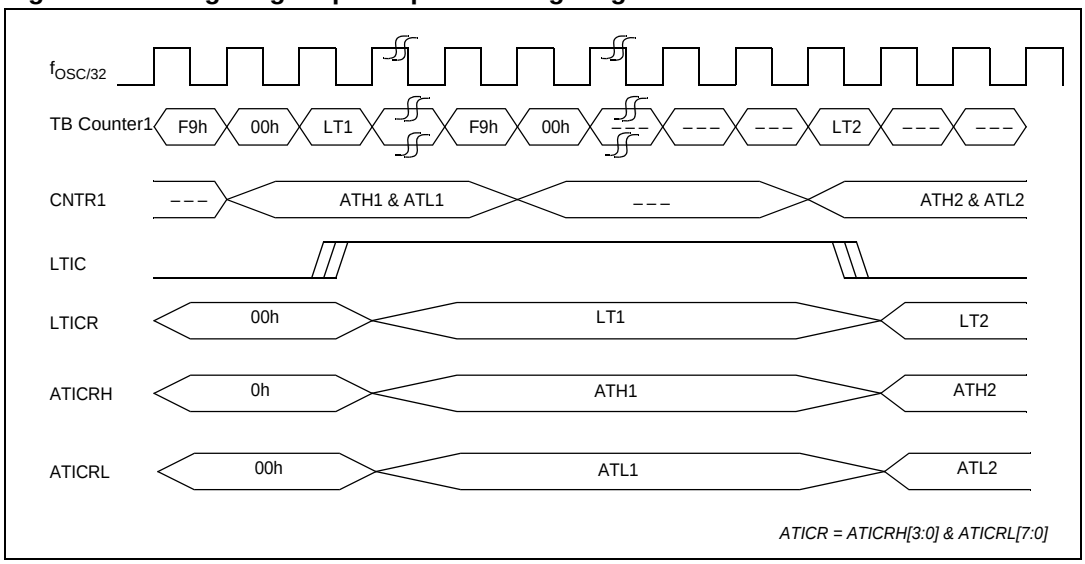
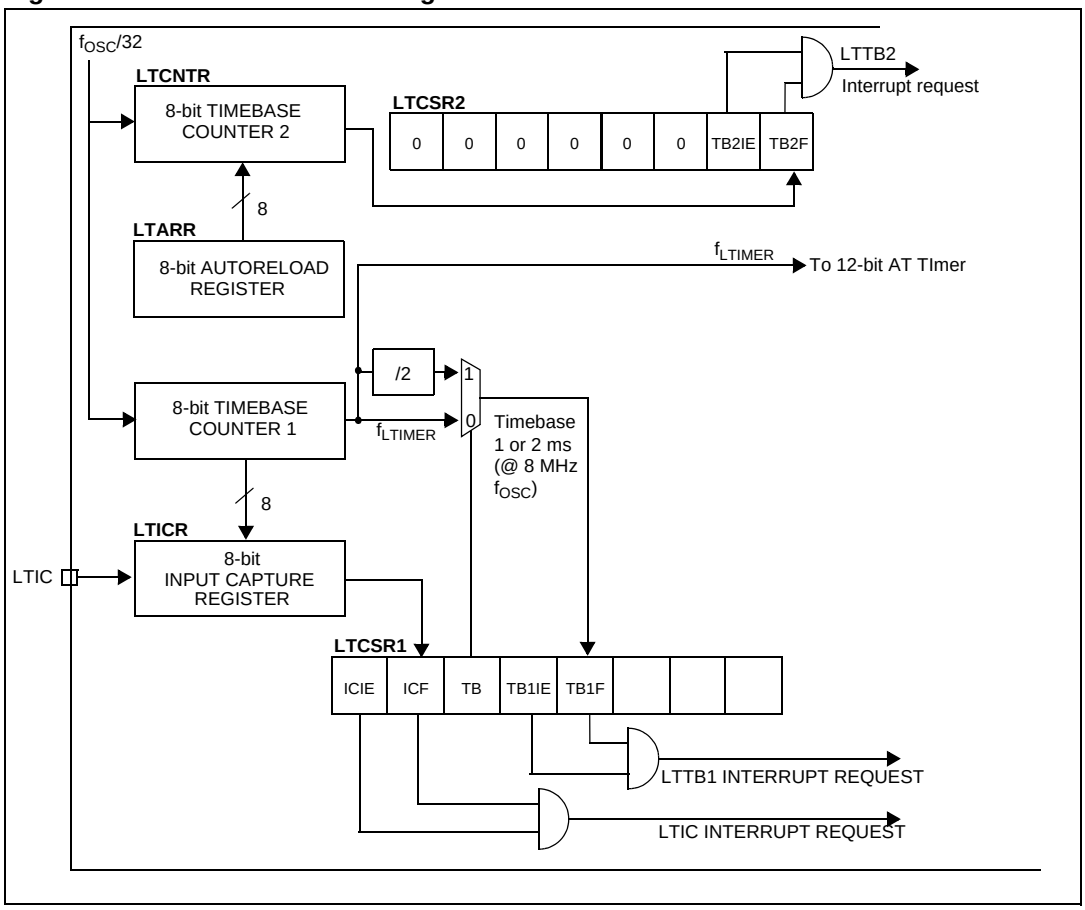


Figure 52. Lite timer 2 block diagram



10.3.3 Functional description

Timebase Counter 1

The 8-bit value of Counter 1 cannot be read or written by software. After an MCU reset, it starts incrementing from 0 at a frequency of $f_{OSC}/32$. An overflow event occurs when the counter rolls over from F9h to 00h. If f_{OSC} = 8 MHz, then the time period between two counter overflow events is 1 ms. This period can be doubled by setting the TB bit in the LTCSR1 register.

When Counter 1 overflows, the TB1F bit is set by hardware and an interrupt request is generated if the TB1IE bit is set. The TB1F bit is cleared by software reading the LTCSR1 register.

Input Capture

The 8-bit Input Capture register is used to latch the free-running upcounter (Counter 1) 1 after a rising or falling edge is detected on the LTIC pin. When an Input Capture occurs, the ICF bit is set and the LTICR register contains the counter 1 value. An interrupt is generated if the ICIE bit is set. The ICF bit is cleared by reading the LTICR register.

The LTICR is a read-only register and always contains the data from the last Input Capture. Input Capture is inhibited if the ICF bit is set.

Timer A Output compare 1 high register (TAOC1HR)

Reset value: 1000 0000 (80h)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

7							0
MSB							LSB
Read / Write							

Timer A Output compare 1 low register (TAOC1LR)

Reset value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

7							0
MSB							LSB
Read / Write							

Output compare 2 high register (OC2HR)

Reset value: 1000 0000 (80h)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

7							0
MSB							LSB
Read / Write							

Output compare 2 low register (OC2LR)

Reset value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

7							0
MSB							LSB
Read / Write							

Counter high register (CHR)

Reset value: 1111 1111 (FFh)

This is an 8-bit read-only register that contains the high part of the counter value.

7							0
MSB							LSB
Read Only							

Counter low register (CLR)

Reset value: 1111 1100 (FCh)

This is an 8-bit read-only register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after accessing the CSR register clears the TOF bit.

7							0
MSB							LSB
Read Only							

Alternate counter high register (ACHR)

Reset value: 1111 1111 (FFh)

This is an 8-bit read-only register that contains the high part of the counter value.

7							0
MSB							LSB
Read Only							

Alternate counter low register (ACLR)

Reset value: 1111 1100 (FCh)

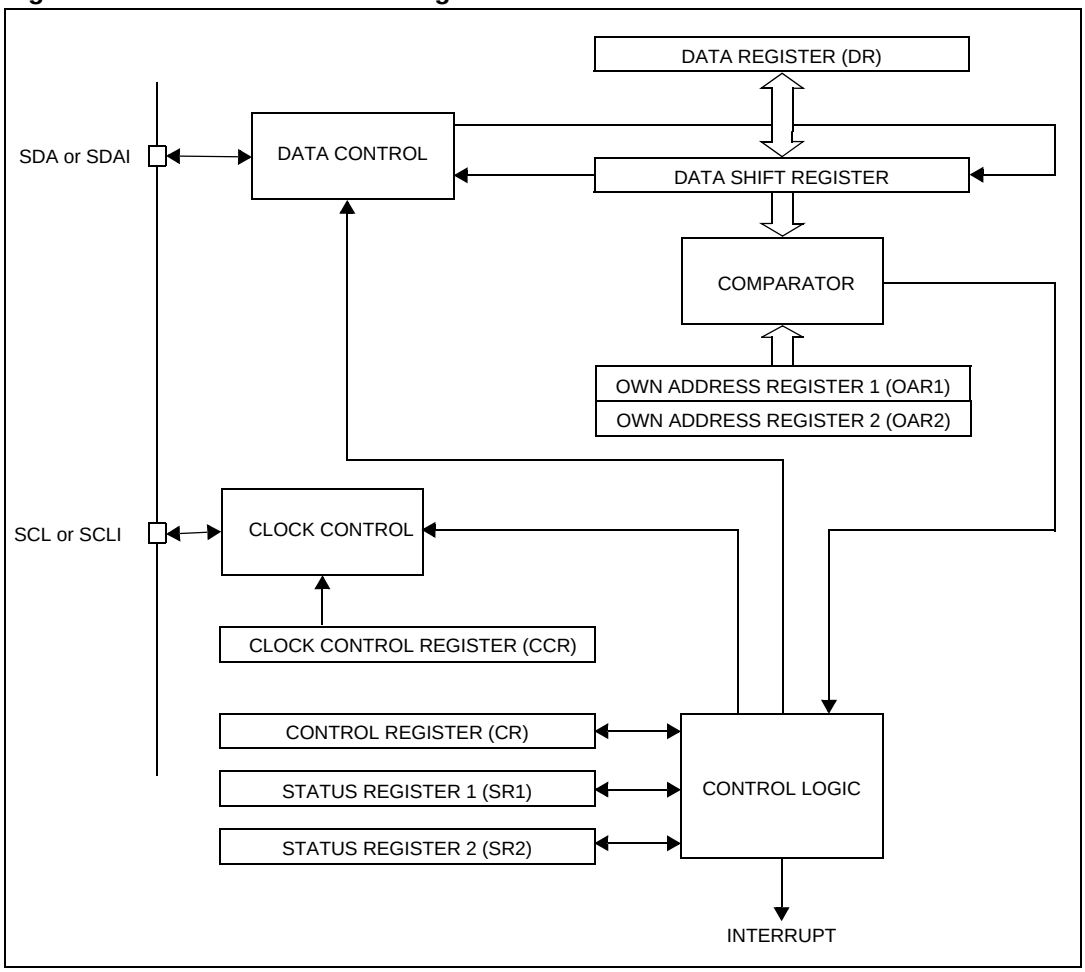
This is an 8-bit read-only register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to CSR register does not clear the TOF bit in the CSR register.

7							0
MSB							LSB
Read Only							

When the I²C cell is enabled, the SDA and SCL ports must be configured as floating inputs. In this case, the value of the external pull-up resistor used depends on the application.

When the I²C cell is disabled, the SDA and SCL ports revert to being standard I/O port pins.

Figure 70. I²C interface block diagram



Master transmitter

Following the address transmission and after SR1 register has been read, **the master sends bytes from** the DR register to **the SDA line** via the internal shift register.

The master waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see *Figure 71* Transfer sequencing EV8).

When the acknowledge bit is received, the interface sets EVF and BTF bits with an interrupt if the ITE bit is set.

To close the communication: after writing the last byte to the DR register, set the STOP bit to generate the Stop condition. The interface goes automatically back to slave mode (M/SL bit cleared).

Error cases

- **BERR**: Detection of a Stop or a Start condition during a byte transfer. In this case, the EVF and BERR bits are set by hardware with an interrupt if ITE is set.
  Note that BERR will not be set if an error is detected during the first pulse of each 9-bit transaction:
  Single Master mode
  If a Start or Stop is issued during the first pulse of a 9-bit transaction, the BERR flag will not be set and transfer will continue however the BUSY flag will be reset. To work around this, slave devices should issue a NACK when they receive a misplaced Start or Stop. The reception of a NACK or BUSY by the master in the middle of communication gives the possibility to reinitiate transmission.
  Multimaster mode
  Normally the BERR bit would be set whenever unauthorized transmission takes place while transfer is already in progress. However, an issue will arise if an external master generates an unauthorized Start or Stop while the I^2C master is on the first pulse of a 9-bit transaction. It is possible to work around this by polling the BUSY bit during I^2C master mode transmission. The resetting of the BUSY bit can then be handled in a similar manner as the BERR flag being set.
- **AF**: Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set by hardware with an interrupt if the ITE bit is set. To resume, set the Start or Stop bit. The AF bit is cleared by reading the I2CSR2 register. However, if read before the completion of the transmission, the AF flag will be set again, thus possibly generating a new interrupt. Software must ensure either that the SCL line is back at 0 before reading the SR2 register, or be able to correctly handle a second interrupt during the 9th pulse of a transmitted byte.
- **ARLO:** Detection of an arbitration lost condition.
  In this case the ARLO bit is set by hardware (with an interrupt if the ITE bit is set and the interface goes automatically back to slave mode (the M/SL bit is cleared).

Note: In all these cases, the SCL line is not held low; however, the SDA line can remain low if the last bits transmitted are all 0. It is then necessary to release both lines by software. The SCL line is not held low while AF=1 but by other flags (SB or BTF) that are set at the same time.

I²C Status register 2 (I2CSR2)

Reset value: 0000 0000 (00h)

7							0
0	0	0	AF	STOPF	ARLO	BERR	GCAL
Read Only							

Bits 7:5 = Reserved. Forced to 0 by hardware.

Bit 4 = **AF** *Acknowledge failure* bit

This bit is set by hardware when no acknowledge is returned. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while AF=1 but by other flags (SB or BTF) that are set at the same time.

0: No acknowledge failure

1: Acknowledge failure

Bit 3 = **STOPF** *Stop detection bit (slave mode)*

This bit is set by hardware when a Stop condition is detected on the bus after an acknowledge (if ACK=1). An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while STOPF=1.

0: No Stop condition detected

1: Stop condition detected

Bit 2 = **ARLO** *Arbitration lost bit*

This bit is set by hardware when the interface loses the arbitration of the bus to another master. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

After an ARLO event the interface switches back automatically to Slave mode (M/SL=0).

The SCL line is not held low while ARLO=1.

0: No arbitration lost detected

1: Arbitration lost detected

Note: In a Multimaster environment, when the interface is configured in Master Receive mode it does not perform arbitration during the reception of the Acknowledge Bit. Mishandling of the ARLO bit from the I2CSR2 register may occur when a second master simultaneously requests the same data from the same slave and the I²C master does not acknowledge the data. The ARLO bit is then left at 0 instead of being set.

Bit 1 = **BERR** *Bus error bit*

This bit is set by hardware when the interface detects a misplaced Start or Stop condition. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while BERR=1.

0: No misplaced Start or Stop condition

1: Misplaced Start or Stop condition

Bit 1 = **SSM** *SS Management*.

This bit is set and cleared by software. When set, it disables the alternate function of the SPI SS pin and uses the SSI bit value instead. See Section Slave select management.

0: Hardware management (SS managed by external pin)

1: Software management (internal SS signal controlled by SSI bit. External SS pin free for general-purpose I/O)

Bit 0 = **SSI** *SS Internal Mode*.

This bit is set and cleared by software. It acts as a 'chip select' by controlling the level of the SS slave select signal when the SSM bit is set.

0: Slave selected

1: Slave deselected

SPI data I/O register (SPIDR)

Reset Value: Undefined

7							0
D7	D6	D5	D4	D3	D2	D1	D0
Read / Write							

The SPIDR register is used to transmit and receive data on the serial bus. In a master device, a write to this register will initiate transmission/reception of another byte.

Note: During the last clock cycle the SPIF bit is set, a copy of the received data byte in the shift register is moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read.

While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

Warning: A write to the SPIDR register places data directly into the shift register for transmission.

A read to the SPIDR register returns the value located in the buffer and not the content of the shift register (see *Figure 73*).

Table 53. SPI register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
70	SPIDR Reset Value	MSB x	x	x	x	x	x	x	LSB x
71	SPICR Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
72	SPICSR Reset Value	SPIF 0	WCOL 0	OVR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

12.8.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body model and Machine model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 85. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body model)	T_A=+25 °C	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device model)	T_A=+25 °C	500	

1. Data based on characterization results, not tested in production.

Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance.

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 86. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C	A

Bit 0 = **FMP_W** *Flash write protection*

This option indicates if the Flash program memory is write protected.

0: Write protection off

1: Write protection on

Warning: When the Flash write protection is selected, the program memory (and the option bit itself) can never be erased or programmed again.

	Option byte 0								**Option byte 1**							
	7							0	7							0
	AWUCK	OSCRANGE[2:0]			SEC1	SEC0	FMPR	FMPW	CKSEL1	CKSEL0	Res	Res	Res	LVD	WDGSW	WDGHALT
Default value	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1

Figure 96. 32-pin plastic dual in-line package, shrink 400-mil width, package outline

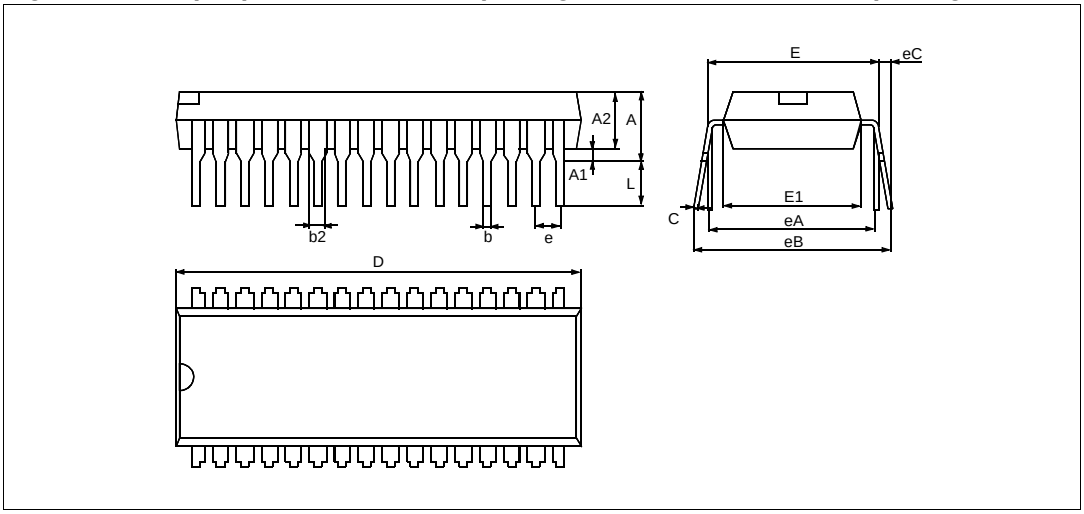


Table 99. 32-pin plastic dual in-line package, shrink 400-mil width, mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.56	3.76	5.08	0.1402	0.1480	0.2000
A1	0.51			0.0201		
A2	3.05	3.56	4.57	0.1201	0.1402	0.1799
b	0.36	0.46	0.58	0.0142	0.0181	0.0228
b1	0.76	1.02	1.40	0.0299	0.0402	0.0551
C	0.20	0.25	0.36	0.0079	0.0098	0.0142
D	27.43		28.45	1.0799		1.1201
E	9.91	10.41	11.05	0.3902	0.4098	0.4350
E1	7.62	8.89	9.40	0.3000	0.3500	0.3701
e		1.78			0.0701	
eA		10.16			0.4000	
eB			12.70			0.5000
eC			1.40			0.0551
L	2.54	3.05	3.81	0.1000	0.1201	0.1500
	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.