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# M16C/1N Group SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0002-0100Z Rev.1.00 2004.10.20

### 1. Overview

The M16C/1N group consists of single-chip microcomputers that use high-performance silicon gate CMOS processes and have a on-chip M16C/60 series CPU core. The microcomputers are housed in 48-pin plastic mold QFP package. These single-chip microcomputers have both high function instructions and high instruction efficiency and feature a one-megabyte address space and the capability to execute instructions at high speed.

# 1.1 Applications

Automotive and industrial control systems, other automobile, other



M16C/1N Group 1. Overview

# 1.2 Performance Overview

Table 1.1 gives an overview of the M16C/1N group performance specification.

**Table 1.1 Performance overview** 

	Item	Performance		
Number of bas	sic instructions	91 instructions		
Shortest instru	iction execution time	62.5 ns (when f(XIN)=16MHz)		
Memory	ROM	See Table 1.2 Performance overview		
size	RAM	See Table 1.2 Performance overview		
I/O port		P0 to P5: 37 lines		
Multifunction	T1	8 bits x 1		
timer	TX, TY, TZ	8 bits x 3		
	TC	16 bits x 1		
Serial I/O (UAR	T or clock synchronous)	x 2		
A/D converter		x 12 channels		
(maximum res	olution: 10 bits)	(Expandable up to 14 channels)		
D/A converter		8 bits x 1		
CAN controller	r	1 channel, 2.0B active		
Watchdog time	er	15 bits x 1 (with prescaler)		
Interrupts		15 internal causes, 8 external causes, 4 software causes		
Clock generati	ing circuits	3 internal circuits		
Power supply	voltage	4.2 V to 5.5V (when f(XIN)=16MHz)		
Power consum	nption	70mW(Vcc=5.0V, f(XIN)=16MHz)		
I/O	I/O withstand voltage	5V		
characteristics	Output current	5mA (10mA:LED drive port)		
Device configu	ıration	CMOS silicon gate		
Package		48-pin LQFP		

M16C/1N Group 1. Overview

# 1.4 Performance Overview

Table 1.2 shows performance overview.

**Table 1.2 Performance overview** 

As of June 2004

Type No.	ROM	RAM	Package	Remarks
M301N2M4T-XXXFP(D)	32Kbytes	1Kbytes		Mask ROM
M301N2M8T-XXXFP(D)			40D6O A	IVIASK ROIVI
M301N2F8TFP(D)	64Kbytes	3Kbytes	48P6Q-A	Floor mamory
M301N2F8FP(D)				Flash memory

(D): Under development

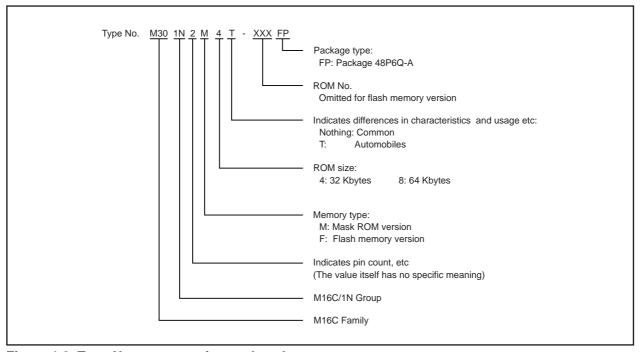


Figure 1.2 Type No., memory size, and package

M16C/1N Group 1. Overview

# 1.6 Pin Description

Table 1.3 shows the pin description.

Table 1.3 Pin Description

Pin name	Signal name	I/O type	Function
Vcc, Vss	Power supply input	Input	Supply 4.2 to 5.5 V to the Vcc pin. Supply 0 V to the Vss pin.
IVcc	IVcc	Input	Connect a capacitor (0.1 µF) between this pin and Vss.
CNVss	CNVss	Input	Connect it to the Vss pin via resistance (about 5 $k\Omega$ ).
RESET	Reset input	Input	A "L" on this input resets the microcomputer.
XIN	Clock input	Input	These pins are provided for the main clock oscillation circuit. Connect a ceramic resonator or crystal between the XIN and
Xout	Clock output	Output	XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
VREF	Reference voltage input	Input	This pin is a reference voltage input for the A/D converter.
P00 to P07	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor. These pins are shared with analog input pins. P02 and P03 function as CANO I/O pins by using software.
P10 to P17	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. P10 to P13 are shared with analog inputs and key input interrupts. P14 to P16 are shared with serial I/O pins. P17 is shared with timer input. Can be used as an LED drive port.
P20 to P21	I/O port P2	Input/output	This is a 2-bit I/O port equivalent to P0.
P30 to P37	I/O port P3	Input/output	This is a 8-bit I/O port equivalent to P0. P30 to P33 are shared with timer input/output. P34 to P37 are shared with serial I/O. P34 is shared with analog outputs.
P40 to P47	I/O port P4	Input/output	This is a 8-bit I/O port equivalent to P0. P40 to 41 are shared with analog inputs. P42 to P45 are shared with interrupt inputs. P46 to P47 are shared with the I/O pin of the clock oscillation circuit for the clock.
P50 to P52	I/O port P5	Input/output	This is a 3-bit I/O port equivalent to P0. P50 and P51 function as CAN0 I/O pins by using software.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

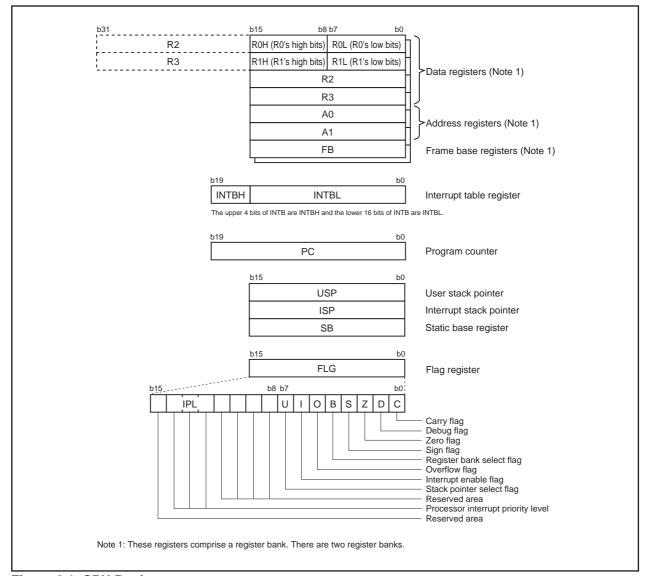


Figure 2.1 CPU Registers

# 2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

# 2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).



# 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

# 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

# 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

# 2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

# 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

# 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

#### 2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

## 2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

#### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

# 2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

#### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is set to "0" when the interrupt request is accepted.

#### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is set to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

#### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

#### 2.8.10 Reserved Area

When white to this bit, write "0". When read, its content is indeterminate.



# 4. Special Function Registers (SFR)

Address	Register	Symbol	After reset
000016	5		
000116			
000216			
000316			V0.00.00.00
000416	Processor mode register 0	PM0	XXXX0X00 <sub>2</sub>
000516	Processor mode register 1	PM1 CM0	00XXX0X02
0006 <sub>16</sub>	System clock control register 0 System clock control register 1	CM1	48 <sub>16</sub> 20 <sub>16</sub>
000716	System clock control register 1	CIVIT	2016
000916	Address match interrupt enable register	AIER	XXXXXX002
000A <sub>16</sub>	Protect register	PRCR	XXXXX0002
000B <sub>16</sub>	Ü		
000C <sub>16</sub>	Oscillation stop detection register	CM2	0416
000D <sub>16</sub>			
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog timer control register	WDC	000XXXXX <sub>2</sub>
001016	Address metals into mount as distant	DMADO	00000002
0011 <sub>16</sub> 0012 <sub>16</sub>	Address match interrupt register 0	RMAD0	00000002 XXXX00002
001216			^^^\UUU02
001316			00000002
001516	Address match interrupt register 1	RMAD1	00000002
001616	, -3		XXXX00002
0017 <sub>16</sub>			
001816			
001916			
001A <sub>16</sub> 001B <sub>16</sub>			
001B <sub>16</sub>			
001D <sub>16</sub>			
001E <sub>16</sub>	INTO input filter select register	INT0F	XXXXX0002
001F <sub>16</sub>			
002016			
002116			
002216			
002316			
0024 <sub>16</sub> 0025 <sub>16</sub>			
002516			
002716			
002816			
002916			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>			
002D <sub>16</sub> 002E <sub>16</sub>			
002E16			
0021 16			
003116			
003216			
003316			
003416			
003516			
0036 <sub>16</sub>			
003716		<del>     </del>	
003016			
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>			
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X: Undefined



000Fits         Timer Y, Zmode register         TYZMR         0000000000           00081te         Prescaler Y         PREY         FF-te           00082e         Timer F personaler Y         PREY         FF-te           00083e         Timer F primary         TYPR         FF-te           00085e         Prescaler Z         PF-te         PREZ         FF-te           00066e         Timer S primary         TZSC         FF-te           00087e         Timer Z primary         TZSC         FF-te           00088e         Prescaler 1         PRE1         XX-u           00088e         Prescaler 1         PRE1         XX-u           00088e         Timer 1 miner 7 mode register         TYZOC         XXXXXXXXXXXX           00088e         Timer 6 mode register         TXMR         000000000           00089e         Timer 7 mode register         TXMR         000000000           00080e         Timer 8 mode register         TXMR         0000000000           00081e         Timer 9 mode register         TXX         FF-te           00096e         Timer C toolker feest flag         CPSRF         0XXXXXXXXX           00097e         Timer C counter         TC         XX-te	Address	Register	Symbol	After reset
D081s				
OBS28				
00834s         Timer Y primary         TYPR         FFis           0084ss         Imer Y Z waveform output control register         PREZ         FFis           0086is         Prescaler Z         PREZ         FFis           0087is         Timer Z primary         TZPR         FFis           0088is         Prescaler 1         PRE1         XXis           0088is         Timer P Prescaler 1         PRE1         XXis           0088is         Timer Y Coutput control register         TYZOG         XXXXXX0002           0088is         Timer X mode register         TYMR         00000000           0088is         Timer X mode register         TYMR         00000000           0088is         Timer X mode register         TYMR         00000000           0088is         Timer X mode register         TXX         FFis           0088is         Timer X mode register         TXMR         00000000           0088is         Timer C counter         TC         XXis           0088is         Timer C counter         TC         XXis           0099is         Timer C counter         TC         XXis           0092is         Timer C counter         TC         XXis           0093is				
00846s         Timer Y, Z. waveform output control register         PUM         00%           0085is         Prescaler Z         FFis           0086is         Timer Z primary         TZSC         FFis           0088is         Prescaler 1         PRE1         XXis           0088is         Prescaler 1         PRE1         XXis           0088is         Timer 2 primary         TZPR         FFis           0088is         Timer 2         PRE2         FFis           0088is         Timer 2 primary         TZPR         FFis           0088is         Timer 2         TMR         No           0088is         Timer 3         August 2         TXMR         0000000002           0088is         Timer 4 mode register         TXMR         0000000002         XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
0086is         Prescaler Z         PREZ         FF:6           0087is         Timer Z primary         TZPR         FF:6           0087is         Timer Z primary         TZPR         FF:6           0088is         Timer Z primary         TZPR         FF:6           0084is         Timer X         TYZOC         XXXXX000-           008Bis         Timer X mode register         TXMR         000000000           008Dis         Timer X mode register         TXMR         00000000           008Dis         Timer X mode register         TXXX         FF:6           008Fis         Timer X         TX         FF:6           008Fis         Clock prescaler reset flag         CPSRF         0XXXXXXX           0091s         Timer C counter         TC         XX:6           0092s         Clock prescaler reset flag         CPSRF         0XXXXXXXX           0092s         Timer C counter         TC         XX:6           0092s         Timer C counter         TC         XX:6           0093s         Clock prescaler reset flag         CPSRF         0XXXXXXXX           0094s         External input enable register         INTEN         00:6           0095s         Colonal				
OBB6s				
OBSPIRED				
O088				
0089s         Timer 1         T1         XXs           008Ass         Timer X mode register         TYXOC         XXXXXX0002           008Dus         Timer X mode register         TXMR         00000000           008Dus         Timer X         TX         FF1s           008Est         Timer X         TX         FF1s           008Est         Timer Counts source set register         TCSS         00%           0090us         Timer Counter         TC         XXxis           0091us         Timer C counter         TC         XXxis           0092us         0093us         Timer C counter         TC         XXxis           0093us         0094us         Timer C counter         TC         XXxis           0095us         0095us         Timer C counter         INTEN         00us           0095us         External input enable register         INTEN				
OBBA   Timer X   Doubut control register				
O008Bis   Timer X mode register		-		
ORDERS   Prescaler X   PREX   FFire				
OBBE   Timer C   Timer C   TCSS   O0-16				
O08E+16				
OSS-16		-		
O090-12				
O0921-16				
0092-te   0093-te   0093-te   0095-te   0095-te   0095-te   0095-te   0095-te   0095-te   0095-te   0097-te   0099-te   0099		Timer C counter	TC —	
0093-16			1	,
009416			1	
009516				
009616				
009916		External input enable register	INTEN	0016
009816		The state of the s	1	
00994s		Key input enable register	KIEN	0016
009A₁6		They impart smaller regions:		
0.09B16		Timer C control register 0	TCC0	0XX000002
O09C+6   O09D+6   O				
O09Dr6	009C <sub>16</sub>	•		
009E16         009F16         UART0 transmit/receive mode register         UOMR         0016           00A016         UART0 bit rate generator         UOBRG         XX16           00A216         UART0 transmit buffer register         UOTB         XX16           00A316         UART0 transmit/receive control register 0         UOC0         0816           00A416         UART0 transmit/receive control register 1         UOC1         XXX000102           00A616         UART0 transmit/receive control register 1         UOC1         XXX000102           00A616         UART0 receive buffer register         UORB         XX16           00A916         UART1 bit rate generator         U1BRG         XX16           00A916         UART1 bit rate generator         U1BRG         XX16           00A016         UART1 transmit/receive control register         U1TB         XX16           00A016         UART1 transmit/receive control register 0         U1C0         0816           00A016         UART1 transmit/receive control register 1         U1C1         XXX00102           00A16         UART1 transmit/receive control register 1         U1C1         XXX16           00B16         UART1 transmit/receive control register 2         UCON         X00000002           00B16		Time measurement register	TM —	
O0A016				
O0A016	009F <sub>16</sub>		1	
00A1:6 00A2:6 00A3:6 00A3:6 00A4:6 00A4:6 00A4:6 00A5:0 00A6:0 00A6:0 00A7:6		UART0 transmit/receive mode register	UOMR	0016
00A2:6 00A3:6 00A3:6 00A4:6 00A5:6 00A5:6 00A5:6 00A6:6 00A6:6 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6 00A6:0 00A7:6				
OA316	00A2 <sub>16</sub>	·		XX <sub>16</sub>
00A416         UART0 transmit/receive control register 0         U0C0         0816           00A516         UART0 transmit/receive control register 1         U0C1         XXXX00102           00A616         UART0 receive buffer register         U0RB         XX16           00A716         UART1 transmit/receive mode register         U1MR         0016           00A916         UART1 transmit/receive mode register         U1MR         0016           00A916         UART1 transmit/receive mode register         U1BRG         XX16           00A916         UART1 transmit buffer register         U1BRG         XX16           00AB16         UART1 transmit/receive control register 0         U1C0         0816           00AD16         UART1 transmit/receive control register 1         U1C1         XXXX00102           00AE16         UART1 receive buffer register         U1RB         XX16           00B016         UART1 transmit/receive control register 2         UCON         X00000002           00B16         UART1 transmit/receive control register 2         UCON         X00000002           00B316         00B316         00B316         00B316           00B316         00B316         00B316         00B316           00B316         00B316         00B316 <t< td=""><td></td><td>UART0 transmit buffer register</td><td>U0TB</td><td></td></t<>		UART0 transmit buffer register	U0TB	
00A516 00A616 00A716 00A716 00A916 00A916 00A916 00AB16 00AB16 00AB16 00B216 00BS16		UART0 transmit/receive control register 0	U0C0	
OAB16	00A5 <sub>16</sub>			
UNA/16		Ü		
O0A816	00A7 <sub>16</sub>	UAR10 receive buffer register	U0RB	XX <sub>16</sub>
O0A916	00A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	
OOAA16	00A9 <sub>16</sub>			
OAB16				
00AC16         UART1 transmit/receive control register 0         U1C0         0816           00AD16         UART1 transmit/receive control register 1         U1C1         XXXX00102           00AE16         UART1 receive buffer register         U1RB         XX16           00B016         UART transmit/receive control register 2         UCON         X00000002           00B116         00B216         00B316         00B316           00B316         00B416         00B516         00B516           00B316         00B316         00B316         00B316           00B316         00B316         00B316         00B316           00B316         00B316         00B316         00B316         00B316           00B316         00B		UAKT1 transmit buffer register	U1 IB	
00AD16         UART1 transmit/receive control register 1         U1C1         XXXX00102           00AE16         UART1 receive buffer register         U1RB         XX16           00B016         UART transmit/receive control register 2         UCON         X00000002           00B116         00B216         00B316           00B416         00B416         00B416           00B716         00B716         00B316           00B316         00B316		UART1 transmit/receive control register 0	U1C0	
00AE16 00AF16 00B016         UART1 receive buffer register         U1RB         XX16 XX16 XX16           00B016 00B116 00B216 00B416 00B516 00B616 00B816 00B916 00BB16 00BB16 00BB16 00BB16 00BB16 00BB16         U1RB         XX16 XX16 XX16 XX16 XX10 XX10 XX10 XX10	00AD <sub>16</sub>			
00AF16         UART freceive butter register         UCON         XX16           00B016         UART transmit/receive control register 2         UCON         X00000002           00B16         00B316	00AE <sub>16</sub>			
00B016         UART transmit/receive control register 2         UCON         X00000002           00B16         00B216         00B316         00B416         00B416         00B516         00		UARTITIECEIVE DUITET FEGISTEF	UIKB	XX <sub>16</sub>
00B16       00B26       00B36       00B46       00B56       00B76       00B86       00B96       00B46       00B86       00B46       00B66       00B76       00B66       00B66       00B76       00B66       00B67       00B7       00B7       00B7       00B7       00B7       00B7       00B7		UART transmit/receive control register 2	UCON	X0000002
00B316       00B416       00B516       00B616       00B716       00B816       00B916       00BA16       00BB16       00BC16       00BD16       00BD16       00BE16				
00B416       00B516       00B616       00B716       00B816       00B916       00BA16       00BB16       00BC16       00BD16       00BD16       00BE16	00B2 <sub>16</sub>			
00B516         00B616         00B716         00B816         00B916         00BA16         00BB16         00BC16         00BD16         00BD16         00BE16				
00B616       00B716       00B816       00B916       00BA16       00BB16       00BC16       00BD16       00BE16				
00B716       00B816       00B916       00BA16       00BB16       00BC16       00BD16       00BE16				
00B816       00B916       00BA16       00BB16       00BC16       00BD16       00BE16				
00B916 00BA16 00BB16 00BC16 00BD16 00BE16				
00BA16 00BB16 00BC16 00BD16 00BE16				
00BB16 00BC16 00BD16 00BE16				
00BC <sub>16</sub> 00BD <sub>16</sub> 00BE <sub>16</sub>				
00BD <sub>16</sub> 00BE <sub>16</sub>				
00BE16				
00BF <sub>16</sub>				
	00BF <sub>16</sub>			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X: Undefined



D2CO   18	Address	Register	Symbol	After reset
CANO slot 6: Identifier / DLC	02C0 <sub>16</sub>	1.2-3.000		XX <sub>16</sub>
OZC34s   OZC5ss   O				
DC2-16		CANO slot 6: Identifier / DLC		
XX ts   XX t		S. 110 Giol G. Idolitilioi / DEO		
2020   2020				
XX ts				
XX   50				
AND slot 6: Data Field				
CANU Stot 6: Data Field				
DOCK		CAN0 slot 6: Data Field		
DZCC   To   DZCD   To   DZCD				
OZCE				
CANO slot 6: Time Stamp				
CAND slot 6: Time Stamp		CANIC state C. Time Of some		
CZD1   CZD2   CZD3   CZD4   CZD5		CANU slot 6: Time Stamp		
CZD21-6   CZD3-6   CZD3-6   CZD3-6   CZD3-6   CZD5-6				XX <sub>16</sub>
CANO slot 7: Identifier / DLC   XX is   XX i	02D1 <sub>16</sub>			
OZD346   OZD546   O		CAN0 slot 7: Identifier / DLC		
OZD5-16   OZD6-16   OZE6-16   OZE6		S. 1.15 GIGET . IGGINATION / DEG		
O2D616   O2D716   O				
Q2D7-6   Q2D9-6   Q				
OZDB-16   OZDB-16   OZDB-16   OZDB-16   OZDB-16   OZDB-16   OZDD-16   OZDD-16   OZDD-16   OZDD-16   OZDD-16   OZDD-16   OZDD-16   OZDB-16   OZBB-16   OZBB				
02D9-16 02DA16 02DA16 02DD16 02DD16 02DD16 02DD16 02DD16 02DD16 02DD16 02ED1				
OZDA16   OZDB16   OZBB16   O				
C2DB-16   CANO slot 7: Time Stamp   XX-16   XX-16   XX-16   CANO slot 7: Time Stamp   XX-16		CAN0 slot 7: Data Field		
O2DC16				
O2DD16   O2ED16				
O2DE16   O2DF16   O				
O2DF16	02DE <sub>16</sub>	CANIC alot 7: Time Charac		
O2E16   O2E216   O2E316   O2		CANU Slot 7: Time Stamp		
O2E216   O2E316   O2E416   O2E416   O2E516   O				XX <sub>16</sub>
02E316 02E416 02E516 02E616 02E616 02E816 02E816 02E816 02EA16 02EB16 02EC16 02ED16 02EC16 02ED16 02EC16 02ED16 02EF16 02EF16 02EF16 02F516				
02E316 02E416 02E616 02E616 02E816		CAN0 slot 8: Identifier / DLC		
02E516         02E616           02E716         02E716           02E816         02E816           02E916         02EA16           02EB16         02EB16           02ED16         02ED16           02ED16         02ED16           02EF16         02ED16           02EF16         02ED16           02EF16         02ED16           02EF16         02ED16           02F016         02ED16           02F016         02ED16           02F016         02ED16           02F016         02ED16           02F016         02ED16           02F016         02ED16           02ED16		97 H 10 3:01 01 103:11		
02E616         02E716           02E816         02E916           02E916         02E916           02E916         02E916           02E916         02E916           02E016         02E916           02E916				
O2E716   O2E816   O2E916   O2E916   O2E916   O2ED16   O				
02E816         02E916           02EA16         02EA16           02EB16         XX16           02ED16         XX16           02ED16         XX16           02ED16         XX16           02ED16         XX16           02EF16         XX16           02F16         XX16           02F16         XX16           02F316				
02E916         02EA16           02EB16         02ED16           02ED16         XX16           02ED16         XX16           02ED16         XX16           02EB16         XX16           02ED16         XX16           02ED16         XX16           02ED16         XX16           02ED16         XX16           02FD16         XX16           02FD16         XX16           02F316         XX16           02F3				
02EA16     02EB16       02ED16     XX16       02ED16     XX16       02ED16     XX16       02EE16     XX16       02EF16     XX16       02F016     XX16       02F116     XX16       02F316     XX16       02F316     XX16       02F316     XX16       02F516     XX16       02F616     XX16       02F716     XX16       02F816     XX16       02F916     XX16       02F816				
02EB16       02EC16         02ED16       XX16         02EE16       XX16         02EF16       XX16         02F016       XX16         02F016       XX16         02F116       XX16         02F216       XX16         02F316       XX16		CAN0 slot 8: Data Field		
02EC16         02ED16           02ED16         XX16           02E16         XX16           02E716         XX16           02F016         XX16           02F116         XX16           02F216         XX16           02F316         XX16           02F317<				
02ED16       02EE16         02EF16       02F16         02F016       02F016         02F116       02F116         02F216       02F316         02F316       02F316         02F416       02F316         02F516       02F516         02F616       02F616         02F716       02F816         02F916       02F916         02F316       02F316	02EC <sub>16</sub>			XX <sub>16</sub>
02EF16         CANO slot 8: Time Stamp           02F016         02F116           02F216         XX16           02F216         XX16           02F316         XX16           02F416         XX16           02F516         XX16           02F616         XX16           02F716         XX16           02F816         XX16           02F916         XX16           02F816         XX16				XX <sub>16</sub>
O2F16   O2F016   O2		CANO slot 8: Time Stamp		
02F116     02F216       02F316     02F316       02F416     02F416       02F516     02F516       02F716     02F716       02F316     02F316		Orativo Giot of Tillio Otaliip		XX <sub>16</sub>
02F216     02F316       02F316     02F416       02F516     02F516       02F516     02F616       02F716     02F816       02F316     02F816       02F316     02F316				
O2F316				
02F416     XX16       02F516     XX16       02F616     XX16       02F716     XX16       02F816     XX16       02F916     XX16       02FA16     XX16       02FB16     XX16       02FC16     XX16       02FD16     XX16       02FE16     XX16       02FE16     XX16       02FE16     XX16		CAN0 slot 9: Identifier / DLC		
02F516     XX16       02F616     XX16       02F716     XX16       02F816     XX16       02F916     XX16       02FA16     XX16       02FB16     XX16       02FC16     XX16       02FD16     XX16       02FE16     XX16       02FE16     XX16				
02F616     02F716       02F816     02F816       02F916     02F816       02F816     02F816       02F816     02F816       02F016     02F816       02F016     02F816       02F816     02F816       02F816     02F816       02F816     02F816       02F816     02F816				
02F716     02F816       02F916     02F916       02FA16     02FB16       02F016     02FC16       02FD16     02FD16       02FE16     02FC16       02FD16     02FC16       02FD16     02FC16			1	
02F816     02F916       02FA16     02FA16       02FB16     02FC16       02FD16     02FD16       02FD16     XX16       02FE16     XX16       02FL16     XX16				
02F916     02FA16       02FB16     02FC16       02FD16     02FD16       02FE16     XX16       02FE16     XX16       XX16     XX16				
02FA16     02FB16       02FC16     02FD16       02FD16     02FD16		CAND LAD BA FILL		
02FB16 02FC16 02FD16 02FB16 02FB16 02FB16 02FB16 02FB16 02FB16 02FB16 02FB16 02FB16		CANU slot 9: Data Field		
02FC16	02FB <sub>16</sub>			
02FE16 XX16				
02FF <sub>16</sub> XX <sub>16</sub>		CANO slot 9: Time Stamp		
	02FF <sub>16</sub>	S. a. to diet of Time Stamp		XX <sub>16</sub>

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined



Address	Register	Symbol	After reset
034016	. togisto.		XX <sub>16</sub>
034116			XX <sub>16</sub>
034216	CAN0 slot 14: Identifier / DLC		XX <sub>16</sub>
034316	CANO SIOU 14. Identifier / DLC		XX <sub>16</sub>
034416			XX <sub>16</sub>
034516			XX <sub>16</sub>
034616			XX <sub>16</sub>
034716			XX <sub>16</sub>
034816			XX <sub>16</sub>
034916	CAN0 slot 14: Data Field		XX <sub>16</sub>
034A <sub>16</sub>	CANO SIOU 14. Data Fleid		XX <sub>16</sub>
034B <sub>16</sub>			XX <sub>16</sub>
034C <sub>16</sub>			XX <sub>16</sub>
034D <sub>16</sub>			XX <sub>16</sub>
034E <sub>16</sub>	CAN0 slot 14: Time Stamp		XX <sub>16</sub>
034F <sub>16</sub>	CANO SIOU 14. Time Gramp		XX <sub>16</sub>
035016			XX <sub>16</sub>
035116			XX <sub>16</sub>
035216	CAN0 slot 15: Identifier / DLC		XX <sub>16</sub>
035316	ON 140 SIDE TO. IGGIRING! / DEG		XX <sub>16</sub>
035416			XX <sub>16</sub>
035516			XX <sub>16</sub>
035616			XX <sub>16</sub>
035716			XX <sub>16</sub>
035816			XX <sub>16</sub>
035916	CAN0 slot 15: Data Field		XX <sub>16</sub>
035A <sub>16</sub>	S. 1.10 GIOL TO. Data I IGIU		XX <sub>16</sub>
035B <sub>16</sub>			XX <sub>16</sub>
035C <sub>16</sub>			XX <sub>16</sub>
035D <sub>16</sub>			XX <sub>16</sub>
035E <sub>16</sub>	CAN0 slot 15: Time Stamp		XX <sub>16</sub>
035F <sub>16</sub>	Critto diet 16. Timo Gtamp		XX <sub>16</sub>
036016			XX <sub>16</sub>
036116			XX <sub>16</sub>
036216	CAN0 Global mask	COGMR	XX <sub>16</sub>
036316			XX <sub>16</sub>
036416			XX <sub>16</sub>
036516			XX16
036616			XX <sub>16</sub>
036716			XX <sub>16</sub>
036816	CAN0 local mask A		XX16
036916		C0LMAR	XX <sub>16</sub>
036A <sub>16</sub>			XX <sub>16</sub>
036B <sub>16</sub>			XX16
036C <sub>16</sub>			XX <sub>16</sub>
036D <sub>16</sub>			XX16
036E <sub>16</sub>	CAN0 local mask B	C0LMBR -	XX16
036F <sub>16</sub>			XX <sub>16</sub>
037016			XX16
037116			XX16
03B4 <sub>16</sub>			
03B4 <sub>16</sub> 03B5 <sub>16</sub>			
03B316 03B616			
03B016 03B716			
03B716 03B816			
03B816 03B916			
U3B916			
03FA <sub>16</sub>			
03FA <sub>16</sub>			
03FB16 03FC16			
03FC <sub>16</sub> 03FD <sub>16</sub>			
03FD <sub>16</sub> 03FE <sub>16</sub>			
03FE16 03FF16			
U3FF16			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X: Undefined



# 5. Electrical Characteristics

Table 5.1 Absolute maximum ratings

Symbol		Parameter	Condition	Rated value	Unit
Vcc	Supply voltage			- 0.3 to 6.5	V
Vı	Input voltage	RESET, VREF, XIN P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52, CNVss (Note 1)		- 0.3 to Vcc + 0.3	V
Vo	Output voltage	P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52, XOUT		- 0.3 to Vcc + 0.3	V
		IVcc		- 0.3 to 2.8V	V
Pd	Power dissipation	Power dissipation		300	mW
Topr	Operating ambie	Operating ambient temperature		- 40 to 85 (Note 2)	°C
Tstg	Storage tempera	ature		- 65 to 150	°C

Note 1: CNVss pin of flash memory version: -0.3 to 6.5 V

Note 2: When flash memory version is program/erase mode: 0 to 60 °C



Table 5.2 Recommended operating conditions
(Unless otherwise noted: Vcc = 4.2V to 5.5V, Topr = -40 to 85°C)

0		Dovernator					1.1
Symbol		Parameter	Min	Тур.	Max.	Unit	
Vcc	Supply voltage			4.2	5.0	5.5	V
Vss	Supply voltage				0		V
VIH	HIGH input voltage	P00 to P07, P10 to P17, P20, P21, P30 t P50 to P52, XIN, RESET, CNVss	o P37, P40 to P47,	0.8Vcc		Vcc	V
VIL	LOW input voltage	P00 to P07, P10 to P17, P20, P21, P30 t P50 to P52, XIN, RESET, CNVss	o P37, P40 to P47,	0		0.2Vcc	V
IOH (peak)	HIGH peak output current	P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52				- 10.0	mA
IOH (avg)	HIGH average output current	P00 to P07, P10 to P17, P20, P21, P30 t P50 to P52	o P37, P40 to P47,			- 5.0	mA
IOL (peak)	LOW peak	P00 to P07, P20, P21, P30 to P37, P40 t	to P47, P50 to P52			10.0	mA
	output current	P10 to P17	HIGH POWER			20.0	mA
			LOW POWER			10.0	IIIA
IOL (avg)	LOW average	P00 to P07, P20, P21, P30 to P37, P40 to	to P47, P50 to P52			5.0	mA
	output current	P10 to P17	HIGH POWER			10.0	mA
			LOW POWER			5.0	IIIA
f (XIN)	Main clock input oscillation frequency (Note 3) Vcc=4.2V to 5.5V					16	MHz
f (Xcin)	Subclock oscillat	ion frequency	•		32.768	50	kHz

Note 1: The average output current is an average value measured over 100ms.

Note 2: Keep output current as follows:

The sum of port P00 to P03, P13 to P17, P21, P34 to P37, P46, P47, P50 to P52 IoL (peak) is under 60 mA. The sum of port P00 to P03, P13 to P17, P21, P34 to P37, P46, P47, P50 to P52 IoH (peak) is under 60 mA. The sum of port P04 to P07, P10 to P12, P20, P30 to P33, P40 to P45 IoL (peak) is under 60 mA. The sum of port P04 to P07, P10 to P12, P20, P30 to P33, P40 to P45 IoH (peak) is under 60 mA.

Note 3: Relationship between main clock oscillation frequency and supply voltage is shown as below.

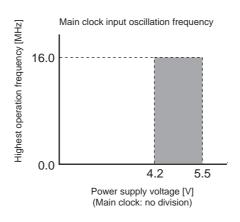


Table 5.3 Electrical characteristics (1) (Unless otherwise noted: Vcc = 5V, Vss = 0V at Topr = -40 to 85°C, f(XIN) = 16MHz)

Symbol		Doromotor		Magazing condition	5	Standard		
Symbol		Parameter		Measuring condition	Min.	Тур.	Max.	Unit
Vон	HIGH output	P00 to P07,P10 t	o P17,P20 to P21,	Iон = - 5 mA	3.0			.,
	voltage	P30 to P37,P40 to P47,P50 to P52		Ioн = - 200 μA	4.7			V
Vон	HIGH output	Хоит	HIGH POWER	Iон = - 1 mA	3.0			V
	voltage		LOW POWER	Iон = - 0.5 mA	3.0			V
Vон	HIGH output	Хсоит	HIGH POWER	No load		2.5		V
	voltage		LOW POWER	No load		1.6		V
Vol	LOW output	P00 to P07,P20,F	P21,P30 to P37,	IoL = 5 mA			2.0	V
	voltage	P40 to P47,P50 t	o P52	Ιοι = 200 μΑ			0.45	V
VoL	LOW output	P10 to P17	HIGH POWER	IoL = 10 mA			2.0	V
	voltage		LOW POWER	IoL = 5 mA			2.0	\ \
Vol	LOW output	Хоит	HIGH POWER	IOH = 1 mA			2.0	.,
	voltage		LOW POWER	Iон = 0.5 mA			2.0	V
Vol	LOW output	output Хсоит Э	HIGH POWER	No load		0		V
	voltage		LOW POWER	No load		0		
VT+ -VT-	Hysteresis	SiS CNTR0,TCIN, INT0 to INT3,CLK0,CLK1,P45 RxD0,RxD1,KI0 to KI3,CRX0			0.2		0.8	V
VT+ -VT-	Hysteresis	RESET			0.2		1.8	V
Іін	HIGH input current	P00 to P07,P10 t P30 to P37,P40 t XIN,RESET,CNV	o P47,P50 to P52,	VI = 5V			5.0	μA
lıL	LOW input current	P00 to P07,P10 t P30 to P37,P40 t XIN,RESET,CNV	o P47,P50 to P52,	VI = 0V			-5.0	μA
RPULLUP	Pull-up resistor	P00 to P07,P10 t P30 to P37,P40 t	o P17,P20,P21, o P47,P50 to P52	Vi = 0V	30.0	50.0	167.0	kΩ
Rfxin	Feedback resistor	XIN				1.0		МΩ
Rfxcin	Feedback XCIN resistor					15.0		ΜΩ
VRAM	RAM retention	n voltage		When clock is stopped	2.0			V
Rosc	Oscillation fre	equency of	Mask ROM		000	000	4000	
	On-chip oscill	ator	Flash memory		300	600	1200	kHz

Table 5.6 Flash memory version electrical characteristics (Unless otherwise noted: Vcc = 4.2 to 5.5 V, Topr= 0 to 60°C)

Cumbal	Parameter		Standard			
Symbol			Min.	Typ. (Note 1)	Max.	- Unit
-	Erase/write cycle (No	ote 2)	100 (Note 3)			cycle
-	Word programming time			75	600	μs
-	Block erasing time 2Kbyte block			0.2	9	s
		8Kbyte block		0.4	9	S
		16Kbyte block		0.7	9	S
		32Kbyte block		1.2	9	S
td(SR-ES)	Transition time from erasure operation				20	
	to erase-suspend				20	ms
-	Data retention		10			year

Note1: Vcc=5.0V, Topr=25°C

Note2: Definition of Programming and erasure times

The Programming and erasure times are defined to be per-block erasure times. For example a case where a 2K-byte block is programmed in 1,024 operations by writing one word at a time and erased thereafter. Performing multiple programs to the same address before an erase operation is prohibited.

Note 3: Minimum number of programming/erasure for which operation is guaranteed.

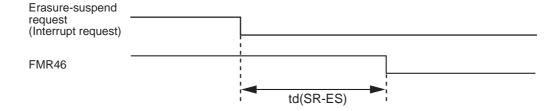


Table 5.7 A/D conversion characteristics
(Unless otherwise noted: VCC = VREF = 5V, Vss = 0V at Topr = 25°C, f(XIN) = 16MHz)

Symbol	Parameter		Magazing condition		Standard			Linit
Cymbol		i didilietei	Measuring condition		Min.	Тур.	Max.	Unit
_	Resolution		VREF =VCC				10	Bits
_	Absolute	Sample & hold function not available	VREF =VCC = 5V	1			±3	LSB
	accuracy	Sample & hold function available(10bit)	VREF =VCC = 5V	ANo to AN11 input			±3	LSB
				ANEX <sub>0</sub> , ANEX <sub>1</sub> input, external op-amp connected mode			±7	LSB
		Sample & hold function available(8bit)	VREF =VCC = 5V	,			±2	LSB
RLADDER	Ladder resistance		VREF=VCC		10		40	kΩ
tconv	Conversion time(10bit)		f(XIN)=10MHz, ØAD=fAD=10MHz		3.3			μs
tconv	Conversion time(8bit)		f(XIN)=10MHz, 9	ØAD=fAD=10MHz	2.8			μs
<b>t</b> SAMP	Sampling time		f(XIN)=10MHz, \$	ØAD=fAD=10MHz	0.3			μs
VREF	Reference voltage		f(XIN)=10MHz, 9	ØAD=fAD=10MHz	2		Vcc	V
VIA	Analog input voltage		f(XIN)=10MHz, 9	ØAD=fAD=10MHz	0		VREF	V

Note 1: Divide the fAD if f(XIN) exceeds 10MHz, and make AD operation clock frequency (ØAD) equal to or lower than 10MHz.

Table 5.8 D/A conversion characteristics
(Unless otherwise noted: VCC = VREF = 5V, Vss = 0V at Topr = 25°C, f(XIN) = 16MHz)

Cumple of	Davamatas	Manageria a condition	Standard			I limit
Symbol	Parameter	Measuring condition	Min.	Тур.	Max.	Unit
_	Resolution				8	Bits
_	Absolute accuracy				1.0	%
<b>t</b> su	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
Ivref	Reference power supply input current	(Note 1)			1.5	mA

Note 1: The A/D converter's ladder resistance is not included.

When D/A register contents are not "0016", the current IVREF always flows even though VREF may have been set to be unconnected by the A/D control register.

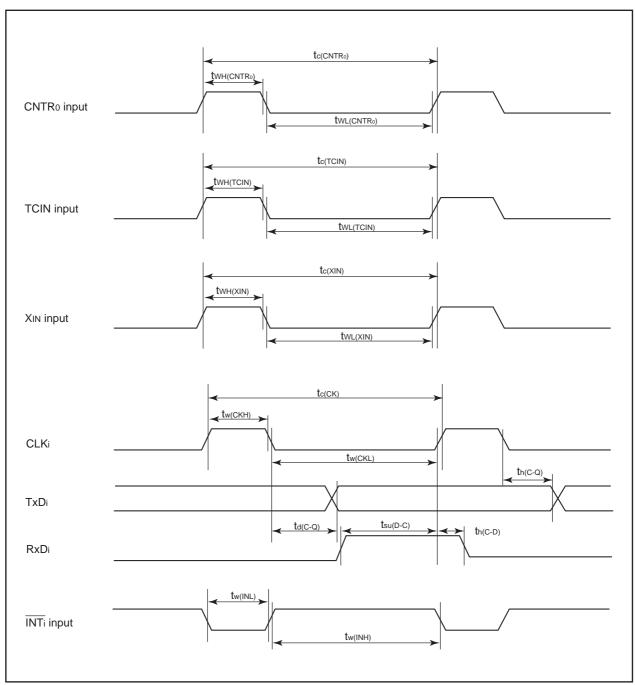


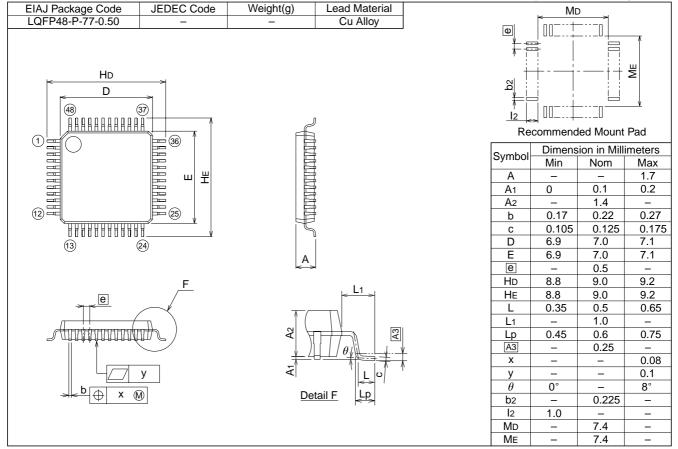
Figure 5.2 Vcc=5V timing diagram

M16C/1N Group Package Dimension

# **Package Dimension**

# 48P6Q-A Recommended

# Plastic 48pin 7×7mm body LQFP



REVISION HISTORY	M16C/1N Group Data Sheet
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Rev.	Date	Description			
L.Sv.		Page	Summary		
1.00	Oct 20, 2004				
1.00	Oct 20, 2004		First edition issued (Renesas Technology version)		

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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