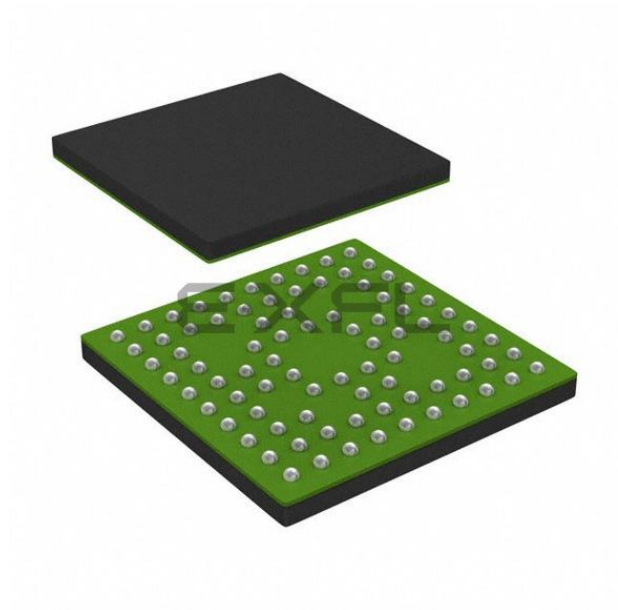

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	23
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-WFBGA
Supplier Device Package	84-WFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3222-sx-tr

TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
2-7	nRTS1/ SYSOPT0	Request to Send 1/ SYSOPT (Configuration Port Base Address Control)	nRTS1/ SYSOPT0		GATE/ Hi-Z	OP14 / I
	nCTS1	Clear to Send 1	nCTS1		GATE	I
	nDTR1 / SYSOPT1	Data Terminal Ready 1	nDTR1 / SYSOPT1		GATE/ Hi-Z	O6 / I
2-9	nRI1	Ring Indicator 1		nRI1	GATE	IS
	nDCD1	Data Carrier Detect 1	nDCD1		GATE	I
SERIAL PORT 2 INTERFACE						
2-9	GP50 / nRI2	Ring Indicator 2	GP50	nRI2	NO GATE/ HI-Z	(I/OD8/OD8) / IS
2-9	GP51 / nDCD2	Data Carrier Detect 2	GP51 / nDCD2		NO GATE/ HI-Z	(I/OD8/OD8) / I
2-9	GP52 / RXD2 (IRRX2)	Receive Data 2 (IRRX2)	GP52 / RXD2 (IRRX2)		NO GATE/ HI-Z	(I/OD8OD8) / IS
2-11, 2-9	GP53 / TXD2 (IRTX2)	Transmit Data 2 (IRTX2)	GP53 / TXD2 (IRTX2)		NO GATE/ HI-Z	(I/O12/OD12) / (O12/OD12) / (O12/OD12)
2-9	GP54 / nDSR2	Data Set Ready 2	GP54 / nDSR2		NO GATE/ HI-Z	(I/OD8/OD8) / I
2-9 2-15	GP55 / nRTS2 / RESGEN	Request to Send 2 / Reset Generator Pulse Width Strap Option	GP55 / nRTS2 / RESGEN		NO GATE/ HI-Z	(I/O8/OD8) / I / IOP8
2-9	GP56 / nCTS2	Clear to Send 2	GP56 / nCTS2		NO GATE/ HI-Z	(I/OD8OD8) / I
2-9	GP57 / nDTR2	Data Terminal Ready 2	GP57 / nDTR2		NO GATE/ HI-Z	(I/OD8OD8) / O6
SERIAL PORT 3 INTERFACE						
2-9	GP13 / nRI3	GPIO / Ring Indicator 3		GP13 / nRI3	NO GATE	(I/O8/OD8) / I
2-9	GP12 / nDCD3	GPIO / Data Carrier Detect 3	nDCD3	GP12	NO GATE	(I/O8/OD8) / I
2-9	GP10 / RXD3	GPIO / Receive Data 3	GP10 / RXD3		/ HI-Z	(IS/O8/OD8) / IS
2-11, 2-9	GP11 / TXD3	GPIO / Transmit Data 3	TXD3	GP11	/ HI-Z	(I/O8/OD8) / O8
2-9	GP14 / nDSR3	GPIO / Data Set Ready 3	nDSR3	GP14	NO GATE	(I/O8/OD8) / I
2-9	GP17 / nRTS3/	GPIO / Request to Send 3	GP17 / nRTS3/		/ HI-Z	(I/O8/OD8) / I
2-9	GP16 / nCTS3	GPIO / Clear to Send 3	GP16 / nCTS3		/ HI-Z	(I/O8/OD8) / I
2-9	GP15 / nDTR3	GPIO / Data Terminal Ready 3	GP15 / nDTR3		/ HI-Z	(I/O12/OD12) / O12
SERIAL PORT 4 INTERFACE						
2-9	GP31 / nRI4	GPO (OD Only in Output Mode) / Ring Indicator 4		GP31 / nRI4	NO GATE	(I/OD8) / I

TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
2-9	GP63* / nDCD4	GPIO with I_VID buffer Input / Data Carrier Detect 4	nDCD4	GP63*	NO GATE	(I/O8/OD8) / I
2-9	GP64* / RXD4	GPIO with I_VID buffer Input / Receive Data 4	RXD4	GP64*	NO GATE	(IS/O8/OD8) / IS
2-11, 2-9	GP65* / TXD4	GPIO with I_VID buffer Input / Transmit Data 4	TXD4	GP65*	/ HI-Z	(I/O8/OD8) / O8
2-9	GP66* / nDSR4	GPIO with I_VID buffer Input / Data Set Ready 4	nDSR4	GP66*	NO GATE	(I/O8/OD8) / I
2-9	GP67* / nRTS4	GPIO with I_VID buffer Input / Request to Send 4	nRTS4	GP67*	/ HI-Z	(I/O8/OD8) / I
2-9	GP62* / nCTS4	GPIO with I_VID buffer Input / Clear to Send 4	nCTS4	GP62*	NO GATE	(I/O8/OD8) / I
2-9	GP34 / nDTR4	GPIO (OD Only in Output Mode)/ Data Terminal Ready 4	nDTR4	GP34	/ HI-Z	(I/OD12) / O12
SERIAL PORT 5 INTERFACE						
	nSCOUT5	Serial Port 5 out control	nSCOUT5		/ HI-Z	(O8/OD8)
2-9	nSCIN5	Serial Port 5 input Control		nSCIN5	NO GATE	I
	RXD5	Receive 5	RXD5		GATE	IS
	TXD5	Serial Port 5 Transmit	TXD5		NO GATE / HI-Z	(O12.OD12)
SERIAL PORT 6 INTERFACE						
2-12	GP47 / nSCOUT6	GPIO with Schmitt trigger input Serial Port 6 output control	nSCOUT6	GP47 /	HI-Z	(IS/O4/OD4) / (O4/OD4)
2-12	GP46 / nSCIN6	GPIO with Schmitt trigger input Serial Port 6 input Control		GP46 / nSCIN6	NO GATE	(IS/O8/OD8) / (O8/OD8)
2-12	GP45 / RXD6	GPIO with Schmitt trigger input Receive serial port 6	RXD6	GATE	PG	(IS/O8/OD8) / (O8/OD8)
2-12	GP44 / TXD6	GPIO with Schmitt trigger input Serial Port 6 Transmit	TXD6	GP44	NO GATE/ Hi-Z	(IS/O4/OD4) / (O4/OD4)
PARALLEL PORT INTERFACE						
2-12	nINIT	Initiate Output	nINIT		GATE / HI-Z	(OD14/OP14)
2-12	nSLCTIN	Printer Select Input (Output to printer)	nSLCTIN		GATE / HI-Z	(OD14/OP14)
2-12	PD0	Port Data 0	PD0		GATE / HI-Z	IOP14
2-12	PD1	Port Data 1	PD1		GATE / HI-Z	IOP14
2-12	PD2	Port Data 2	PD2 /		GATE / HI-Z	IOP14

Note:	All Vbat powered pins and registers are powered by VTR when VTR power is on and are battery backed-up when VTR is removed.

4.5 32.768 KHz Trickle Clock Input

The SCH322x utilizes a 32.768 KHz trickle input to supply a clock signal for the WDT, LED blink, Power Recovery Logic, and wake on specific key function.

Indication of 32KHZ Clock

There is a bit to indicate whether or not the 32KHz clock input is connected to the SCH322x. This bit is located at bit 0 of the CLOCKI32 register at 0xF0 in Logical Device A. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32KHz clock is connected to the CLKI32 pin (default)

1=32KHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32KHz (nominal) clock for the LED blink logic and the “wake on specific key” logic. When the external 32KHz clock is connected, that will be the source for the fan, LED and “wake on specific key” logic. When the external 32KHz clock is not connected, an internal 32KHz clock source will be derived from the 14MHz clock for the LED and “wake on specific key” logic.

The following functions will not work under VTR power (VCC removed) if the external 32KHz clock is not connected. These functions will work under VCC power even if the external 32 KHz clock is not connected.

- Wake on specific key
- LED blink
- Power Recovery Logic
- WDT
- Front Panel Reset with Input Debounce, Power Supply Gate, and CPU Powergood Signal Generation

4.6 Super I/O Functions

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The super I/O pins that are powered by VTR are as follows: GP42/nIO_PME, GP60/LED1, and GP61/LED2. These pins, if configured as push-pull outputs, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

The maximum Vbat current, I_{bat}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

4.7 Power Management Events (PME/SCI)

The SCH322x offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the Section 13.0, "PME Support," on page 94 section.

5.0 LPC INTERFACE

5.1 LPC Interface Signal Definition

The signals implemented for the LPC bus interface are described in the tables below. LPC bus signals use PCI 33MHz electrical signal characteristics.

5.1.1 LPC REQUIRED SIGNALS

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset. Same functionality as RST_DRV but active low 3.3V.
PCI_CLK	Input	PCI Clock.

5.1.2 LPC OPTIONAL SIGNALS

Signal Name	Type	Description	Comment
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.	Implemented
SER_IRQ	I/O	Serial IRQ.	Implemented
CLKRUN#	OD	Clock Run	Not Implemented
nIO_PME	OD	Same as the PME# or Power Mgt Event signal. Allows the SCH3227/SCH3226/SCH3224/SCH3222 to request wakeup in S3 and below.	Implemented
LPCPD#	I	Power down - Indicates that the device should prepare for LPC I/F shutdown	Not Implemented
LSMI#	OD	Only need for SMI# generation on I/O instruction for retry.	Not Implemented

5.2 Supported LPC Cycles

Table 5-1 summarizes the cycle types are supported by the SCH3227/SCH3226/SCH3224/SCH3222. All other cycle types are ignored.

TABLE 5-1: SUPPORTED LPC CYCLES

Cycle Type	Transfer Size	Comment
I/O Write	1 Byte	Supported
I/O Read	1 Byte	Supported
Memory Write	1 Byte	Not Supported
Memory Read	1 Byte	Not Supported
DMA Write	1 Byte	Supported
DMA Write	2 Byte	Supported
DMA Write	4 Byte	Not Supported
DMA Read	1 Byte	Supported
DMA Read	2 Byte	Supported
DMA Read	4 Byte	Not Supported
Bus Master Memory Write	1 Byte	Not Supported
Bus Master Memory Write	2 Byte	Not Supported
Bus Master Memory Write	4 Byte	Not Supported
Bus Master Memory Read	1 Byte	Not Supported
Bus Master Memory Read	2 Byte	Not Supported
Bus Master Memory Read	4 Byte	Not Supported
Bus Master I/O Write	1 Byte	Not Supported

If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Programming High Speed Serial Port baud Rates

The SCH322x family of devices supports serial ports with speeds up to 1.5Mb/s. Changing the serial ports baud rates between standard speeds (115k baud and slower) during runtime is possible with standard drivers. In order to change baud rates to high speed (230k, 460k, 921k and 1.5M bauds) on the SCH322x devices during runtime, registers in both Configuration space and Runtime space must be programmed.

Note that this applies only if the application requires a serial port baud rate to change during runtime. Standard windows drivers could be used to select the specific high speed rate if it will remain unchanged during runtime Table 6-4 on page 45 shows the baud rates possible.

6.1.12 EFFECT OF THE RESET ON THE REGISTER FILE

The Reset Function (details the effect of the Reset input on each of the registers of the Serial Port.

6.1.13 FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = “1”, IER bit 0 = “1”), RCVR interrupts occur as follows:

- The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
- The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
- The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

- A FIFO timeout interrupt occurs if all the following conditions exist:

At least one character is in the FIFO.

The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).

The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12-bit character.

- Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
- When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
- When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = “1”, IER bit 1 = “1”), XMIT interrupts occur as follows:

- The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
- The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

6.1.16 NOTES ON SERIAL PORT OPERATION

FIFO Mode Operation:

General

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

6.1.16.1 TX and RX FIFO Operation

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

6.1.16.2 TXD2 Pin

The TXD2 signal is located on the GP53/TXD2(IRTX) pin. The operation of this pin following a power cycle is defined in Section 6.2.1, "IR Transmit Pin," on page 51.

6.2 Infrared Interface

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two IR implementations have been provided for the second UART in this chip (logical device 5), IrDA and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TXD2 and RXD2 pins. These can be selected through the configuration registers.

IrDA 1.0 allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows asynchronous serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

7.2.3 REGISTER DEFINITIONS

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. Table 7-4 lists these dependencies. Operation of the devices in modes other that those specified is undefined.

TABLE 7-4: ECP REGISTER DEFINITIONS

Name	Address (See Notes)	ECP Modes	Function
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.

2: All addresses are qualified with AEN. Refer to the AEN pin definition.

TABLE 7-5: MODE DESCRIPTIONS

Mode	Description
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	Reserved
110	Test mode
111	Configuration mode
*Refer to ECR Register Description	

7.2.4 DATA AND ECPAFIFO PORT

ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of ‘00H’ from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0).

9.2 SER_IRQ Cycle Control

There are two modes of operation for the SER_IRQ Start Frame

1. **Quiet (Active) Mode**: Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The SCH3227/SCH3226/SCH3224/SCH3222 which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle

2. **Continuous (Idle) Mode**: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

9.3 SER_IRQ Data Frame

Once a Start Frame has been initiated, the SCH3227/SCH3226/SCH3224/SCH3222 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the SCH3227/SCH3226/SCH3224/SCH3222 must drive the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ must be left tri-stated. During the Recovery phase the SCH3227/SCH3226/SCH3224/SCH3222 must drive the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the SCH3227/SCH3226/SCH3224/SCH3222 must tri-state the SER_IRQ.The SCH3227/SCH3226/SCH3224/SCH3222 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

SER_IRQ Sampling Periods		
SER_IRQ Period	**Signal Sampled**	**# of Clocks Past Start**
1	Not Used	2
2	IRQ1	5
3	nIO_SMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38

Host I/F Status Register

The Status register is 8 bits wide.

Table 10-3 shows the contents of the Status register.

TABLE 10-3: STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

Status Register

This register is cleared on a reset. This register is read-only for the Host and read/write by the SCH3227/SCH3226/SCH3224/SCH3222 CPU.

UD Writable by SCH3227/SCH3226/SCH3224/SCH3222 CPU. These bits are user-definable.

C/D (Command Data)-This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to “1” if SA2 = 1 or reset to “0” if SA2 = 0.

IBF (Input Buffer Full)- This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the SCH3227/SCH3226/SCH3224/SCH3222 CPU’s nIBF (MIRQ) interrupt if enabled. When the SCH3227/SCH3226/SCH3224/SCH3222 CPU reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full) - This flag is set to whenever the SCH3227/SCH3226/SCH3224/SCH3222 CPU write to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

10.7 External Clock Signal

The SCH3227/SCH3226/SCH3224/SCH3222 Keyboard Controller clock source is a 12 MHz clock generated from a 14.318 MHz clock. The reset pulse must last for at least 24 16 MHz clock periods. The pulse-width requirement applies to both internally (VCC POR) and externally generated reset signals. In power-down mode, the external clock signal is not loaded by the chip.

10.8 Default Reset Conditions

The SCH3227/SCH3226/SCH3224/SCH3222 has one source of hardware reset: an external reset via the PCI_RESET# pin. Refer to Table 10-4 for the effect of each type of reset on the internal registers.

TABLE 10-4: RESETS

Description	Hardware Reset (PCI_RESET#)
KCLK	Low
KDAT	Low
MCLK	Low
MDAT	Low
Host I/F Data Reg	N/A
Host I/F Status Reg	00H
Note: N/A = Not Applicable	

10.9 GATEA20 and Keyboard Reset

The SCH3227/SCH3226/SCH3224/SCH3222 provides two options for GateA20 and Keyboard Reset: 8042 Software Generated GateA20 and KRESET and Port 92 Fast GateA20 and KRESET.

15.0 PROGRAMMABLE CLOCK OUTPUT

A CLK_OUT pin is available on the SCH322x. This will output a programmable frequency between 0.5 Hz to 16 Hz, and have the following characteristics:

- Must run when Vcc if off - could use 32Khz clock
- Accuracy is not an issue
- CLOCK_OUT register at offset 3Ch in runtime registers with the following programming:
  - Options for 0.25, 0.5, 1, 2, 4, 8, or 16 Hz

APPLICATION NOTE: No attempt has been made to synchronize the clock. As a result, glitches will occur on the clock output when different frequencies are selected.

CLOCK Output Control Register VTR POR = 0x00	3C (R/W)	Bit[0] Enable 1= Output Enabled 0= Disable Clock output Bit[3:1] Frequency Select 000= 0.25 Hz 001= 0.50 Hz 010= 1.00 Hz 011= 2.00 Hz 100= 4.00 Hz 101= 8.00 Hz 110= 16 hz 111 = reserved Bit[7:4] Reserved

TABLE 16-3: WDT OPERATION FOLLOWING VCC_POR OR WDT2_CTL WRITING

WDT2_CTL	VCC_PORB	RST_WDT2B	Counter Reset	Condition
x	0	x	Yes	Power On
0	1	1	No	State after VCC_PORB. Counter starts Counting
0->1	1	1	Yes	Write 1 to WDT2_CTL. Counter reset and starts counting.
1->0	1	1	No	Write 0 to WDT2_CTL. No affect - counter running.
x	1	0	Yes	Counter timeout under normal conditions.

16.2 Voltage Scaling and Reset Generator Tolerances

The 5V supply is scaled internally. The input resistance is 20kohms (min). The voltage trip point is 4.45V (nominal) with a tolerance of ±0.15V (range: 4.3V-4.6V).

For the 3.3V VTR and 3.3V supplies, the voltage trip point is 2.8V (nominal) with a tolerance of ±0.1V (range: 2.7V-2.9V).

Refer to FIGURE 16-1: on page 102.

duty cycle will be held constant for a minimum of 18 periods (206/11.4 = 18.07) until the Ramp Logic increments/decrements the actual PWM duty cycle by '1'.

- If the period of the PWM output is greater than the step size created by the PWM Ramp Rate, the ramp rate logic will force the PWM output to increment/decrement the actual duty cycle in increments larger than 1/255. For example, if the PWM frequency is 11Hz (1/11Hz = 90.9msec) and the PWM Step time is 5msec, the PWM duty cycle output will be incremented 18 or 19 out of 255 (i.e., 90.9/5 = 18.18) until it reaches the calculated duty cycle. Note that the step size may be less if the calculated duty cycle minus the actual duty cycle is less than 18.

Note: The calculated PWM Duty cycle reacts immediately to a change in the temperature reading value. The temperature reading value may be updated once in 105.8msec (default) (see Table 21-2, "ADC Conversion Sequence," on page 126). The internal PWM duty cycle generated by the Ramp Rate control logic gradually ramps up/down to the calculated duty cycle at a rate pre-determined by the value programmed in the PWM Ramp Rate Control bits. The PWM output latches the internal duty cycle generated by the Ramp Rate Control Block every 1/(PWM frequency) seconds to determine the actual duty cycle of the PWM output pin.

PWM Output Transition from OFF to ON

When the calculated PWM Duty cycle generated by the auto fan control logic transitions from the 'OFF' state to the 'ON' state (i.e., Current PWM duty cycle>00h), the internal PWM duty cycle in the Ramp Rate Control Logic is initialized to the calculated duty cycle without any ramp time and the PWMx Current Duty Cycle register is set to this value. The PWM output will latch the current duty cycle value in the Ramp Rate Control block to control the PWM output.

PWM Output Transition from ON to OFF

Each PWM output has a control bit to determine if the PWM output will transition immediately to the OFF state (default) or if it will gradually step down to Off at the programmed Ramp Rate. These control bits (SZEN) are located in the PWMx Options registers at offsets 94h-96h.

TABLE 21-4: PWM RAMP RATE

RRx-[2:0]	PWM Ramp Time (sec) (Time from 33% Duty Cycle to 100% Duty Cycle)	PWM Ramp Time (sec) (Time from 0% Duty Cycle to 100% Duty Cycle)	Time per PWM Step (PWM Step Size = 1/255)	PWM Ramp Rate (Hz)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

occurred and the Tach Reading register will be set to either FFFEh or FFFFh depending on the state of the Slow Tach bits located in the TACHx Options registers at offsets 90h - 93h. Software can easily compute the RPM value using the tachometer reading value if it knows the number of edges per revolution.

Note 1: If the PWM output associated with a tach input is configured for the high frequency option then the tach input must be configured for Mode 1.

2: Some enhanced features added to support Mode 2, are available to Mode 1 also. They are: programmable number of tach edges and force tach reading register to FFFEh to indicate a SLOW fan.

3: Five edges or two tach pulses are generated per revolution.

4: If a tach input is left unconnected it must be configured for Mode 1.

21.14.2.4 Mode 2 – Monitor Tach input When PWM is 'ON'

In this mode, the PWM is used to pulse the Fan motor of a 3-wire fan. 3-wire fans use the same power supply to drive the fan motor and to drive the tachometer output logic. When the PWM is 'ON' the fan generates valid tach pulses. When the PWM is not driving the Fan, the tachometer signal is not generated and the tach signal becomes indeterminate or tristate. Therefore, Mode 2 only makes tachometer measurements when the associated PWM is driving high during an update cycle. As a result, the Fan tachometer measurement is "synchronized" to the PWM output, such that it only looks for tach pulses when the PWM is 'ON'.

Note:	Any fan tachometer input may be associated with any PWM output (see Linking Fan Tachometers to PWMs on page 155.)

During an update cycle, if an insufficient number of tachometer pulses are detected during this time period, the following applies: If at least one edge but less than the programmed number of edges is detected, the fan is considered slow. If no edge is detected, the fan is considered stopped.

Note 1: The interrupt status bits are set, if enabled, to indicate that a slow or stopped fan event has occurred when the tach reading registers are greater than the tach limit registers.

2: At some duty cycles, the programmed number of edges will appear during some PWM High times, but not all. If opportunistic mode is enabled, the tach logic will latch the count value any time it detects the programmed number of edges and reset the update counter. An interrupt will only be generated if no valid readings were made during the programmed update time.

21.14.2.5 Assumptions (refer to Figure 21-16 - PWM and Tachometer Concept):

The Tachometer pulse generates 5 transitions per fan revolution (i.e., two fan tachometer periods per revolution, edges 2→6). One half of a revolution (one tachometer period) is equivalent to three edges (2→4 or 3→5). One quarter of a revolution (one-half tachometer period) is equivalent to two edges. To obtain the fan speed, count the number of 90Khz pulses that occurs between 2 edges i.e., 2→3, between 3 edges i.e., 2→4, or between 5 edges, i.e. 2→6 (the case of 9 edges is not shown). The time from 1-2 occurs through the guard time and is not to be used. For the discussion below, an edge is a high-to-low or low-to-high transition (edges are numbered – refer to Figure 21-16 - PWM and Tachometer Concept.

The Tachometer circuit begins monitoring the tach when the associated PWM output transitions high and the guard time has expired. Each tach circuit will continue monitoring until either the "ON" time ends or the programmed number of edges has been detected, whichever comes first.

The Fan Tachometer value may be updated every 300ms, 500ms, or 1000ms.

See definition of Register 42h: Interrupt Status Register 2 on page 168 for setting and clearing bits.

Note: Only the primary status registers generate an interrupt event.

22.2.49 REGISTER A7H: INTERRUPT STATUS REGISTER 3 - SECONDARY

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A7h	R/WC	Interrupt Status Register 3-Secondary	RES	RES	RES	RES	RES	RES	VBAT	VTR	00h

Note 1: This register is reset to its default value when the PWRGD_PS signal transitions high.

2: This is a read/write-to-clear register. The status bits in this register are cleared on a write of one if the event causing the interrupt is no longer active. Writing a zero to these bits has no effect.

See definition of Register 83h: Interrupt Status Register 3 on page 182 for setting and clearing bits.

Note: Only the primary status registers generate an interrupt event.

22.2.50 REGISTER ABH: TACH 1-3 MODE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
ABh	R/W	Tach 1-3 Mode	T1M1	T1M0	T2M1	T2M0	T3M1	T3M0	RES	RES	00h

The following defines the mode control bits:

- bits[7:6]: Tach1 Mode
- bits[5:4]: Tach2 Mode.
- bits[3:2]: Tach3 Mode.
- bits[1:0]: RESERVED.

For bits[7:2], these bits are defined as follows:

- 00= normal operation (default)
- 01= locked rotor mode, active high signal
- 10= locked rotor mode, active low signal
- 11= undefined.

For bits[1:0], these bits are defined as RESERVED. Writes have no affect, reads return 00.

22.2.51 REGISTER ADH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
ADh	R	MCHP Test Register	7	6	5	4	3	2	1	0	00h

This is a read-only MCHP test register. Writing to this register has no effect.

22.2.52 REGISTERS AE-AFH, B3H: TOP TEMPERATURE LIMIT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
AEh	R/W	Top Temperature Remote Diode 1 (Zone 1)	7	6	5	4	3	2	1	0	2Dh
AFh	R/W	Top Temperature Remote Diode 2 (Zone 3)	7	6	5	4	3	2	1	0	2Dh
B3h	R/W	Top Temperature Ambient (Zone 2)	7	6	5	4	3	2	1	0	2Dh

Note: These registers are reset to their default values when the powergood_ps signal transitions high.

22.2.64 REGISTERS C4-C5, C9H: THERMTRIP TEMPERATURE LIMIT ZONE REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C4h	R/W	THERMTRIP Temp Limit ZONE 1 (Remote Diode 1)	7	6	5	4	3	2	1	0	7Fh
C9h	R/W	THERMTRIP Temp Limit ZONE 2 (Ambient)	7	6	5	4	3	2	1	0	7Fh
C5h	R/W	THERMTRIP Temp Limit ZONE 3 (Remote Diode 2)	7	6	5	4	3	2	1	0	7Fh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated THERMTRIP temperature limit (THERMTRIP Temp Limit ZONES 1-3). The THERMTRIP temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Temp Limit ZONE 1-3 registers represent the upper temperature limit for asserting nTHERMTRIP pin for each zone. These registers are defined as follows:

If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit ZONE 1-3 registers, the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERMTRIP Output Enable register).

Note: The zone must exceed the limits set in the associated THERMTRIP Temp Limit ZONE 1-3 register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

22.2.65 REGISTER CAH: THERMTRIP STATUS REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CAh	R/WC	THERMTRIP Status	RES	RES	RES	RES	RES	RD 2	RD 1	AMB	00h
Note:	Each bit in this register is cleared on a write of 1 if the event is not active.										

Note: This register is reset to its default value when the PWRGD_PS signal transitions high.

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to ‘1’ if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

22.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default).

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode
2. Configure the Configuration Registers
3. Exit Configuration Mode.

Enter Configuration Mode

To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. The config key consists of 0x55 written to the CONFIG PORT. Once the configuration key is received correctly the chip enters into the Configuration State (The auto Config ports are enabled).

Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In configuration mode, the INDEX PORT is located at the CONFIG PORT address and the DATA PORT is at INDEX PORT address + 1.

The desired configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note:	If accessing the Global Configuration Registers, step (a) is not required.

Exit Configuration Mode

To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note:	Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

Programming Example

The following is an example of a configuration program in Intel 8086 assembly language.

```
;-----------------------------.
; ENTER CONFIGURATION MODE    |
;-----------------------------'
MOV DX,02EH
MOV AX,055H
OUT DX,AL
;-----------------------------.
; CONFIGURE REGISTER CRE0,    |
; LOGICAL DEVICE 8            |
;-----------------------------'
MOV DX,02EH
MOV AL,07H
OUT DX,AL ;Point to LD# Config Reg
MOV DX,02FH
MOV AL, 08H
OUT DX,AL;Point to Logical Device 8
;
MOV DX,02EH
MOV AL,E0H
OUT DX,AL; Point to CRE0
MOV DX,02fH
MOV AL,02H
OUT DX,AL; Update CRE0
;-----------------------------.
; EXIT CONFIGURATION MODE     |
;-----------------------------'
MOV DX,02EH
MOV AX,0AAH
OUT DX,AL
```

TABLE 23-10: PARALLEL PORT, LOGICAL DEVICE 3 [LOGICAL DEVICE NUMBER = 0X03]

Name	REG Index	Definition
PP Mode Register Default = 0x3C on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bits[2:0] Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Bit[6:3] ECP FIFO Threshold 0111b (default) Bit[7] PP Interrupt Type Not valid when the parallel port is in the Printer Mode (100) or the Standard & Bi-directional Mode (000). = 1 Pulsed Low, released to high-Z. = 0 IRQ follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP. IRQ level type when the parallel port is in ECP, TEST, or Centronics FIFO Mode.
PP Mode Register 2 Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF1 R/W	Bit [3:0] Reserved. Set to zero. Bit [4] TIMEOUT_SELECT = 0 TMOUT (EPP Status Reg.) cleared on write of ‘1’ to TMOUT. = 1 TMOUT cleared on trailing edge of read of EPP Status Reg. Bits[7:5] Reserved. Set to zero.

TABLE 23-11: SERIAL PORT 1, LOGICAL DEVICE 4 [LOGICAL DEVICE NUMBER = 0X04]

Name	REG Index	Definition
Serial Port 1 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit [3:2] Enhanced Frequency Select = 00 Standard Mode (default) = 01 Select 921K = 10 Select 1.5M = 11 Reserved Bit[5:4] Reserved, set to zero Bit[6] All Share IRQ =0 Use bit 7 to determine sharing =1 Share all serial ports on the SCH3227/SCH3226/SCH3224/SCH3222 device. Bit[7]: Share IRQ =0 UARTs 1,2 use different IRQs =1 UARTs 1,2 share a common IRQ (Note 23-10)

Note 23-10 To properly share and IRQ:

- Configure UART1 (or UART2) to use the desired IRQ.
- Configure UART2 (or UART1) to use No IRQ selected.
- Set the share IRQ bit.

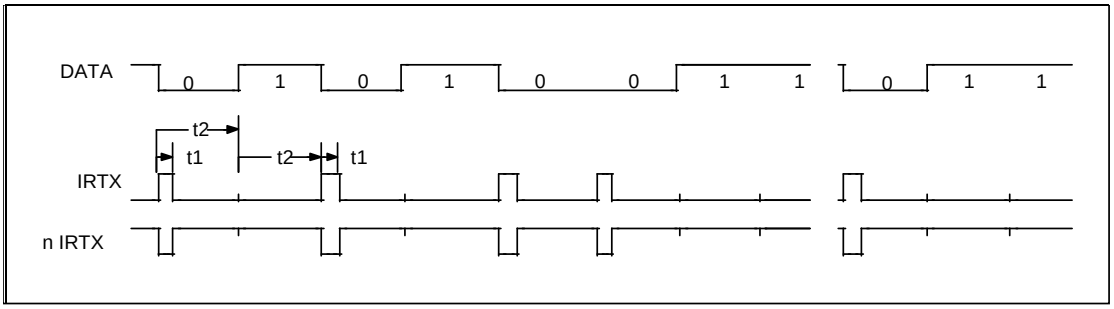
TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
Keyboard PWRBTN/SPEKEY (continued)		Bit [7] Keyboard PWRBTN/SPEKEY Lock (Note) (This bit is Reset on a Vbat POR, VTR POR, VCC POR, and PCI Reset) 0 = Keyboard PWRBTN/SPEKEY and Keyboard Scan Code Registers are Read/Write 1 = Keyboard PWRBTN/SPEKEY and Keyboard Scan Code Registers are Read Only **Note:** The following registers become Read-Only when Bit [7] is '1': • Keyboard Scan Code – Make Byte 1 at offset 5Fh • Keyboard Scan Code – Make Byte 2 at offset 60h • Keyboard Scan Code – Break Byte 1 at offset 61h • Keyboard Scan Code – Break Byte 2 at offset 62h • Keyboard Scan Code – Break Byte 3 at offset 63h • Keyboard PWRBTN/SPEKEY at offset 64h
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and PCI Reset	65 (R/W)	Watch-dog Timeout Bit[0] Reserved Bit[1] Reserved Bits[6:2] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and PCI Reset	66 (R/W)	Watch-dog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and PCI Reset	67 (R/W)	Watch-dog timer Configuration Bit[0] Reserved Bit[1] Keyboard Enable =1 WDT is reset upon a Keyboard interrupt. =0 WDT is not affected by Keyboard interrupts. Bit[2] Mouse Enable =1 WDT is reset upon a Mouse interrupt. =0 WDT is not affected by Mouse interrupts. Bit[3] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = IRQ2 (Note) 0001 = IRQ1 0000 = Disable **Note:** IRQ2 is used for generating SMI events via the serial IRQ's stream. The WDT should not be configured for IRQ2 if the IRQ2 slot is enabled for generating an SMI event.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP45 Default = 0x01 on VTR POR (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	6Fh (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=RXD6 0=GPIO (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
HW_Reg INDEX Default=0x00 on VTR POR (All except SCH3222)	70 (R/W)	The register is used to access the registers located in the H/W Monitoring Register block. The value in this register is the register INDEX (address), which determines the register currently accessible.
HW_Reg DATA Default=0x00 on VTR POR (All except SCH3222)	71 (R/W)	This register is used to Read/Write the data in the hardware monitoring register that is currently INDEX'd. (See the HW_Reg INDEX register at offset 60h.)
GP46 Default = 0x00 on VTR POR (SCH3227 or SCH3226, and STRAPOPT=0)	72h (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=GPIO 0=nPCI_RST2 (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP46 Default = 0x01 on VTR POR (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	72h (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nSCIN6 0=GPIO (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP47 Default = 0x00 on VTR POR (SCH3227 or SCH3226, and STRAPOPT=0)	73h (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=GPIO 0=nPCI_RST3 (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

FIGURE 27-20: IRDA TRANSMIT TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0