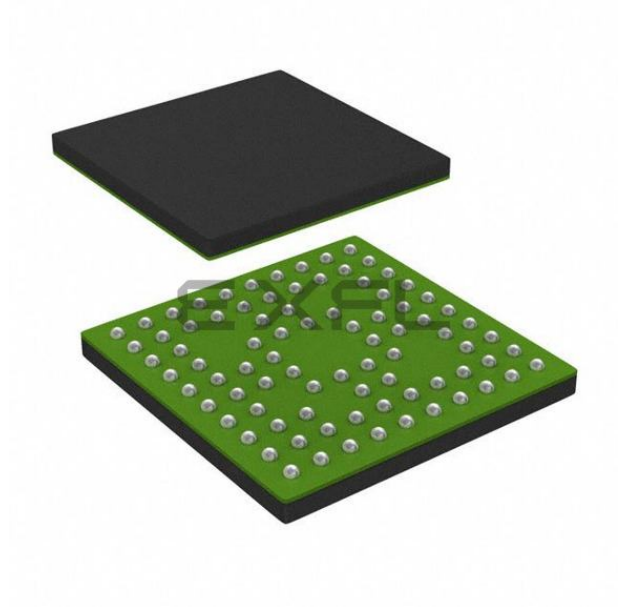

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	23
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-WFBGA
Supplier Device Package	84-WFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3222-sx

1.0 GENERAL DESCRIPTION

The SCH3227/SCH3226/SCH3224/SCH3222 Product Family is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. The Product Family also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

1.1 Scope and Definitions

For the purposes of this document, the term “SCH322x Family” refers only to the parts numbered SCH3227, SCH3226, SCH3224 and SCH3222. Similarly-numbered parts may also exist, but they are outside the scope of this document.

1.2 Important New Usage Considerations

The SCH322x Family is the next generation of the SCH311x family components. They mainly differ in the number of pins brought out of the package. In some cases (SCH3227, SCH3226) a new pin called STRAPOPT is brought out, allowing a hard-wired selection between the legacy SCH3114 vs. SCH3116 features of 8 of the pins. This selection also affects the Device ID register, which will display the legacy SCH3114 or SCH3116 code. Other SCH322x members, which do not have a STRAPOPT pin, are hard-wired internally to identify themselves as the legacy SCH3116.

CAUTION: This device contains circuits and registers affecting pin functions which must not be used when they are not brought out of the package. These pins are pulled to known states internally. Any features, especially Logical Devices and GPIOs, that are not listed in this document for a particular family member must not be activated, accessed, or in any way changed from its default reset state. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system. See Table 2-1 SCH3227, Table 2-2 SCH3226, Table 2-3 SCH3224, or Table 2-4 SCH3222, for the pin features that are brought out.

1.3 Feature Sets

See Table 1-1 on page 5 for features available per family member.

The Product Family is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard.

The Product Family supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, hardware IRQ and DMA Channel of each Logical Device may be reprogrammed through the internal configuration registers. There are up to 480 I/O address location options (960 for the Parallel Port), a Serialized IRQ interface, and a choice of three Legacy DMA channel assignments.

Super I/O functionality includes an 8042 based keyboard and mouse controller, one IrDA 1.0 infrared port and multiple serial ports. Some family members (Table 1-1) also provide an IEEE 1284 EPP/ECP compatible parallel port.

The serial ports are fully functional NS16550 compatible UARTs that support data rates up to 1.5 Mbps. There are both 8-pin Serial Ports and 4-pin Serial Ports. The reduced-pin serial ports have selectable input and output controls. The Serial Ports contain programmable direction control, which will automatically drive nRTS when the Output Buffer is loaded, then drive nRTS when the Output Buffer is empty.

Hardware Monitoring capability has programmable, automatic fan control. Three fan tachometer inputs and three pulse width modulator (PWM) fan control outputs are available.

Hardware Monitoring capability also includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans in response. There are four analog inputs for monitoring external voltages of +5V, +2.5V, +12V and Vccp (core processor voltage), as well as internal monitoring of the device’s internal VCC, VTR, and VBAT power supplies. Hardware Monitoring includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring local ambient temperature. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and fan speed conditions. Hardware Monitoring features are accessible via the LPC bus, and the same interrupt event reported on the nHWM_INT pin also creates PME wakeup events. A separate THERMTRIP output is available, which generates a pulse output on a programmed over-temperature condition. This can be used to generate a reset or shutdown indication to the system.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, a programmable Clock output, and reset generation. The reset generation includes a watchdog timer which can be used to generate a reset pulse. The width of this pulse is selectable via an external strapping option.

System related functionality, which offers flexibility to the system designer, includes General Purpose I/O control functions, and control of two LED's.

1.4 Reference Documents

1. Intel Low Pin Count Specification, Revision 1.0, September 29, 1997
2. PCI Local Bus Specification, Revision 2.2, December 18, 1998
3. Advanced Configuration and Power Interface Specification, Revision 1.0b, February 2, 1999
4. IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993
5. Hardware Description of the 8042, Intel 8 bit Embedded Controller Handbook
6. Application Note (AN 8-8) “Keyboard and Mouse Wakeup Functionality”, dated 03/23/02

TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
B2	+2.5V_IN	+2.5V_IN
--	RESERVED=N/C[d]: E9, F9, G9, H9, J5, J6, J7, J8, J9, G3, J11, K11, L4, L10	

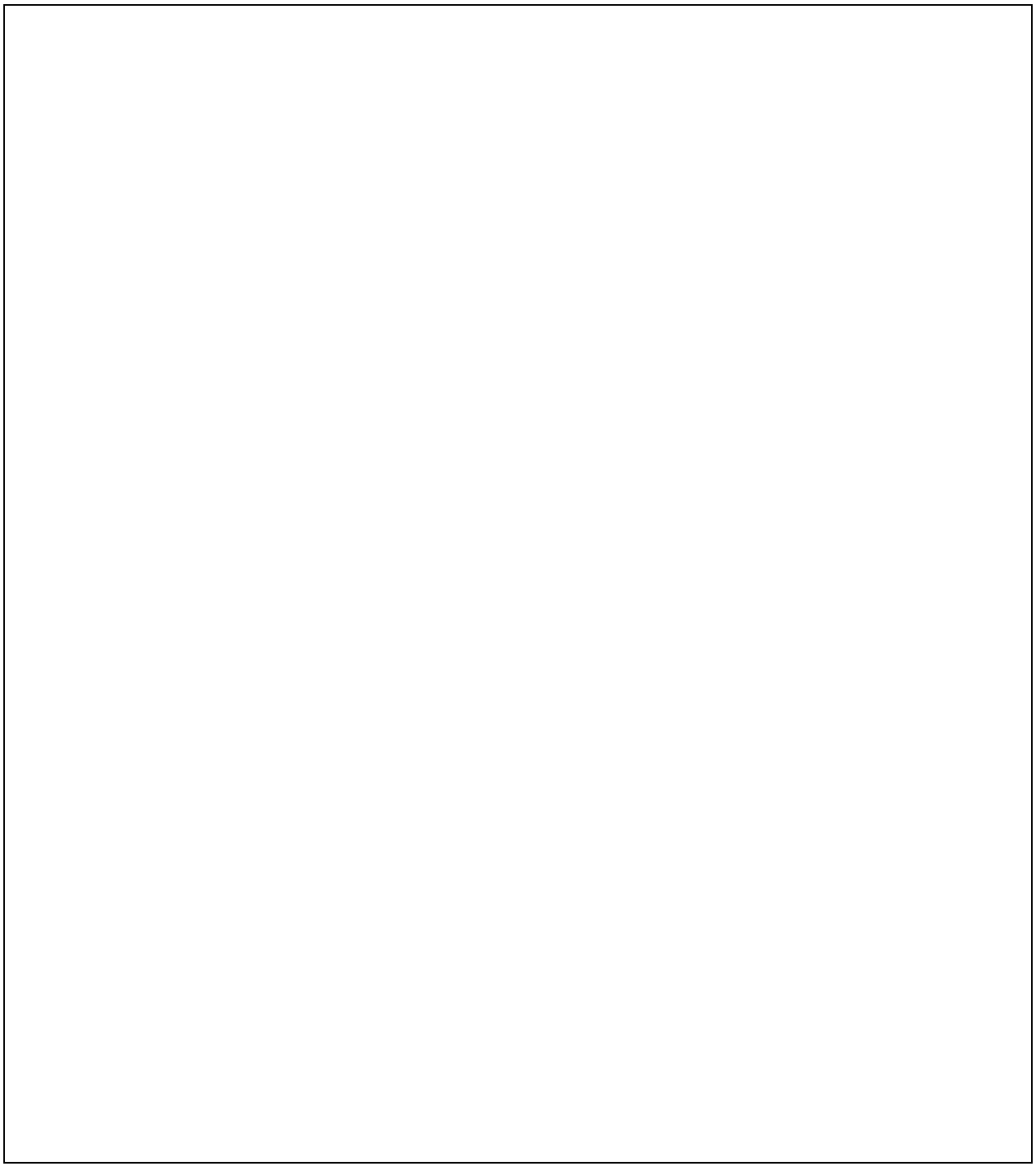
a. The STRAPOPT connection defines pin functions for this package, and also the contents of the Device ID register at Plug&Play Index 0x20:
When connected to VTR, the table column STRAPOPT=1 applies,
and Device ID = 0x7F.
When connected to VSS, the table column STRAPOPT=0 applies,
and Device ID = 0x7D.

b. For correct operation, this lead must always be connected to VTR.

c. For correct operation and minimal current consumption, this lead must always be connected to VSS.

d. Make No Connection to these leads.

FIGURE 2-4: SCH3222 PIN DIAGRAM



Note 2-10 This analog input is backdrive protected. Although HVTR is powered by VTR, it is possible that monitored power supplies may be powered when HVTR is off.

Note 2-11 The GP53/TXD2(IRTX) pin defaults to the GPIO input function on a VTR POR and presents a tristate impedance. When VCC=0 the pin is tristate. If GP53 function is selected and VCC is power is applied, the pin reflects the current state of GP53. The GP53/TXD2(IRTX) pin is tristate when it is configured for the TXD2 (IRTX) function under various conditions detailed in Section 6.2.1, "IR Transmit Pin," on page 51.

Note 2-12 The Reset and Glue Logic functions are only available on these pins in the SCH3227 and SCH3226 family members, requiring also that the STRAPOPT pin on these devices be tied low.
Serial Ports 5 and 6 are available on all family members, on the same pins, and also require (SCH3227 and SCH3226 only) that the STRAPOPT pin be pulled high.
In all the SCH322x family, GP44--47 have Schmitt trigger inputs.

Note 2-13 The pins listed here are pins used in all of the SCH322x devices.

Note 2-14 All logic is powered by VTR. Vcc on pin 29 is used as an indication of the presence of the VCC rail being active. All logic that requires VCC power, is only enabled when the VCC rail is active.

Note 2-15 The GP55/nRTS2/RESGEN pin requires an external pull-down resistor to enable 500ms delay circuit. An external pull-up resistor is required to enable 200ms delay circuit.

USER'S NOTE:

Open-drain pins should be pulled-up externally to supply shown in the power well column. All other pins are driven under the power well shown.

- NOMENCLATURE:
  - No Gate indicates that the pin is not protected, or affected by VCC=0 operation
  - Gate indicates that the pin is protected as an input (if required) or set to a HI-Z state as an output (if required)
  - In these columns, information is given in order of pin function: e.g. 1st pin function / 2nd pin function

2.3 Buffer Description

Table 2-6 lists the buffers that are used in this device. A complete description of these buffers can be found in Section 26.0, "Operational Description," on page 252.

TABLE 2-6: BUFFER DESCRIPTION

Buffer	Description
I	Input TTL Compatible - Super I/O Block.
IL	Input, Low Leakage Current.
I_M	Input - Hardware Monitoring Block.
I_{AN}	Analog Input, Hardware Monitoring Block.
I_{ANP}	Back Bias Protected Analog Input, Hardware Monitoring Block.
I_{AND-}	Remote Thermal Diode (current sink) Negative Input
I_{AND+}	Remote Thermal Diode (current source) Positive Input
IS	Input with Schmitt Trigger.
I_VID	Input. See DC Characteristics Section.
I_MOD3	Input/Output (Open Drain), 3mA sink.
I_MO3	Input/Output, 3mA sink, 3mA source.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
IOD8	Input/Open Drain Output, 8mA sink, 4mA source.
IS/O8	Input with Schmitt Trigger/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.

7.1.7 EPP DATA PORT 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.1.8 EPP DATA PORT 3

ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.1.9 EPP 1.9 OPERATION

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

7.1.10 SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

7.1.11 EPP 1.9 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

- If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
- If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host initiates an I/O write cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
6.
   a) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b) The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.
7. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
8. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

7.2.5 DEVICE STATUS REGISTER (DSR)

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

Bit 3 nFault

The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

Bit 4 Select

The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

Bit 5 PError

The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

Bit 6 nAck

The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

Bit 7 nBusy

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

7.2.6 DEVICE CONTROL REGISTER (DCR)

ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

Bit 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

Bit 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

Bit 2 nINIT - INITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

Bit 3 SELECTIN

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

Bit 4 ackIntEn - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

Bit 5 DIRECTION

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)

Case 1: Keyboard and/or Mouse Powered by VTR

The KBD and/or MOUSE status bits will be set upon a VTR POR if the keyboard and/or mouse are powered by VTR.

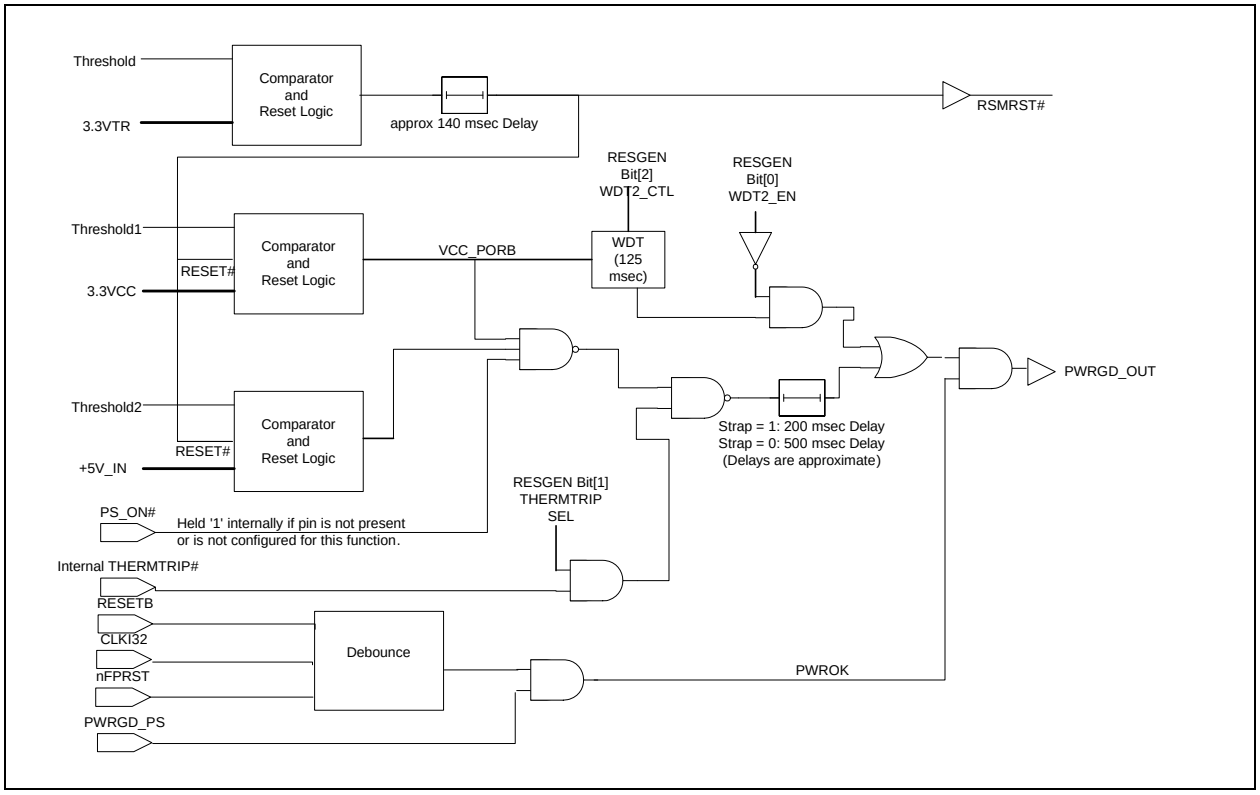
In this case, a nIO_PME will not be generated, since the keyboard and mouse PME enable bits are reset to zero on a VTR POR. The BIOS software needs to clear these PME status bits after power-up.

In this case, an nIO_PME will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are Bvat powered. Therefore, if the keyboard and mouse are powered by VTR, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VTR is removed (i.e., S4 or S5) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME and/or wake events from the power states S3 or below.

Case 2: Keyboard and/or Mouse Powered by VCC

The KBD and/or MOUSE status bits will be set upon a VCC POR if the keyboard and/or mouse are powered by VCC. In this case, a nIO_PME and a nIO_PME will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are VTRor Vbat powered. Therefore, if the keyboard and mouse are powered by VCC, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VCC is removed (i.e., S3) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME and/or wake events from the S0 and/or S1 states. The BIOS software needs to clear these PME status bits after power-up.

FIGURE 16-1: RESET GENERATION CIRCUIT (FOR ILLUSTRATIVE PURPOSES ONLY)



16.1 Watchdog Timer for Resets on VCC_POR

The current WDT implementation resets after a VCC_POR, and does not begin counting until after WDT2_CTL bit is toggled. The current operation of the RESGEN watchdog timer is as follows:

1. Feature enable/disable via a bit in a control register, accessible from the LPC. When enabled, the RESGEN WDT output is selected as a source for the PWRGD_OUT signal.
2. Watchdog input bit in a the RESGEN register, WDT2_CTL, reset to 0 via VCC_POR, accessible from the LPC. See Table 16-3.
3. The counter is reset by VCC_POR. The counter will remain reset as long as VCC_POR is active.
4. Counter will start when the following conditions are met:
   a) VCC_POR is released AND
   b) The WDT2_CTL bit is toggled from 0 to 1
5. If the host toggles the WDT2_CTL bit in the RESGEN control register, then the counter is reset to 1.6 seconds and begins to count.
6. If the host does not toggle the WDT2_CTL bit in the RESGEN register by writing a 0 followed by a 1, before the WDT has timed out, a 100 msec pulse is output.
7. After a timeout has occurred, a new timeout cycle does not begin until the host toggles the WDT2_CTL bit in RESGEN register, by writing a 0 followed by a 1. This causes the counter to be reset to 1.6 seconds and begins to count again.

18.3.2 POWER SUPPLY TIMING DIAGRAMS

The following diagrams show the relative timing for the I/O pins associated with the Power Control logic. These are conceptual diagrams to show the flow of events.

FIGURE 18-3: POWER SUPPLY DURING NORMAL OPERATION

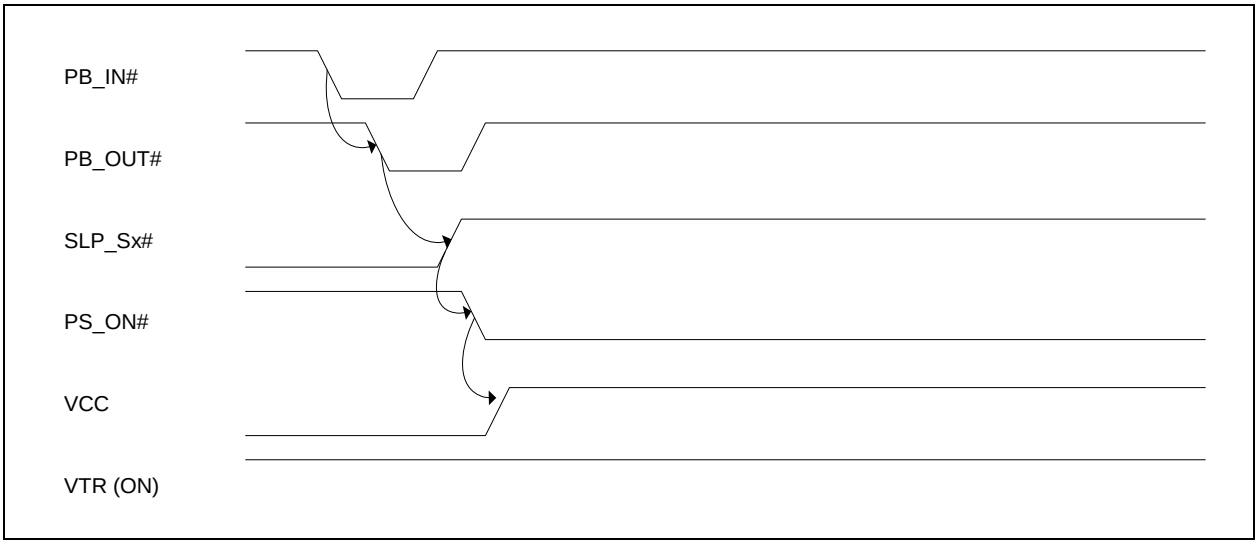


FIGURE 18-4: POWER SUPPLY AFTER POWER FAILURE (RETURN TO OFF)

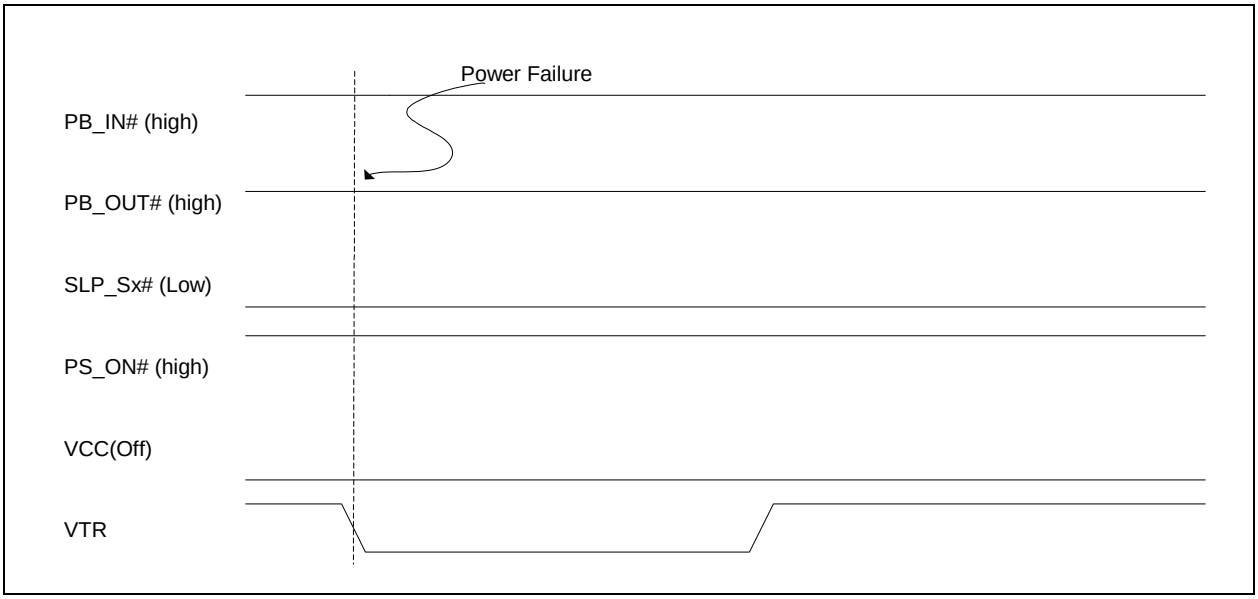
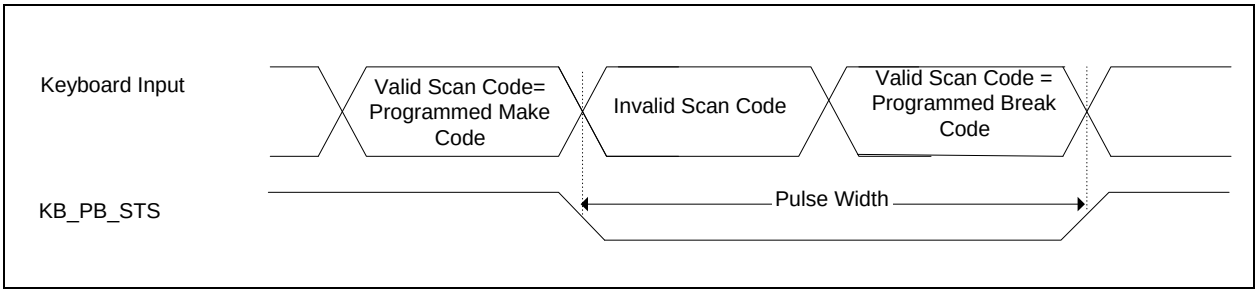


FIGURE 18-10: OPTION 3: DE-ASSERT KB_PB_STS WHEN SCAN CODE EQUAL BREAK CODE.



Note: The SPEKEY ScanCode bits are located in the register Keyboard PWRBTN/SPEKEY located at offset 64h.

TABLE 18-5: DECODING KEYBOARD SCAN CODE FOR BREAK CODE

SPEKEY Scan Code		Scan Code	Number of Bytes in Break Code	Description
Bit[3]	Bit[2]			
0	0	Scan 1	1 Byte	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit.
0	1	Scan 1	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.
1	0	Scan 2	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.

21.4.2 VCC POWER-ON RESET

The PWRGD_PS signal is used by the hardware-monitoring block to determine when a VCC POR has occurred. The PWRGD_PS signal indicates that the VCC power supply is within operation range and the 14.318MHz clock source is valid.

Note: Throughout the description of the hardware monitoring block VCC POR and PWRGD_PS are used interchangeably, since the PWRGD_PS is used to generate a VCC POR.

All the HWM registers will retain their value through a sleep cycle unless otherwise specified. If a VCC POR is preceded by a VTR POR the registers will be reset to their default values. The following is a list of the registers and bits that are reset to their default values following a VCC POR.

- FANTACH1 LSB register at offset 28h
- FANTACH1 MSB register at offset 29h
- FANTACH2 LSB register at offset 2Ah
- FANTACH2 MSB register at offset 2Bh
- FANTACH3 LSB register at offset 2Ch
- FANTACH3 MSB register at offset 2Dh
- Bit[1] LOCK of the Ready/Lock/Start register at offset 40h
- Zone 1 Low Temp Limit at offset 67h
- Zone 2 Low Temp Limit at offset 68h
- Zone 3 Low Temp Limit at offset 69h
- Bit[3] TRDY of the Configuration register at offset 7Fh
- Top Temperature Remote diode 1 (Zone 1) register at offset AEh
- Top Temperature Remote diode 2 (Zone 3) register at offset AFh
- Top Temperature Ambient (Zone 2) register at offset B3h

21.4.3 SOFT RESET (INITIALIZATION)

Setting bit 7 of the Configuration Register (7Fh) performs a soft reset on all the Hardware Monitoring registers except the reading registers. This bit is self-clearing.

21.5 Clocks

The hardware monitor logic operates on a 90kHz nominal clock frequency derived from the 14MHz clock input to the SIO block. The 14MHz clock source is also used to derive the high PWM frequencies.

21.6 Input Monitoring

The SCH322x device's monitoring function is started by writing a '1' to the START bit in the **Ready/Lock/Start** Register (0x40). Measured values from the temperature sensors are stored in Reading Registers. The values in the reading registers can be accessed via the LPC interface. These values are compared to the programmed limits in the Limit Registers. The out-of-limit and diode fault conditions are stored in the Interrupt Status Registers.

Note: All limit and parameter registers must be set before the START bit is set to '1'. Once the start bit is set, these registers become read-only.

21.7 Monitoring Modes

The Hardware Monitor Block supports two Monitoring modes: Continuous Mode and Cycle Mode. These modes are selected using bit 1 of the Special Function Register (7Ch). The following subsections contain a description of these monitoring modes.

The time to complete a conversion cycle depends upon the number of inputs in the conversion sequence to be measured and the amount of averaging per input, which is selected using the AVG[2:0] bits in the Special Function register (see the Special Function Register, 7Ch).

For each mode, there are four options for the number of measurements that are averaged for each temperature reading. These options are selected using bits[7:5] of the Special Function Register (7Ch). These bits are defined as follows:

21.14.2.9 Examples of Minimum RPMs Supported

The following tables show minimum RPMs that can be supported with the different parameters. The first table uses 3 edges and the second table uses 2 edges.

TABLE 21-5: MINIMUM RPM DETECTABLE USING 3 EDGES

PWM Frequency	Pulse Width at Duty Cycle (PWM "ON" Time)			Minimum RPM at Duty Cycle (Note 21-2) ($30/T_{TachPulse}$)		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 21-1)	25%	50%	100%
87.7	2.85	5.7	11.36	10865	5347	2662
58.6	4.27	8.53	17	7175	3554	1774
44	5.68	11.36	22.64	5366	2662	1330
35.2	7.1	14.2	28.3	4279	2126	1063
29.3	8.53	17.06	34	3554	1768	885
21.9	11.42	22.83	45.48	2648	1319	661
14.6	17.12	34.25	68.23	1761	878	440
11	22.73	45.45	90.55	1325	661	332

Note 21-1 100% duty cycle is 255/256

Note 21-2 RPM=60/$T_{Revolution}$, $T_{TachPulse}$= $T_{Revolution}$/2. Using 3 edges for detection, $T_{TachPulse}$ = (PWM "ON" Time – Guard Time). Minimum RPM values shown use minimum guard time (88.88usec).

TABLE 21-6: MINIMUM RPM DETECTABLE USING 2 EDGES

PWM Frequency	Pulse Width at Duty Cycle (PWM "ON" Time)			Minimum RPM at Duty Cycle (Note 21-4) ($30/T_{TachPulse}$)		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 21-3)	25%	50%	100%
87.7	2.85	5.7	11.36	5433	2673	1331
58.6	4.27	8.53	17	3588	1777	887
44	5.68	11.36	22.64	2683	1331	665
35.2	7.1	14.2	28.3	2139	1063	532
29.3	8.53	17.06	34	1777	884	442
21.9	11.42	22.83	45.48	1324	660	330
14.6	17.12	34.25	68.23	881	439	220
11	22.73	45.45	90.55	663	331	166

Note 21-3 100% duty cycle is 255/256

Note 21-4 RPM=60/$T_{Revolution}$, $T_{TachPulse}$= $T_{Revolution}$/2. Using 2 edges for detection, $T_{TachPulse}$ = 2*(PWM "ON" Time-Guard Time). Minimum RPM values shown use minimum guard time (88.88usec).

21.14.2.10 Detection of a Stalled Fan

There is a fan failure bit (TACHx) in the interrupt status register used to indicate that a slow or stalled fan event has occurred. If the tach reading value exceeds the value programmed in the tach limit register the interrupt status bit is set. See Interrupt Status register 2 at offset 42h.

Note 1: The reading register will be forced to FFFFh if a stalled event occurs (i.e., stalled event =no edges detected.)

2: The reading register will be forced to either FFFFh or FFFEh if a slow fan event occurs. (i.e., slow event: 0 < #edges < programmed #edges). If the control bit, SLOW, located in the TACHx Options registers at offsets 90h - 93h, is set then FFFEh will be forced into the corresponding Tach Reading Register to indicate that the fan is spinning slowly.

clear the status bit. Setting or clearing the START bit when the individual enable bit is one has no effect on the status bits.

Note 1: The individual enable bits for D2, AMB, and D1 are located in the Interrupt Enable 3 (Temp) register at offset 82h.

2: Clearing the group Temp enable bit or the global INTEN enable bit has no effect on the status bits.

Bit	Name	R/W	Default	Description
0	2.5V_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the Vccp input voltage is less than or equal to the limit set in the Vccp Low Limit register or greater than the limit set in the Vccp High Limit register.
2	VCC_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the VCC input voltage is less than or equal to the limit set in the VCC Low Limit register or greater than the limit set in the VCC High Limit register.
3	5V_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Remote Diode 1 Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ is less than or equal to the limit set in the Remote Diode 1 Low Temp register or greater than the limit set in Remote Diode 1 High Temp register.
5	Internal Sensor Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal Low Temp register or greater than the limit set in the Internal High Temp register.
6	Remote Diode 2 Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the Remote2- and Remote2+ is less than or equal to the limit set in the Remote Diode 2 Low Temp register or greater than the limit set in the Remote Diode 1 High Temp register.
7	INT2 Event Active	R/WC	0	The device automatically sets this bit to 1 when a status bit is set in the Interrupt Status Register 2.

22.2.11 REGISTER 42H: INTERRUPT STATUS REGISTER 2

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
42h	R/WC	Interrupt Status Register 2	ERR2	ERR1	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	RES	12V	00h

Note 1: This register is reset to its default value when the PWRGD_PS signal transitions high.

2: This is a read/write-to-clear register. The status bits are cleared on a write of one if the event causing the interrupt is no longer active. Writing a zero to these bits has no effect.

The Interrupt Status Register 2 bits is automatically set by the device whenever a tach reading value is above the minimum value set in the tachometer minimum registers or when a remote diode fault occurs. When a remote diode fault occurs (if the start bit is set) 80h will be loaded into the associated temperature reading register, which causes the associated diode limit error bit to be set (see Register 41h: Interrupt Status Register 1 on page 167) in addition to the diode fault bit (ERRx). These individual status bits remain set until the bit is written to one by software or until the individual enable bit is cleared, even if the event no longer persists.

- Clearing the status bits by a write of ‘1’
  - The FANTACHx status bits are cleared (set to 0) automatically by the SCH322x after they are written to one by software, if the FANTACHx reading register no longer violates the programmed FANTACH Limit. (See Registers 28-2Dh: Fan Tachometer Reading on page 164 and Registers 54-59h: Fan Tachometer Low Limit on page 171)

22.2.18 REGISTERS 64-66H: MINIMUM PWM DUTY CYCLE

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
64h	R/W	PWM1 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h
65h	R/W	PWM2 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h
66h	R/W	PWM3 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These registers specify the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting in Auto Fan Control Mode.

TABLE 22-12: PWM DUTY VS. REGISTER SETTING

Minimum PWM Duty	Value (Decimal)	Value (HEX)
0%	0	00h
. . .	. . .	. . .
25%	64	40h
. . .	. . .	. . .
50%	128	80h
. . .	. . .	. . .
100%	255	FFh

22.2.19 REGISTERS 67-69H: ZONE LOW TEMPERATURE LIMIT

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
67h	R/W	Zone 1 (Remote Diode 1) Low Temp Limit	7	6	5	4	3	2	1	0	80h Note 22-18
68h	R/W	Zone 2 (Ambient) Low Temp Limit	7	6	5	4	3	2	1	0	80h Note 22-18
69h	R/W	Zone 3 (Remote Diode 2) Low Temp Limit	7	6	5	4	3	2	1	0	80h Note 22-18

Note 22-18 This register is reset to the default value following a VCC POR when the PWRGD_PS signal is asserted.

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the auto fan algorithm based on the setting in the Zone x Range / PWMx Frequency register. Default = 90°C=5Ah.

Bit[4] 3 Edge Detection (Mode 2 only)

0= Don't ignore first 3 edges (default)

1= Ignore first 3 tachometer edges after guard time

Note:	This bit has been added to support a small sampling of fans that emit irregular tach pulses when the PWM transitions 'ON'. Typically, the guard time is sufficient for most fans.

Bit[7:5] Reserved

22.2.40 REGISTERS 94H-96H: PWMX OPTION REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
94h	R/W	PWM1 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch
95h	R/W	PWM2 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch
96h	R/W	PWM3 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[1:0] Tachs reading registers associated with PWMx are updated: (Mode 2 only)

00= once a second (default)

01= twice a second

1x= every 300msec

Bit[2] Snap to Zero (SZEN)

This bit determines if the PWM output ramps down to OFF or if it is immediately set to zero.

0= Step Down the PWMx output to Off at the programmed Ramp Rate

1= Transition PWMx to Off immediately when the calculated duty cycle is 00h (default)

Bit[4:3] Guard time (Mode 2 only)

00= 63 clocks (90kHz clocks ~ 700usec)

01= 32 clocks (90kHz clocks ~ 356usec) (default)

10= 16 clocks (90kHz clocks ~ 178usec)

11= 8 clocks (90kHz clocks ~ 89usec)

Bit[5] Opportunistic Mode Enable

0= Opportunistic Mode Disabled. Update Tach Reading once per PWMx Update Period (see Bits[1:0] in this register)

1= Opportunistic Mode is Enabled. The tachometer reading register is updated any time a valid tachometer reading can be made during the 'on' time of the PWM output signal. If a valid reading is detected prior to the Update cycle, then the Update counter is reset.

Bit[7:6] Reserved

22.2.41 REGISTER 97H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
97h	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	5Ah

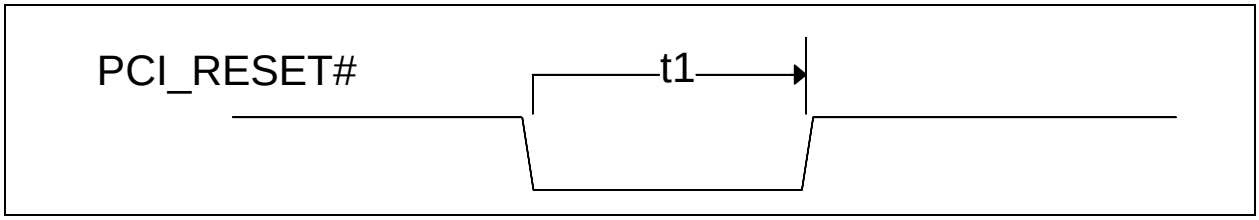
These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This is an MCHP Test Register. Writing to this register may cause unwanted results.

TABLE 24-2: RUNTIME REGISTER POR SUMMARY (CONTINUED)

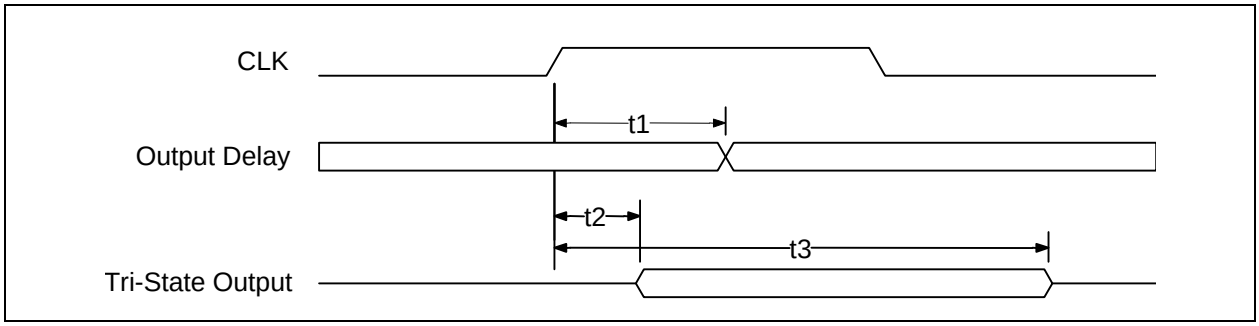
Register Offset (HEX)	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Vbat POR	Register
54	R	-	-	0x01	-	-	GP62
55	R	-	-	0x01	-	-	GP63
56	R	-	-	0x01	-	-	GP64
57	R	-	-	0x01	-	-	GP65
58	R	-	-	0x01	-	-	GP66
59	R	-	-	0x01	-	-	GP67
5A	R	-	-	-	-	-	TEST
5B	Note 2 4-17	-	-	-	-	0x0C	DBLCLICK
5C	Note 2 4-17	Note 24-9	Note 24-9	Note 24-9	-	-	Mouse_Specific_ Wake
5D	R/W	-	-	0x00	-	-	LED1
5E	R/W	-	-	0x00	-	-	LED2
5F	Note 2 4-13	-	-	-	-	0xE0	Keyboard Scan Code – Make Byte 1
60	Note 2 4-13	-	-	-	-	0x37	Keyboard Scan Code – Make Byte 2
61	Note 2 4-13	-	-	-	-	0xE0	Keyboard Scan Code – Break Byte 1
62	Note 2 4-13	-	-	-	-	0xF0	Keyboard Scan Code – Break Byte 2
63	Note 2 4-13	-	-	-	-	0x37	Keyboard Scan Code – Break Byte 3
64	Note 2 4-13	Note 24-9	Note 24-9	Note 24-9	-	Note 24-9	Keyboard PWRBTN/SPEKEY
65	R/W	0x00	0x00	0x00	-	-	WDT_TIME_OUT
66	R/W	0x00	0x00	0x00	-	-	WDT_VAL
67	R/W	0x00	0x00	0x00	-	-	WDT_CFG
68	R/W Note 2 4-15	0x00 Note 24-14	0x00	0x00	-	-	WDT_CTRL
69	R	-	-	-	-	-	Reserved – reads return 0
6A	R	-	-	-	-	-	Reserved – reads return 0
6B	R	-	-	-	-	-	Reserved – reads return 0
6C	R	-	-	-	-	-	Reserved – reads return 0
6D	R	-	-	-	-	-	Reserved – reads return 0
6E	R	-	-	-	-	-	Reserved – reads return 0 (SCH3227 or SCH3226, and STRAPOPT=0)
6E	R/W	-	-	0x01	-	-	GP44 (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)
6F	R/W	-	-	0x00	-	-	GP45 (SCH3227 or SCH3226, and STRAPOPT=0)
6F	R/W	-	-	0x01	-	-	GP45 (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)

FIGURE 27-4: RESET TIMING



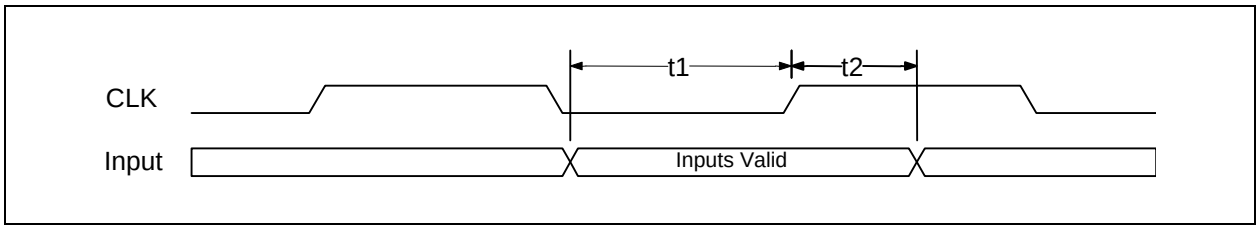
Name	Description	MIN	TYP	MAX	Units
t1	PCI_RESET# width	1			ms

FIGURE 27-5: OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS



Name	Description	MIN	TYP	MAX	Units
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

FIGURE 27-6: INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS



Name	Description	MIN	TYP	MAX	Units
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns

Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

APPENDIX C: TEST MODE

The SCH322x provides board test capability through the implementation of one XNOR chain and one XOR chain. The XNOR chain is dedicated to the Super I/O portion and the Hardware Monitoring Block of the device.

Note:	Pins that are not brought out of the package are tied to a determinate voltage internal to the package, and so will not affect the XNOR output, except that its initial state may differ among family members.

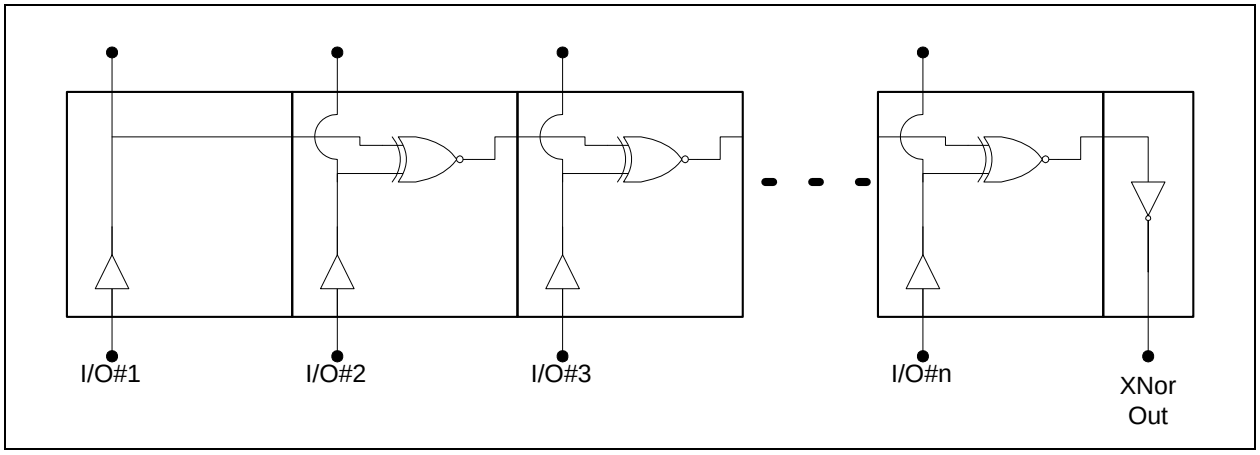
C.1 XNOR-Chain Test Mode Overview

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure C-1. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SCH322x pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

FIGURE C-1: XNOR-CHAIN TEST STRUCTURE



C.1.1 Board Test Mode

Board test mode can be entered as follows:

On the rising (deasserting) edge of PCI_RESET#, drive LFRAME# low and drive LAD[0] low.

Exit board test mode as follows:

On the rising (deasserting) edge of PCI_RESET#, drive either LFRAME# or LAD[0] high.

The PCI_RESET# pin is not included in the XNOR-Chain. The XNOR-Chain output pin# is TXD1. See the following sub-sections for more details.

Pin List of XNOR Chain

All pins on the chip are inputs to the first XNOR chain, with the exception of the following:

- All power supply pins - HVTR, HVSS, VCC, VTR, and Vbat
- VSS and AVSS
- All analog inputs: Remote2-, Remote2+, Remote1-, Remote1+, VCCP_IN, +12V_IN, +5V_IN, +2.5V_IN
- TXD1 This is the chain output.
- PCI_RESET#.

APPENDIX D: DATA SHEET REVISION HISTORY

TABLE D-1: SCH3227/SCH3226/SCH3224/SCH3222 REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002121B (03-20-17)	Figure 2-2, "SCH3226 Pin Diagram" and Figure 2-3, "SCH3224 Pin Diagram"	Updated diagrams
	Table 2-2, "SCH3226 Summaries By Strap Option", Table 2-3, "SCH3224 Summary" and Table 2-4, "SCH3222 Summary"	Added footnote to pin TEST, indicating that a connection to VSS is necessary.
DS00002121A (03-02-16)	Document Release	