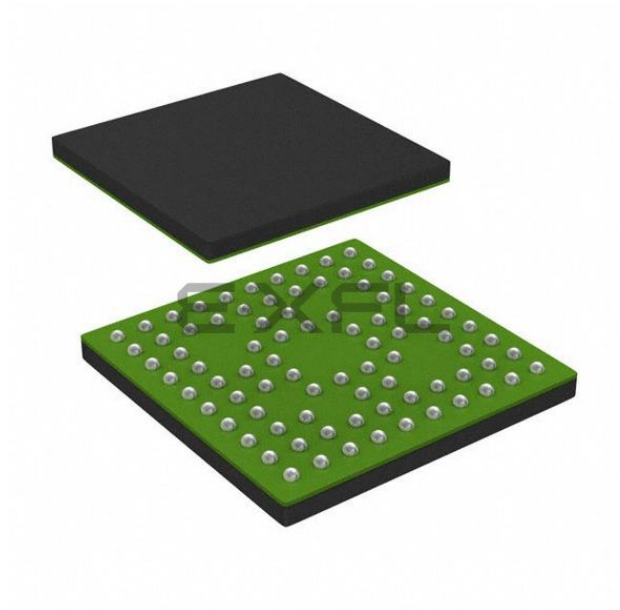

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	23
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-WFBGA
Supplier Device Package	84-WFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3222i-sx-tr

Keyboard Data Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

Keyboard Data Read

This is an 8 bit read only register. If enabled by “ENABLE FLAGS”, when read, the KIRQ output is cleared and the OBF flag in the status register is cleared. If not enabled, the KIRQ and/or AUXOBF1 must be cleared in software.

Keyboard Command Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register for more information.

CPU-to-Host Communication

The SCH3227/SCH3226/SCH3224/SCH3222 CPU can write to the Output Data register via register DBB. A write to this register automatically sets Bit 0 (OBF) in the Status register. See Table 10-2.

TABLE 10-2: HOST INTERFACE FLAGS

8042 Instruction	Flag
OUT DBB	Set OBF, and, if enabled, the KIRQ output signal goes high

Host-to-CPU Communication

The host system can send both commands and data to the Input Data register. The CPU differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is “1”, the CPU interprets the register contents as a command. When bit 3 is “0”, the CPU interprets the register contents as data. During a host write operation, bit 3 is set to “1” if SA2 = 1 or reset to “0” if SA2 = 0.

KIRQ

If “EN FLAGS” has been executed and P24 is set to a one: the OBF flag is gated onto KIRQ. The KIRQ signal can be connected to system interrupt to signify that the SCH3227/SCH3226/SCH3224/SCH3222 CPU has written to the output data register via “OUT DBB,A”. If P24 is set to a zero, KIRQ is forced low. On power-up, after a valid RST pulse has been delivered to the device, KIRQ is reset to 0. KIRQ will normally reflects the status of writes “DBB”. (KIRQ is normally selected as IRQ1 for keyboard support.)

If “EN FLAGS” has not been executed: KIRQ can be controlled by writing to P24. Writing a zero to P24 forces KIRQ low; a high forces KIRQ high.

MIRQ

If “EN FLAGS” has been executed and P25 is set to a one:; IBF is inverted and gated onto MIRQ. The MIRQ signal can be connected to system interrupt to signify that the SCH3227/SCH3226/SCH3224/SCH3222 CPU has read the DBB register. If “EN FLAGS” has not been executed, MIRQ is controlled by P25, Writing a zero to P25 forces MIRQ low, a high forces MIRQ high. (MIRQ is normally selected as IRQ12 for mouse support).

Gate A20

A general purpose P21 is used as a software controlled Gate A20 or user defined output.

8042 PINS

The 8042 functions P17, P16 and P12 are implemented as in a true 8042 part. Reference the 8042 spec for all timing. A port signal of 0 drives the output to 0. A port signal of 1 causes the port enable signal to drive the output to 1 within 20-30nsec. After 500nsec (six 8042 clocks) the port enable goes away and the external pull-up maintains the output signal as 1.

In 8042 mode, the pins can be programmed as open drain. When programmed in open drain mode, the port enables do not come into play. If the port signal is 0 the output will be 0. If the port signal is 1, the output tristates: an external pull-up can pull the pin high, and the pin can be shared. In 8042 mode, the pins cannot be programmed as input nor inverted through the GP configuration registers.

TABLE 11-2: SCH322X GENERAL PURPOSE I/O PORT ASSIGNMENTS (CONTINUED)

Run-Time REG Offset (HEX)	DEF	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	GP Data REG	GP Data Bit
3F	GPIO50	Ring Indicator 2			GP5 OFFSET 4F	0
40	GPIO51	Data Carrier Detect 2				1
41	GPIO52	Receive Serial Data 2				2
42	GPIO53	Transmit Serial Data 2				3
43	GPIO54	Data Set Ready 2				4
44	GPIO55	Request to Send 2				5
45	GPIO56	Clear to Send 2				6
46	GPIO57	Date Terminal Ready				7
47	GPIO60 Note 11-7	nLED1	WDT	WDT	GP6 OFFSET 50	0
48	GPIO61 Note 11-7	nLED2	CLKO			1
54	GPIO62 Note 11-8	nCTS4				2
55	GPIO63 Note 11-8	nDCD4				3
56	GPIO64 Note 11-8	RXD4				4
57	GPIO65 Note 11-8	TXD4				5
58	GPIO66 Note 11-8	nDSR4				6
59	GPIO67 Note 11-8	nRTS4				7

Note 11-6 When this pin function is selected, the associated GPIO pins have bi-directional functionality.

Note 11-7 These pins have Either Edge Triggered Interrupt (EETI) functionality. See Section 11.5, "GPIO PME and SMI Functionality," on page 91 for more details.

Note 11-8 These pins have VID compatible inputs.

11.3 GPIO Control

Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in Section 24.0, "Runtime Register," on page 213 section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. Bit[0] of each GPIO Configuration Register determines the port direction, bit[1] determines the signal polarity, and bit[7] determines the output driver type select. The GPIO configuration register Output Type select bit[7] applies to GPIO functions and the nSMI Alternate functions.

TABLE 16-3: WDT OPERATION FOLLOWING VCC_POR OR WDT2_CTL WRITING

WDT2_CTL	VCC_PORB	RST_WDT2B	Counter Reset	Condition
x	0	x	Yes	Power On
0	1	1	No	State after VCC_PORB. Counter starts Counting
0->1	1	1	Yes	Write 1 to WDT2_CTL. Counter reset and starts counting.
1->0	1	1	No	Write 0 to WDT2_CTL. No affect - counter running.
x	1	0	Yes	Counter timeout under normal conditions.

16.2 Voltage Scaling and Reset Generator Tolerances

The 5V supply is scaled internally. The input resistance is 20kohms (min). The voltage trip point is 4.45V (nominal) with a tolerance of ±0.15V (range: 4.3V-4.6V).

For the 3.3V VTR and 3.3V supplies, the voltage trip point is 2.8V (nominal) with a tolerance of ±0.1V (range: 2.7V-2.9V).

Refer to FIGURE 16-1: on page 102.

If a power failure occurs and the Power Supply should be in the ON state, the Power Failure Recovery logic will assert the PB_OUT# pin active low for a minimum pulse width of 0.5sec when VTR powers on. If the Power Supply should remain off, the Power Failure Recovery logic will have no effect on the PB_OUT# pin. The following table defines the possible states of PB_OUT# after a power failure for each configuration of the APF bits.

TABLE 18-3: DEFINITION OF APF BITS

APF[1:0]	Definition of APF Bits	AFTERG3 Bit (Located in ICH)	PB_OUT#
00 11	Power Supply OFF	1	———
01	Power Supply ON	1	⊓
10	Power Supply set to Previous State (ON)	1	⊓
10	Power Supply set to Previous State (OFF)	1	———

Note: It is a requirement that the AFTERG3 bit located in the ICH controller be programmed to 1 for this AC Recovery logic to be used.

18.3.1 PB_OUT# AND PS_ON#

The PB_OUT# and PS_ON# signals are used to control the state of the power supply.

The PB_OUT# signal will be asserted low if the PB_IN# is asserted and enabled, if the KB_IN# is asserted and enabled, or if recovering from a power failure and the power supply should be turned on. Refer to Figure 18-1. The following is a summary of these signals:

1. If the PB_IN# signal is enabled and asserted low, the PB_OUT# signal should be held low for as long as the PB_IN# signal is held low.
2. If the internal KB_PB_STS# signal (see Figure 14) is asserted low, the PB_OUT# signal is held low for as long as the KB_PB_STS# signal is held low.
3. If returning from a power failure and the power supply need to be turned on, a minimum of a ~0.5sec pulse is asserted on the PB_OUT# pin.

Note: This pulse width is less than 4 seconds, since a 4 second pulse width signifies a power button override event.

The PS_ON# signal is the inverse of the SLP_Sx# input signal. This signal goes directly to the Power Supply to turn the supply on or off.

The SCH#11X indirectly controls the PS_ON# signal by asserting the PB_OUT#. PB_OUT# will be interpreted by an external device (i.e., ICH controller), which will use this information to control the SLP_Sx# signal.

Note: Two modes have been added to save the state of the PS_ON# pin in the event of a power failure. This allows the system to recover from a power failure. See Section 18.3, "A/C Power Failure Recovery Control," on page 109.

TABLE 20-2: DESCRIPTION OF SECURITY KEY CONTROL (SKC) REGISTER BITS[2:1]

Bit[2] (Write-Lock)	Bit[1] (Read-Lock)	Description
0	0	Security Key Bytes[31:0] are read/write registers
0	1	Security Key Bytes[31:0] are Write-Only registers
1	0	Security Key Bytes[31:0] are Read-Only registers
1	1	Security Key Bytes[31:0] are not accessible. All reads/write access is denied.

Note: When Bit[1] (Read-Lock) is '1' all reads to this register block will return 00h.

- As an added layer of protection, bit [0] SKC Register Lock bit has been added to the Security Key Control Register. This lock bit is used to block write access to the Write-Lock and Read-Lock bits defined in the table above. Once this bit is set it can only be cleared by a VTR POR, VCC POR, and PCI Reset.

FIGURE 21-3: INTERRUPT CONTROL

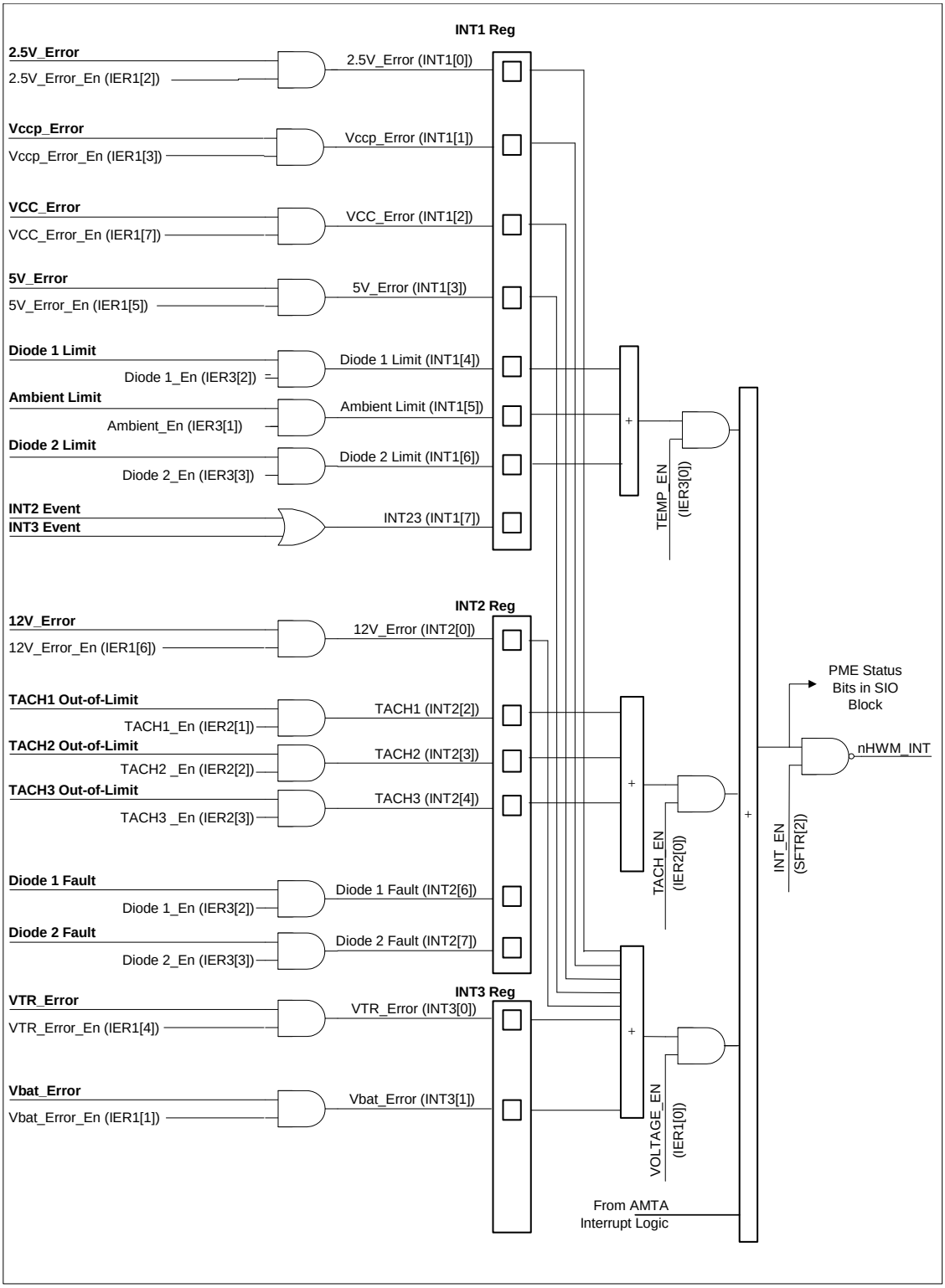
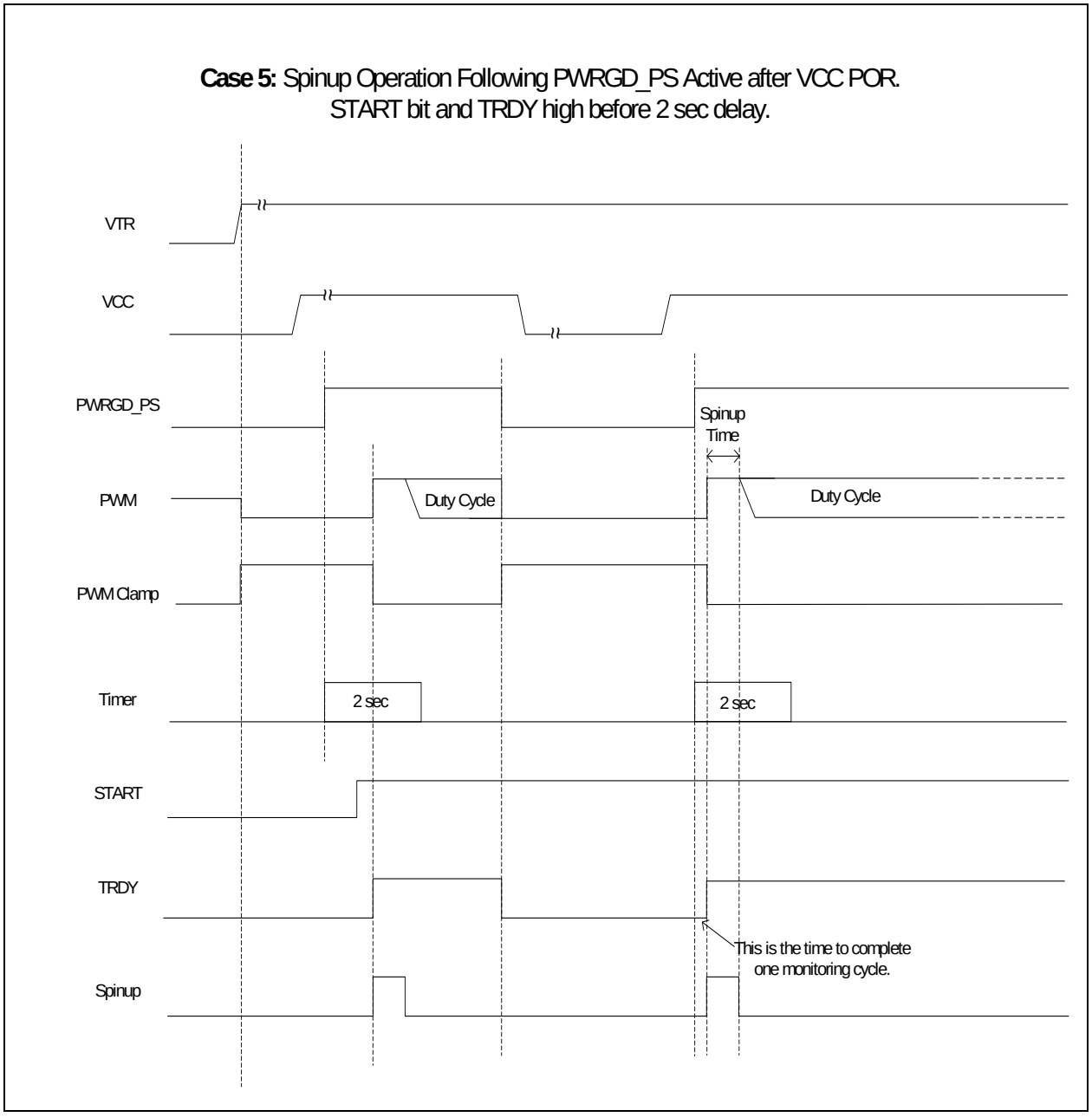


FIGURE 21-12: CASE 5 SPINUP OPERATION



21.13.5 ACTIVE MINIMUM TEMPERATURE ADJUSTMENT (AMTA)

The AMTA operation in the SCH322x consists of a “Top Temperature” register (for each zone) that defines the upper bound of the operating temperature for the zone. If the temperature exceeds this value, the minimum temperature (Low Temp Limit) for the zone is adjusted down. This keeps the zone operating in the lower portion of the temperature range of the fan control function (PWM Duty Cycle vs. Temperature), thereby limiting fan noise by preventing the fan from going to the higher PWM duty cycles.

21.13.5.1 Adjusting Minimum Temperature Based on Top Temperature

This describes the option for adjusting the minimum temperature based on the Top Temperature.

The AMTA option automatically adjusts the preprogrammed value for the minimum temperature and shifts the temperature range for the autofan algorithm to better suit the environment of the system, that is, to bias the operating range of the autofan algorithm toward the low end of the temperature range.

It uses a programmed value for the “Top temperature” for the zone to shift the temperature range of the autofan algorithm, and therefore the speed of the fan, toward the middle of the fan control function (PWM Duty Cycle vs. Temperature). This feature will effectively prevent the fans from going on full, thereby limiting the noise produced by the fans.

The value of the Top temperature for each zone can be programmed to be near the center of the temperature range for the zone, or near the maximum as defined by the low temp limit plus range. The implementation of the AMTA feature is defined as follows:

This feature can be individually enabled to operate for each zone. Each zone has a separate enable bit for this feature (register 0B7h). Note that if the piecewise linear fan function is used, the minimum temperature for the zone (Zone x Low Temp Limit register) is shifted down, which will result in each segment being shifted down.

This feature adjusts the minimum temperature for each zone for the autofan algorithm based on the current temperature reading for the zone exceeding the Top temperature.

When the current temperature for the zone exceeds the Top temperature for the zone, the minimum temperature value is reloaded with the value of the minimum temperature limit minus a programmable temperature adjustment value for the zone, as programmed in the Min Temp Adjust registers. The temperature adjustment value is programmable for each zone.

The zone must exceed the limits set in the associated Top Temp Zone [3:1] register for two successive monitoring cycles in order for the minimum temperature value to be adjusted (and for the associated status bit to be set).

The new minimum temperature value is loaded into the low temp limit register for each zone (Zone x Low Temp Limit). This will cause the temperature range of the autofan algorithm to be biased down in temperature.

Note:	When the minimum temperature for the zone is adjusted, the autofan algorithm will operate with a new fan control function (PWM Duty Cycle vs. Temperature), which will result in a new PWM duty cycle value. The PWM will move to the new value smoothly, so there is little audible effect when the PWM Ramp rate control is enabled.

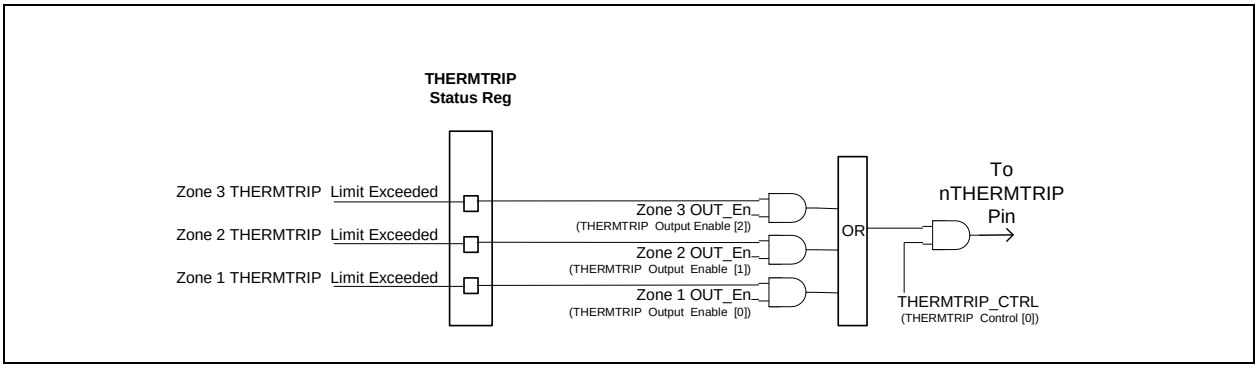
This process will repeat after a delay until the current temperature for the zone no longer exceeds the Top temperature for the zone.

Once the minimum temp value is adjusted, it will not adjust again until after a programmable time delay. The delay is programmed for each zone in the Min Temp Adjust Delay registers. The adjust times are as follows: 1, 2, 3, and 4 minutes.

Figure 8.5 illustrates the operation of the AMTA for one adjustment down in minimum temperature resulting from the temperature exceeding the Top temperature. The effect on the linear fan control function (PWM Duty Cycle vs. Temperature) is shown.

The following figures summarize the THERMTRIP operation in relation to the THERMTRIP status bits.

FIGURE 21-15: NTHERMTRIP OUTPUT OPERATION



21.14.2 FAN SPEED MONITORING

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the Fan Tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

The tachometers will operate in one of two modes:

- Mode 1: Standard tachometer reading mode. This mode is used when the fan is always powered when the duty cycle is greater than 00h.
- Mode 2: Enhanced tachometer reading mode. This mode is used when the PWM is pulsing the fan.

21.14.2.1 TACH Inputs

The tachometer inputs are implemented as digital input buffers with logic to filter out small glitches on the tach signal.

21.14.2.2 Selecting the Mode of Operation:

The mode is selected through the Mode Select bits located in the Tach Option register. This Mode Select bit is defined as follows:

- 0=Mode 1: Standard tachometer reading mode
- 1=Mode 2: Enhanced tachometer reading mode

Default Mode of Operation:

- Mode 1
- Slow interrupt disabled (Don't force FFFEh)
- Tach interrupt enabled via enable bit
- Tach Limit = FFFFh
- Tach readings updated once a second

21.14.2.3 Mode 1 – Always Monitoring

Mode 1 is the simple case. In this mode, the Fan is always powered when it is ‘ON’ and the fan tachometer output ALWAYS has a valid output. This mode is typically used if a linear DC Voltage control circuit drives the fan. In this mode, the fan tachometer simply counts the number of 90kHz pulses between the programmed number of edges (default = 5 edges). The fan tachometer reading registers are continuously updated.

The counter is used to determine the period of the Fan Tachometer input pulse. The counter starts counting on the first edge and continues counting until it detects the last edge or until it reaches FFFFh. If the programmed number of edges is detected on or before the counter reaches FFFFh, the reading register is updated with that count value. If the counter reaches FFFFh and no edges were detected a stalled fan event has occurred and the Tach Reading register will be set to FFFFh. If one or more edges are detected, but less than the programmed number of edges, a slow fan event has

This register contains the following bits:

Bit[0] Reserved

Bit[1] Monitoring Mode Select

0= Continuous Monitor Mode (default)

1= Cycle Monitor Mode

Bit[2] Interrupt (nHWM_INT Pin) Enable

0= Disables nHWM_INT pin output function (default)

1= Enables nHWM_INT pin output function

Bit[3] MCHP Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.Bit [4] MCHP Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated (TABLE 22). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

TABLE 22-15: AVG[2:0] BIT DECODER

SFTR[7:5]			Averages Per Reading		
AVG2	**AVG1**	**AVG0**	**REM Diode 1**	**REM Diode 2**	**Internal Diode**
0	0	0	128	128	8
0	0	1	16	16	1
0	1	X	16	16	16
1	X	X	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

22.2.26 REGISTER 7EH: INTERRUPT ENABLE 1 REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Eh	R/W	Interrupt Enable 1 (Voltages)	VCC	12V	5V	VTR	VCCP	2.5V	VBAT	VOLT	ECh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register is used to enable individual voltage error events to set the corresponding status bits in the interrupt status registers. This register also contains the group voltage enable bit (Bit[0] VOLT), which is used to enable voltage events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] Group interrupt Voltage Enable (VOLT)

0=Out-of-limit voltages do not affect the state of the nHWM_INT pin (default)

1=Enable out-of-limit voltages to make the nHWM_INT pin active low

Bit[1] VBAT Error Enable

Bit[2] 2.5V Error Enable

Bit[3] Vccp Error Enable

22.2.64 REGISTERS C4-C5, C9H: THERMTRIP TEMPERATURE LIMIT ZONE REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C4h	R/W	THERMTRIP Temp Limit ZONE 1 (Remote Diode 1)	7	6	5	4	3	2	1	0	7Fh
C9h	R/W	THERMTRIP Temp Limit ZONE 2 (Ambient)	7	6	5	4	3	2	1	0	7Fh
C5h	R/W	THERMTRIP Temp Limit ZONE 3 (Remote Diode 2)	7	6	5	4	3	2	1	0	7Fh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated THERMTRIP temperature limit (THERMTRIP Temp Limit ZONES 1-3). The THERMTRIP temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Temp Limit ZONE 1-3 registers represent the upper temperature limit for asserting nTHERMTRIP pin for each zone. These registers are defined as follows:

If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit ZONE 1-3 registers, the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERMTRIP Output Enable register).

Note: The zone must exceed the limits set in the associated THERMTRIP Temp Limit ZONE 1-3 register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

22.2.65 REGISTER CAH: THERMTRIP STATUS REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CAh	R/WC	THERMTRIP Status	RES	RES	RES	RES	RES	RD 2	RD 1	AMB	00h
Note:	Each bit in this register is cleared on a write of 1 if the event is not active.										

Note: This register is reset to its default value when the PWRGD_PS signal transitions high.

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to ‘1’ if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

22.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default).

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PME_STS5 Default = 0x00 on VTR POR	06 (R/WC)	PME Wake Status Register 5 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. If enabled, any set bit in this register asserts the nIO_PME pin. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_STS6 Default = 0x00 or 0x01 on VTR POR The default will be 0x01 if there is a LOW_BAT event under VBAT power only, 0x00 if the event does not occurs. Bit[0] will be set to ‘1’ on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. (SCH3227 or SCH3226, and STRAPOPT=0)	07 (R/WC)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. If enabled, any set bit in this register asserts the nIO_PME pin. Bit[0] LOW_BAT, Cleared by a write of ‘1’. When the battery is removed and replaced or the if the battery voltage drops below 1.2V under battery power, then the LOW_BAT PME status bit is set on VTR POR. When the battery voltage drops below 2.4 volts under VTR power (VCC=0) or under battery power only, the LOW_BAT PME status bit is set on VCC POR. The corresponding enable bit must be set to generate a PME. The low battery event is not a PME wakeup event. Bit[1] RESERVED. Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_STS (Wake on specific mouse click) Bit[5] SPEKEY_STS (Wake on specific key) Bit[6] PB_STS Bit[7] PFR_STS Power Failure Recovery Status The PME Status register is not affected by VCC POR, SOFT RESET or PCI RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Status Register has no effect.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SP34 Option Default = 0x44 on VTR POR (All except SCH3224)	0x13 (R/W)	Bit[0] Automatic Direction Control Select SP3 1=FC on 0=FC off Bits[1] Signal select SP3 1=nRTS control 0=nDTR control Bits[2] Polarity SP3 0= Drive low when enabled 1= Drive 1 when enabled Bits[3] RESERVED Bit[4] Automatic Direction Control Select SP4 1=FC on 0=FC off Bits[5] Signal select SP4 1=nRTS control 0=nDTR control Bits[6] Polarity SP4 0= Drive low when enabled 1= Drive 1 when enabled Bits[7] RESERVED
SMI_STS1 Default = 0x02, or 0x03 On VTR POR. The default will be 0x03 if there is a LOW_BAT event under VBAT power only, or 0x02 if this event does not occur. Bit 0 will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. Bit 1 is set to '1' on VCC POR, VTR POR, PCI Reset and soft reset.	14 Bits[0] are R/WC. Bits[1:4,7] are RO.	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source except as shown. Bit[0] LOW_BAT. Cleared by a write of '1'. When the battery is removed and replaced or if the battery voltage drops below 1.2V (nominal) under battery power only (VBAT POR), then the LOW_BAT SMI status bit is set on VTR POR. When the battery voltage drops below 2.4 volts (nominal) under VTR power (VCC=0) or under battery power only, the LOW_BAT SMI status bit is set on VCC POR. Bit[1] PINT. The parallel port interrupt defaults to '1' when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[2] U2INT Bit[3] U1INT Bit[4] FINT Bit[5] Reserved Bit[6] Reserved Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	15 (R/W) Bits[0,1] are RO Bits[2] is Read-Clear.	SMI Status Register 2 This register is used to read the status of the SMI inputs. Bit[0] MINT. Cleared at source. Bit[1] KINT. Cleared at source. Bit[2] IRINT. This bit is set by a transition on the IR pin (IRRX). Cleared by a read of this register. Bit[3] Reserved Bit[4] SPEMSE_STS (Wake on specific mouse click) - Cleared by writing a '1' Bit[7:5] Reserved

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP2 Default = 0x00 on VTR POR	4C (R/W)	General Purpose I/O Data Register 2 Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] GP27
GP3 Default = 0x00 on VTR POR	4D (R/W)	General Purpose I\O Data Register 3 Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] Reserved Bit[6] GP36 Bit[7] GP37
GP4 Default = 0xF0 on VTR POR	4E (R/W)	General Purpose I/O Data Register 4 Bit[0] GP40 Bit[1] Reserved Bit[2] GP42 Bit[3] Reserved Bit[4] GP44 Bit[5] GP45 Bit[6] GP46 Bit[7] GP47
GP5 Default = 0x00 on VTR POR	4F (R/W)	General Purpose I/O Data Register 5 Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57
GP6 Default = 0x00 on VTR POR	50 (R/W)	General Purpose I/O Data Register 6 Bit[0] GP60 Bit[1] GP61 Bit[2] GP62 Bit[3] GP63 Bit[4] GP64 Bit[5] GP65 Bit[6] GP66 Bit[7] GP67
N/A	51 (R)	Bits[7:0] Reserved – reads return 0

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP64 Default = 0x01 on VTR POR (SCH3224)	56 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP64 Default = 0x01 on VTR POR (All except SCH3224)	56 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=RXD4 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP65 Default = 0x01 on VTR POR (SCH3224)	57 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP65 Default = 0x01 on VTR POR (All except SCH3224)	57 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=TXD4 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP66 Default = 0x01 on VTR POR (SCH3224)	58 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP66 Default = 0x01 on VTR POR (All except SCH3224)	58 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDSR4 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP67 Default = 0x01 on VTR POR (SCH3224)	59 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bits[6:2] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP67 Default = 0x01 on VTR POR (All except SCH3224)	59 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nRTS4 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
TEST Default = 0x00 on VBAT POR	5A (R)	Bits[0:1,5] MCHP Reserved bit. Must be written as a '0'. Bits[2:4,6:7] Reserved Read only.
DBLCLICK Default = 0x0C on VBAT POR	5B Bits [5:0] are R/W when Mouse_Specific_ Wake register- Bit [7] is '0' Bits [5:0] are Read Only when Mouse_Specific_ Wake register- Bit [7] is '1'	Double Click for Specific Wake on Mouse Select Register The DBLCLICK contains a numeric value that determines the time interval used to check for a double mouse click. DBLCLICK is the time interval between mouse clicks. For example, if DBLCLICK is set to 0.5 seconds, you have one half second to click twice for a double-click. Bit[0:5] This field contains a six bit weighted sum value from 0 to 0x3Fh which provides a double click interval between 0.0859375 and 5.5 seconds. Each incremental digit has a weight of 0.0859375 seconds. Bit[6] Reserved - returns zero when read Bit[7] Spinup delay 1= zero delay for spinup following VTR POR 0 = spinup delay by 2 seconds (default)
Mouse_Specific_ Wake Default = 00h on VBAT POR Default = 0xxxxxxxb on VTR POR, VCC POR, and PCI Reset Note: The 'x' indicates bit is not affected by reset	5C R/W when Bit [7] is '0' Read Only when Bit [7] is '1'	Specific Wake on Mouse Click Control Register Bit[0:1] MCHP Reserved bit. Must be written as a '0'. Bits[4:2] SPESME SELECT. These bits select which mouse event is/are routed to trigger a PME wake event. 000 = Any button click or any movement (left/right/middle) 001 = One click of left button. 010 = One click of right button. 011 = Any one click of left/right/middle button. 100 = Reserved 101 = Two times click of left button. 110 = Two times click of right button. 111 = Reserved Bit[5] Reserved. Read only zero. Bit[6] KB_MSE_SWAP. This bit swaps the Keyboard and Mouse Port interfaces. 0 = The Keyboard and Mouse Ports are not swapped. 1 = The Keyboard and Mouse Ports are swapped. Bit [7] Mouse_Specific_ Wake Lock (Note) (This bit is Reset on a VBAT POR, VTR POR, VCC POR, and PCI Reset) 0 = Mouse_Specific_ Wake, and DBLCLICK Registers are Read/Write. 1 = Mouse_Specific_ Wake, and DBLCLICK Registers are Read Only.
LED1 Default = 0x00 on VTR POR	5D (R/W)	LED1 Bit[1:0] LED1 Control 00=off 01=blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved

26.3 Capacitance Values for Pins

The input and output capacitance applies to both the Super I/O Block and the Hardware Monitoring Block digital pins.

TABLE 26-2: CAPACITANCE T_A = 25; FC = 1MHZ; V_{CC} = 3.3V ±10%

Limits						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Test Condition**
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

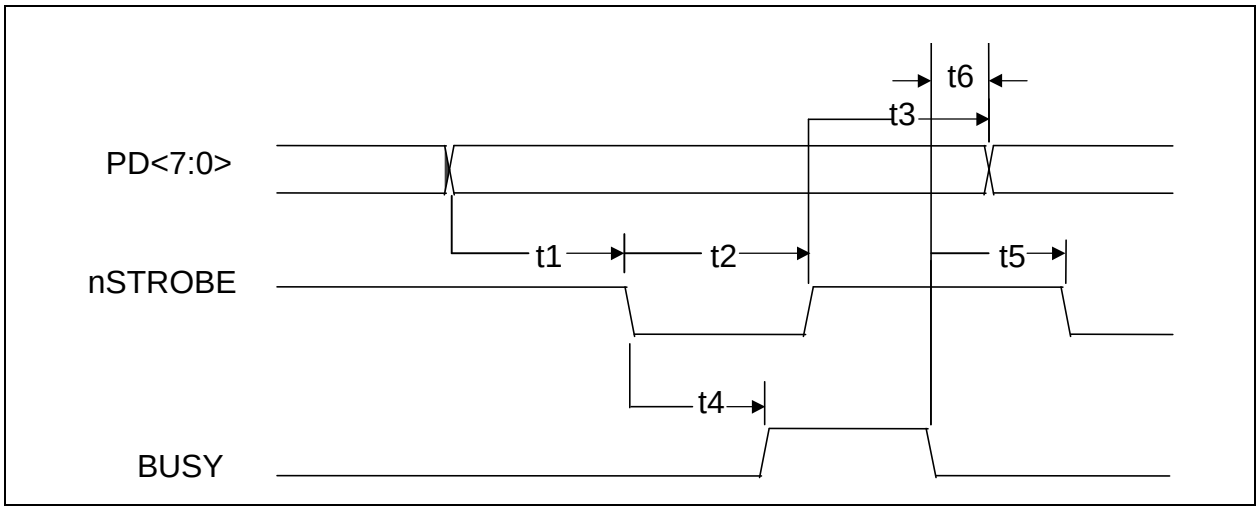
Note: The input capacitance of a port is measured at the connector pins.

26.4 Reset Generators

TABLE 26-3: RESET GENERATORS

Supply	Trip Point	Tolerance
3.3V, 3.3V VTR	2.8V	±100 mV
5.0V	4.45V	±150mV

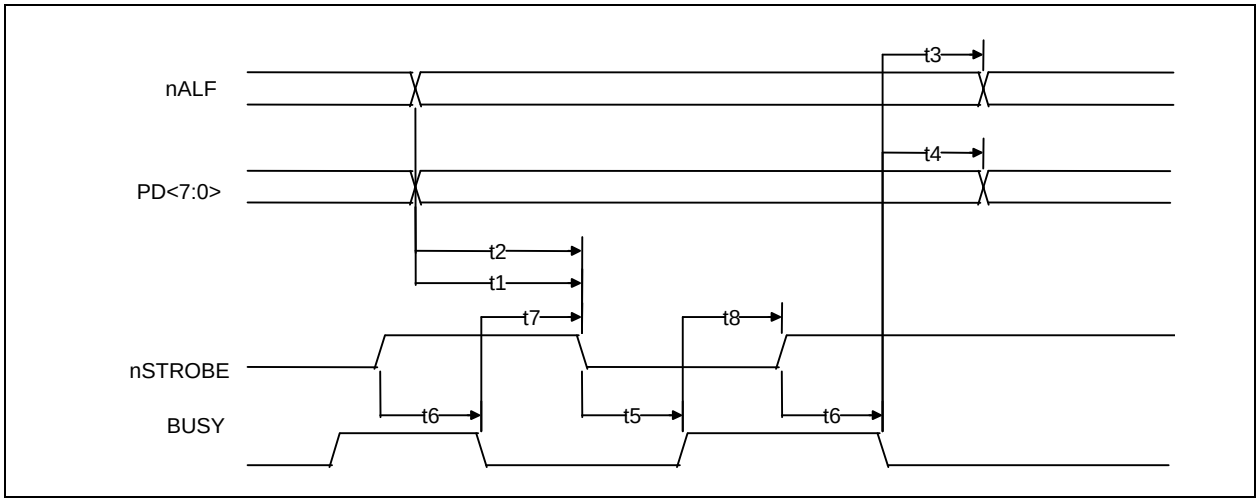
FIGURE 27-16: PARALLEL PORT FIFO TIMING



Name	Description	MIN	TYP	MAX	Units
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (See Note 27-3)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (See Note 27-3)	80			ns

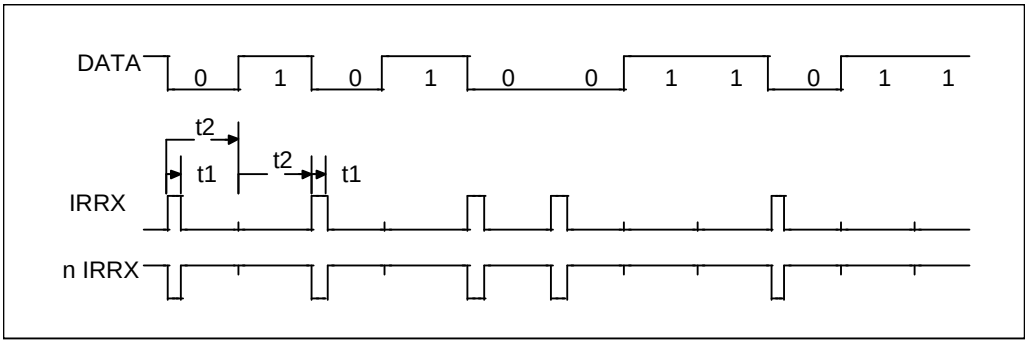
Note 27-3 The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

FIGURE 27-17: ECP PARALLEL PORT FORWARD TIMING



27.5 IR Timing

FIGURE 27-19: IRDA RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	-	XX	-	[XX]
Device	Temperature Range		Package		Tape and Reel Option

Device:	SCH3227/SCH3226/SCH3224/SCH3222
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)
Package:	SZ = 144-pin WFBGA (SCH3227) SY = 100-pin WFBGA (SCH3226. SCH3224) SX = 84-pin WFBGA (SCH3222)
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel (Note 1)

Examples:

a) SCH3227-SZ
Commercial temperature, 144-pin WFBGA, Tray

b) SCH3227I-SZ-TR
Industrial temperature, 144-pin WFBGA, Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.