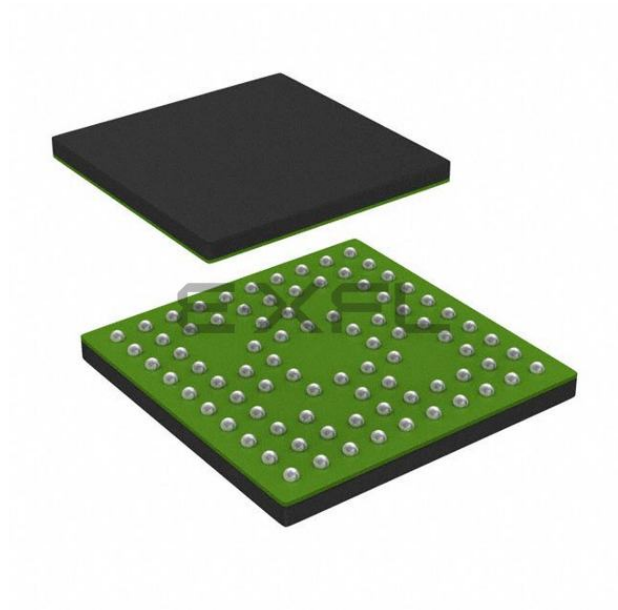

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Product Status	Active
Applications	I/O Controller
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Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	23
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-WFBGA
Supplier Device Package	84-WFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3222i-sx

2.0 PIN LAYOUTS

2.1 SCH322x Pin Layout Summary

FIGURE 2-1: SCH3227 PIN DIAGRAM

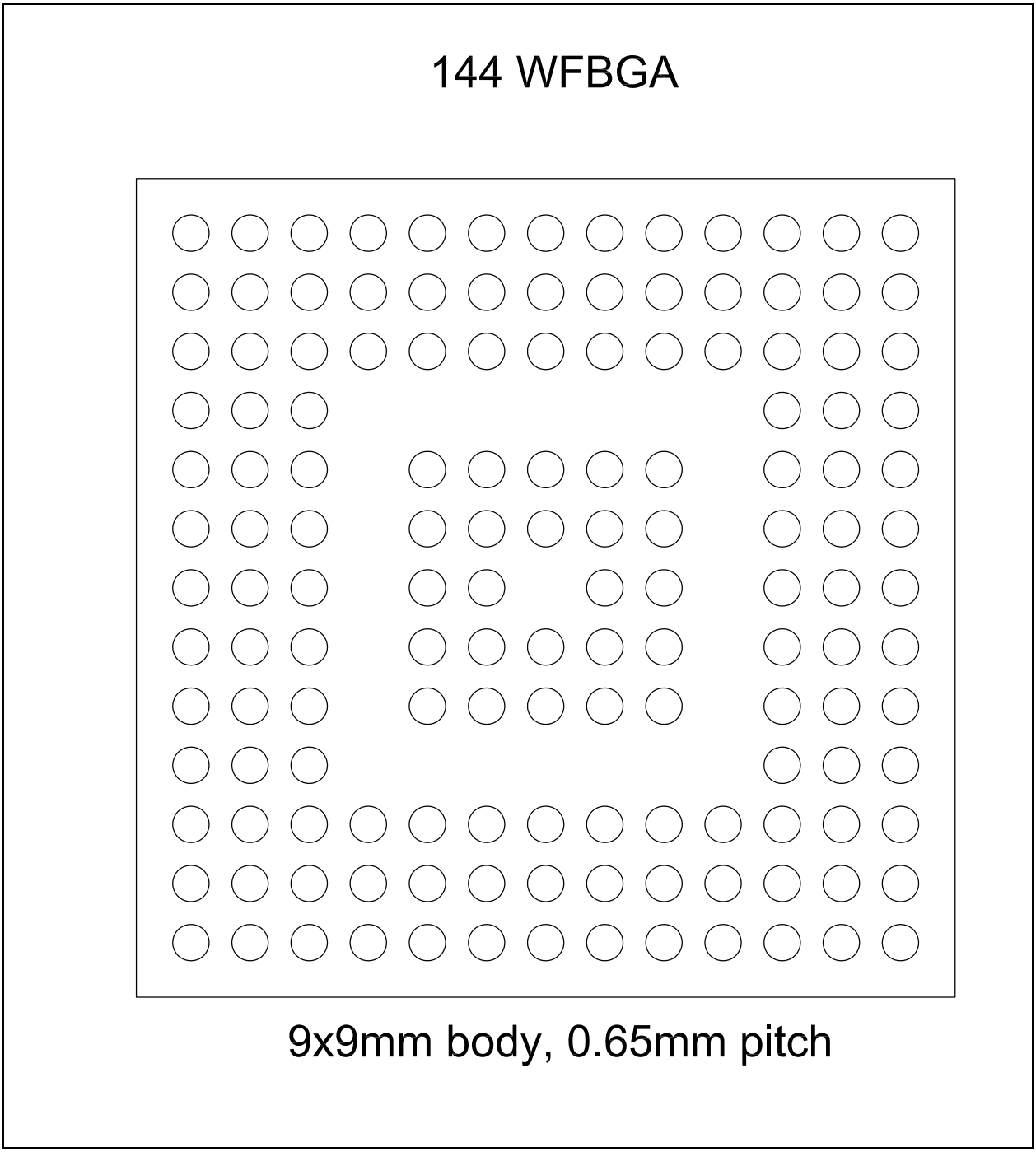


TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
2-12	nPCIRST1 / GP45	PCI Reset output 1 GPIO with Schmitt trigger input	nPCIRST1	GP45	NO GATE	(O8/OD8) / (IS/O8/OD8)
2-12	nIDE_RSTDRV / GP44	IDE Reset output GPIO with Schmitt trigger input	nIDE_RSTDRV	GP44	NO GATE	(O4/OD4) / (IS/O4/OD4)
GLUE LOGIC						
	PB_IN#	Power Button In is used to detect a power button event		PB_IN#	NO GATE	I
2-9	SLP_SX#	Sx Sleep State Input Pin.		SLP_SX#	NO GATE	I
	PB_OUT#	Power Button Out		PB_OUT#	NO GATE	O8
	PS_ON#	Power supply On		PS_ON#	NO GATE	O12
MISCELLANEOUS PINS						
	GP42/ nIO_PME	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in either S3 or S5 and below.		GP42/ nIO_PME	NO GATE	(I/O12/OD12) /(O12/OD12)
2-8, 2-9	GP60 /nLED1 /WDT	General Purpose I/O /nLED1 Watchdog Timer Output		GP60 /nLED1 /WDT	NO GATE	(I/O12/OD12) /(O12/OD12) /(O12/OD12)
	nFPRST / GP30	Front Panel Reset / General Purpose IO		nFPRST / GP30	NO GATE	ISPU_400 / (I/O4/OD4)
	PWRGD_PS	Power Good Input from Power Supply		PWRGD_PS	NO GATE	ISPU_400
	PWRGD_OUT	Power Good Output – Open Drain		PWRGD_OUT	NO GATE	OD8
	nRSMRST	Resume Reset Output		nRSMRST	NO GATE	OD24
2-8, 2-9	GP61 /nLED2 / CLKO	General Purpose I/O /nLED2 / Programmable Clock Output		GP61 /nLED2 / CLKO	NO GATE	(I/O12/OD12) / (O12/OD12) / (O12/OD12)
2-9	GP27 /nIO_SMI /P17	General Purpose I/O /System Mgt. Interrupt /8042 P17 I/O	GP27 /nIO_SMI /P17	GP27	/ HI-Z	(I/O12/OD12) /(O12/OD12) /(I/O12/OD12)
HARDWARE MONITORING BLOCK						
	nHWM_INT	Interrupt output for Hardware monitor		nHWM_INT		OD8
2-10	+5V_IN	Analog input for +5V	HVTR			I_{AN}
2-10	+2.5_IN	Analog input for +2.5V	HVTR			I_{AN}
2-10	VCCP_IN	Analog input for +Vccp (processor voltage: 1.5 V nominal).	HVTR			I_{AN}
2-10	+12V_IN	Analog input for +12V	HVTR			I_{AN}

If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Programming High Speed Serial Port baud Rates

The SCH322x family of devices supports serial ports with speeds up to 1.5Mb/s. Changing the serial ports baud rates between standard speeds (115k baud and slower) during runtime is possible with standard drivers. In order to change baud rates to high speed (230k, 460k, 921k and 1.5M bauds) on the SCH322x devices during runtime, registers in both Configuration space and Runtime space must be programmed.

Note that this applies only if the application requires a serial port baud rate to change during runtime. Standard windows drivers could be used to select the specific high speed rate if it will remain unchanged during runtime Table 6-4 on page 45 shows the baud rates possible.

6.1.12 EFFECT OF THE RESET ON THE REGISTER FILE

The Reset Function (details the effect of the Reset input on each of the registers of the Serial Port.

6.1.13 FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = “1”, IER bit 0 = “1”), RCVR interrupts occur as follows:

- The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
- The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
- The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

- A FIFO timeout interrupt occurs if all the following conditions exist:

At least one character is in the FIFO.

The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).

The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12-bit character.

- Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
- When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
- When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = “1”, IER bit 1 = “1”), XMIT interrupts occur as follows:

- The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
- The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

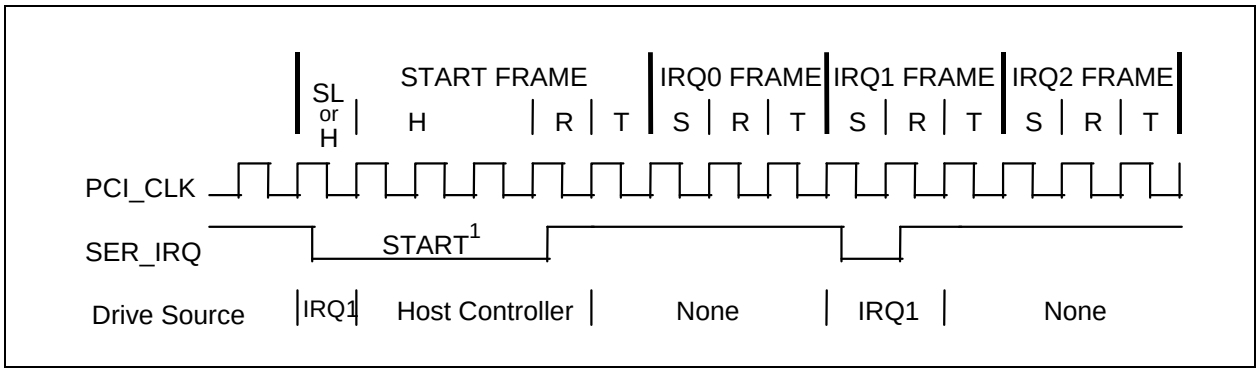
Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

9.0 SERIAL IRQ

The SCH3227/SCH3226/SCH3224/SCH3222 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0.

9.1 Timing Diagrams For SER_IRQ Cycle

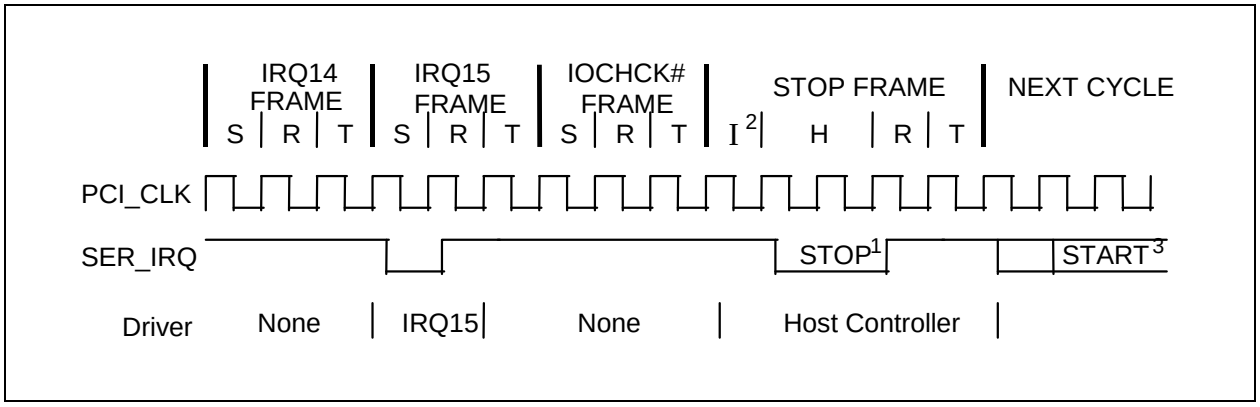
a) Start Frame timing with source sampled a low pulse on IRQ1



Note 1: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample

2: Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

b) Stop Frame Timing with Host using 17 SER_IRQ sampling period



Note 1: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle

2: The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

3: There may be none, one or more Idle states during the Stop Frame.

4: Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.

The basic GPIO configuration options are summarized in Table 11-3, "GPIO Configuration Option".

TABLE 11-3: GPIO CONFIGURATION OPTION

Selected Function	Direction Bit	Polarity Bit	Description
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

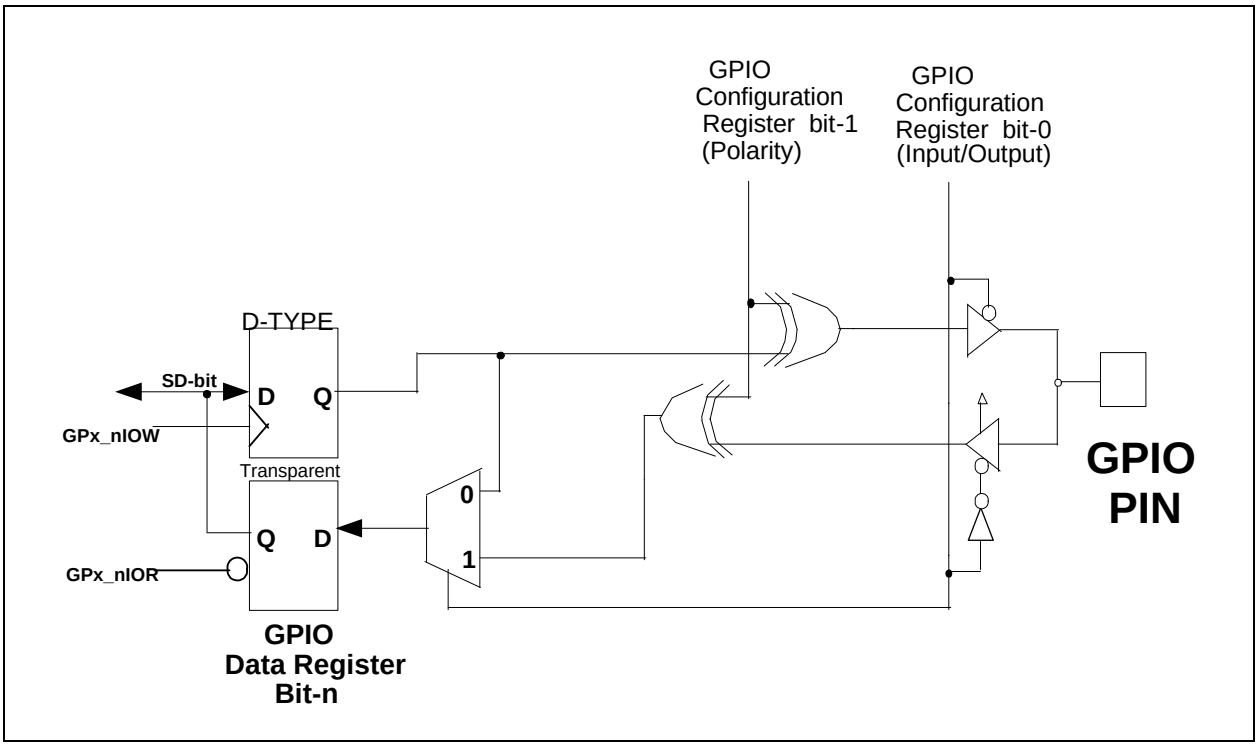
11.4 GPIO Operation

The operation of the GPIO ports is illustrated in Figure 11-1.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 11-4).

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 11-4). When the GPIO is programmed as an output, the pin is excluded from the PME and SMI logic.

FIGURE 11-1: GPIO FUNCTION ILLUSTRATION



Note: Figure 11-1 is for illustration purposes only and is not intended to suggest specific implementation details.

12.0 SYSTEM MANAGEMENT INTERRUPT (SMI)

The SCH322x implements a “group” nIO_SMI output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from each of the functional blocks in the chip and many of the GPIOs and the Fan tachometer pins. The GP27/nIO_SMI/P17 pin, when selected for the nIO_SMI function, can be programmed to be active high or active low via the polarity bit in the GP27 register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the GP27 register. The nIO_SMI pin function defaults to active low, open-drain output.

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1 to 4. The nSMI output is then enabled onto the group nIO_SMI output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2. The internal SMI can also be enabled onto the nIO_PME pin. Bit[5] of the SMI Enable Register 2 (SMI_EN2) is used to enable the SMI output onto the nIO_PME pin (GP42). This bit will enable the internal SMI output into the PME logic through the DEVINT_STS bit in PME_STS3.

An example logic equation for the nSMI output for SMI registers 1 and 2 is as follows:

nSMI = (EN_PINT and IRQ_PINT) or (EN_U2INT and IRQ_U2INT) or (EN_U1INT and IRQ_U1INT) or (EN_FINT and IRQ_FINT) or (EN_MINT and IRQ_MINT) or (EN_KINT and IRQ_KINT) or (EN_IRINT and IRQ_IRINT) or (ENP12 and IRQ_P12) or (SPEMSE_EN and SPEMSE_STS)

Note:	The prefixes EN and IRQ are used above to indicate SMI enable bit and SMI status bit respectively.

12.1 SMI Registers

The SMI event bits for the GPIOs and the Fan tachometer events are located in the SMI status and Enable registers 3-5. The polarity of the edge used to set the status bit and generate an SMI is controlled by the polarity bit of the control registers. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding SMI status bit. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for these events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI registers are accessed at an offset from PME_BLK (see Section 24.0, "Runtime Register," on page 213 for more information).

The SMI event bits for the super I/O devices are located in the SMI status and enable register 1 and 2. All of these status bits are cleared at the source except for IRINT, which is cleared by a read of the SMI_STS2 register; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See the Section 24.0 for the definition of these registers.

If the SMI enable bit (and other associated enable bits) were set prior to VCC going away, then the low battery event will generate an SMI when VCC becomes active again.

19.2.3 UNDER VCC POWER

The LOW_BAT PME and SMI bits are not set when the part is under VCC power. They are only set upon a VCC POR. See Section 19.2.2, "Under VTR Power".

21.13.3 PWM FAN SPEED CONTROL

The following description applies to PWM1, PWM2, and PWM3.

Note: The PWM output pins are held low when VCC=0. The PWM pins will be forced to “spinup” when PWRGD_PS goes active. See “Spin Up” on page 137.

The PWM pin reflects a duty cycle that is determined based on 256 PWM duty cycle intervals. The minimum duty cycle is “off”, when the pin is low, or “full on” when the pin is high for 255 intervals and low for 1 interval. The INVERT bit (bit 4 of the PWMx Configuration registers at 80h-82h) can be used to invert the PWM output, however, the default operation (following a VCC POR) of the part is based on the PWM pin active high to turn the fans “on”. When the INVERT bit is set, as long as power is not removed from the part, the inversion of the pin will apply thereafter.

When describing the operation of the PWMs, the terms “Full on” and “100% duty cycle” means that the PWM output will be high for 255 clocks and low for 1 clock (INVERT bit = 0). The exception to this is during fan spin-up when the PWM pin will be forced high for the duration of the spin-up time.

The SCH322x can control each of the PWM outputs in one of two modes:

- Manual Fan Control Operating Mode: software controls the speed of the fans by directly programming the PWM duty cycle.
- Auto Fan Control Mode: the device automatically adjusts the duty cycle of the PWM outputs based on temperature, according to programmed parameters.

These modes are described in sections that follow.

21.13.3.1 Manual Fan Control Operating Mode (Test Mode)

When operating in Manual Fan Control Operating Mode, software controls the speed of the fans by directly programming the PWM duty cycle. The operation of the fans can be monitored based on reading the temperature and tachometer reading registers and/or by polling the interrupt status registers. The SCH322x offers the option of generating an interrupt indicated by the nHWM_INT signal.

To control the PWM outputs in manual mode:

- To set the mode to operate in manual mode, write ‘111’ to bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWMx Configuration.
- The speed of the fan is controlled by the duty cycle set for that PWM output. The duty cycle must be programmed in Registers 30h-32h: Current PWM Duty

To monitor the fans:

Fans equipped with Tachometer outputs can be monitored via the FANTACHx input pins. See Section 21.14.2, "Fan Speed Monitoring," on page 150.

If an out-of-limit condition occurs, the corresponding status bit will be set in the Interrupt Status registers. Setting this status bit will generate an interrupt signal on the nHWM_INT pin (if enabled). Software must handle the interrupt condition and modify the operation of the device accordingly. Software can evaluate the operation of the Fan Control device through the Temperature and Fan Tachometer Reading registers.

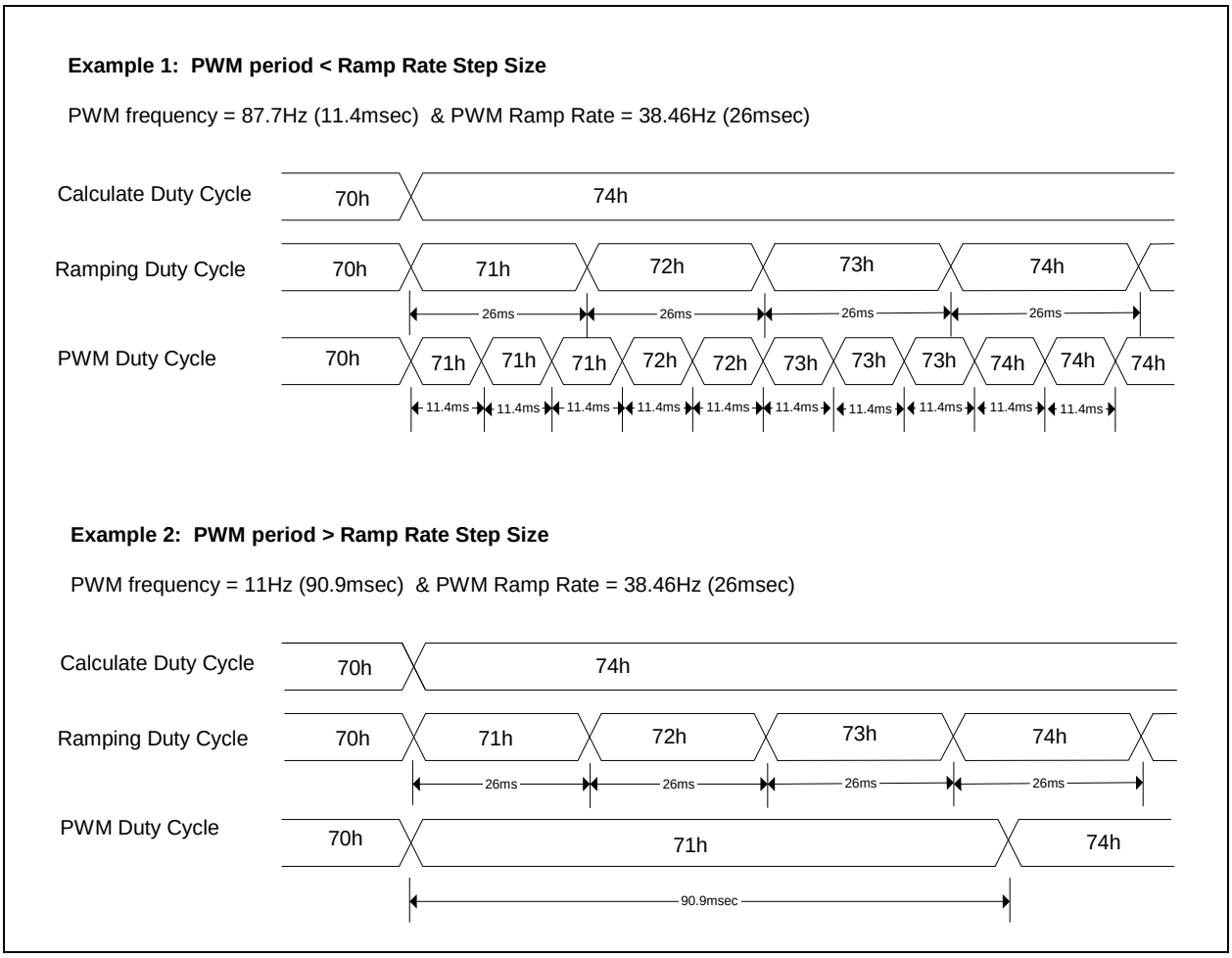
When in manual mode, the current PWM duty cycle registers can be written to adjust the speed of the fans, when the start bit is set. These registers are not writable when the lock bit is set.

Note: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

21.13.3.2 Auto Fan Control Operating Mode

The SCH322x implements automatic fan control. In Auto Fan Mode, this device automatically adjusts the PWM duty cycle of the PWM outputs, according to the flow chart on the following page (see FIGURE 21-4: Automatic Fan Control Flow Diagram on page 135).

FIGURE 21-7: ILLUSTRATION OF PWM RAMP RATE CONTROL



Note 1: The PWM Duty Cycle latches the Ramping Duty Cycle on the rising edge of the PWM output.

2: The calculated duty cycle, ramping duty cycle, and the PWM output duty cycle are asynchronous to each other, but are all synchronized to the internal 90kHz clock source.

It should be noted that the actual duty cycle on the pin is created by the PWM Ramp Rate Control block and latched on the rising edge of the PWM output. Therefore, the current PWM duty cycle may lag the PWM Calculated Duty Cycle.

21.13.4 OPERATION OF PWM PIN FOLLOWING A POWER CYCLE

This device has special features to control the level and operation of the PWM pin following a Power Cycle. These features are PWM Clamping and Forced Spinup.

21.13.4.1 PWM Clamp

The PWM pin has the option to be held low for 0 seconds or 2 seconds following a VCC POR. This feature is selectable by a Vbat powered register bit in the SIO Runtime Register block.

Bit[7] of the DBLCLICK register at offset 5Bh is used to select the 0 or 2 second option.

This bit is defined as follows:

- BIT[3] ZERO_SPINUP
  - 1 = zero delay for spin up
  - 0 = delay spinup by 2 seconds (default)

22.1 Undefined Registers

The registers shown in the table above are the defined registers in the part. Any reads to undefined registers always return 00h. Writes to undefined registers have no effect and do not return an error.

22.2 Defined Registers

22.2.1 REGISTER 10H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
10h	R/W	MCHP TEST	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

Setting the Lock bit has no effect on this registers

This register must not be written. Writing this register may produce unexpected results.

22.2.2 REGISTERS 20-24H, 99-9AH: VOLTAGE READING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
20h	R	2.5V Reading	7	6	5	4	3	2	1	0	N/A
21h	R	Vccp Reading	7	6	5	4	3	2	1	0	N/A
22h	R	VCC Reading	7	6	5	4	3	2	1	0	N/A
23h	R	+5V Reading	7	6	5	4	3	2	1	0	N/A
24h	R	+12V Reading	7	6	5	4	3	2	1	0	N/A
99h	R	VTR Reading	7	6	5	4	3	2	1	0	N/A
9Ah	R	Vbat Reading	7	6	5	4	3	2	1	0	N/A

The Voltage Reading registers reflect the current voltage of the voltage monitoring inputs. Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each register will read C0h, except for the Vbat input. Vbat is nominally a 3.0V input that is implemented on a +3.3V (nominal) analog input. Therefore, the nominal reading for Vbat is AEh.

Note: Vbat will only be monitored when the Vbat Monitoring Enable bit is set to '1'. Updating the Vbat register automatically clears the Vbat Monitoring Enable bit.

TABLE 22-2: VOLTAGE VS. REGISTER READING

Input	Nominal Voltage	Register Reading at Nominal Voltage	Maximum Voltage	Register Reading at Maximum Voltage	Minimum Voltage	Register Reading at Minimum Voltage
VTR	3.3V	C0h	4.38V	FFh	0V	00h
Vbat (Note 22-11)	3.0V	AEh	4.38V	FFh	0V	00h
5.0V	5.0V	C0h	6.64V	FFh	0V	00h
Vccp	1.5V	C0h	2.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

Note 22-11 Vbat is a nominal 3.0V input source that has been implemented on a 3.3V analog voltage monitoring input.

The Voltage Reading registers will be updated automatically by the device with a minimum frequency of 4Hz if the average bits located in the Special Function register at offset 7Ch are set to 001. These registers are read only – a write to these registers has no effect.

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

The Top Temperature Registers define the upper bound of the operating temperature for each zone. If the temperature of the zone exceeds this value, the minimum temperature for the zone can be configured to be adjusted down.

The Top Temperature registers are used as a comparison point for the AMTA feature, to determine if the Low Temp Limit register for a zone should be adjusted down. The Top temp register for a zone is not used if the AMTA feature is not enabled for the zone. The AMTA feature is enabled via the Tmin Adjust Enable register at 0B7h.

22.2.53 REGISTER B4H: MIN TEMP ADJUST TEMP RD1, RD2 (ZONES 1& 3)

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B4h	R/W	Min Temp Adjust Temp RD1, RD2 (Zones 1&3)	R1ATP1	R1ATP 0	R2ATP 1	R2ATP 0	RES	RES	RES	RES	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

Bits[7:4] are used to select the temperature adjustment values that are subtracted from the Zone Low temp limit for zones 1& 3. There is a 2-bit value for each of the remote zones that is used to program the value that is subtracted from the low temp limit temperature register when the temperature reading for the zone reaches the Top Temperature for the AMTA feature. The AMTA feature is enabled via the Tmin Adjust Enable register at B7h.

These bits are defined as follows: ZxATP[1:0]:

- 00= 2oC (default)
- 01= 4oC
- 10= 6oC
- 11= 8oC

Note: The Zones are hardwired to the sensors in the following manner:

- R1ATP[1:0] = Zone 1 = Remote Diode 1
- AMATP[1:0] = Zone 2 = Ambient
- R2ATP[1:0] = Zone 3 = Remote Diode 2

22.2.54 REGISTER B5H: MIN TEMP ADJUST TEMP AND DELAY AMB (ZONE 2)

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B5h	R/W	Min Temp Adjust Temp and Delay (Zone 2)	RES	RES	AMATP 1	AMATP 0	RES	RES	AMAD1	AMAD0	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

Bits[5:4] Min Temp Adjust for Ambient Temp Sensor (Zone 2)

See Register B4h: Min Temp Adjust Temp RD1, RD2 (Zones 1& 3) on page 188 for a definition of the Min Temp Adjust bits.

Bits[1:0] Min Temp Adjust Delay for Ambient Temp Sensor (Zone 2)

See Register B6h: Min Temp Adjust Delay RD1, RD2 (ZONE 1 & 3) Register on page 188 for a definition of the Min Temp Delay bits.

22.2.55 REGISTER B6H: MIN TEMP ADJUST DELAY RD1, RD2 (ZONE 1 & 3) REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B6h	R/W	Min Temp Adjust Temp and Delay RD1, RD2 (Zones 1 & 3)	R1 AD1	R1 AD0	R2 AD1	R2 AD0	RES	RES	RES	RES	00h

22.2.71 REGISTERS E2H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

22.2.72 REGISTERS E3H: MCHP TEST REGISTER

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

22.2.73 REGISTER E9-EEH: MCHP TEST REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
E9h	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EAh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EBh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
ECh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EDh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EEh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

These are MCHP Test Registers. Writing to these registers may cause unwanted results.

22.2.74 REGISTER FFH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
FFh	R	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an MCHP Test register.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SP34 Option Default = 0x44 on VTR POR (All except SCH3224)	0x13 (R/W)	Bit[0] Automatic Direction Control Select SP3 1=FC on 0=FC off Bits[1] Signal select SP3 1=nRTS control 0=nDTR control Bits[2] Polarity SP3 0= Drive low when enabled 1= Drive 1 when enabled Bits[3] RESERVED Bit[4] Automatic Direction Control Select SP4 1=FC on 0=FC off Bits[5] Signal select SP4 1=nRTS control 0=nDTR control Bits[6] Polarity SP4 0= Drive low when enabled 1= Drive 1 when enabled Bits[7] RESERVED
SMI_STS1 Default = 0x02, or 0x03 On VTR POR. The default will be 0x03 if there is a LOW_BAT event under VBAT power only, or 0x02 if this event does not occur. Bit 0 will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. Bit 1 is set to '1' on VCC POR, VTR POR, PCI Reset and soft reset.	14 Bits[0] are R/WC. Bits[1:4,7] are RO.	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source except as shown. Bit[0] LOW_BAT. Cleared by a write of '1'. When the battery is removed and replaced or if the battery voltage drops below 1.2V (nominal) under battery power only (VBAT POR), then the LOW_BAT SMI status bit is set on VTR POR. When the battery voltage drops below 2.4 volts (nominal) under VTR power (VCC=0) or under battery power only, the LOW_BAT SMI status bit is set on VCC POR. Bit[1] PINT. The parallel port interrupt defaults to '1' when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[2] U2INT Bit[3] U1INT Bit[4] FINT Bit[5] Reserved Bit[6] Reserved Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	15 (R/W) Bits[0,1] are RO Bits[2] is Read-Clear.	SMI Status Register 2 This register is used to read the status of the SMI inputs. Bit[0] MINT. Cleared at source. Bit[1] KINT. Cleared at source. Bit[2] IRINT. This bit is set by a transition on the IR pin (IRRX). Cleared by a read of this register. Bit[3] Reserved Bit[4] SPEMSE_STS (Wake on specific mouse click) - Cleared by writing a '1' Bit[7:5] Reserved

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP21 Default =0x8C on VTR POR	2C (R/W)	General Purpose I/O bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KDAT (Default) 10=Either Edge Triggered Interrupt Input 0 (Note 24-20) 01=Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull (Default) **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KDAT function, bit[0] should always be programmed to '0'. The KDAT function will not operate properly when bit[0] is set.
GP22 Default =0x8C on VTR POR	2D (R/W)	General Purpose I/O bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KCLK (Default) 10=Either Edge Triggered Interrupt Input 1 (Note 24-20) 01= Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KCLK function, bit[0] should always be programmed to '0'. The KCLK function will not operate properly when bit[0] is set.
UART5 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2E (R)	Bits[7:0] RESERVED
UART5 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2E (R)	UART FIFO Control Shadow 5 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
UART6 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2F (R)	Bits[7:0] RESERVED
UART6 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2F (R)	Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
Keyboard PWRBTN/SPEKEY (continued)		Bit [7] Keyboard PWRBTN/SPEKEY Lock (Note) (This bit is Reset on a Vbat POR, VTR POR, VCC POR, and PCI Reset) 0 = Keyboard PWRBTN/SPEKEY and Keyboard Scan Code Registers are Read/Write 1 = Keyboard PWRBTN/SPEKEY and Keyboard Scan Code Registers are Read Only **Note:** The following registers become Read-Only when Bit [7] is '1': • Keyboard Scan Code – Make Byte 1 at offset 5Fh • Keyboard Scan Code – Make Byte 2 at offset 60h • Keyboard Scan Code – Break Byte 1 at offset 61h • Keyboard Scan Code – Break Byte 2 at offset 62h • Keyboard Scan Code – Break Byte 3 at offset 63h • Keyboard PWRBTN/SPEKEY at offset 64h
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and PCI Reset	65 (R/W)	Watch-dog Timeout Bit[0] Reserved Bit[1] Reserved Bits[6:2] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and PCI Reset	66 (R/W)	Watch-dog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and PCI Reset	67 (R/W)	Watch-dog timer Configuration Bit[0] Reserved Bit[1] Keyboard Enable =1 WDT is reset upon a Keyboard interrupt. =0 WDT is not affected by Keyboard interrupts. Bit[2] Mouse Enable =1 WDT is reset upon a Mouse interrupt. =0 WDT is not affected by Mouse interrupts. Bit[3] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = IRQ2 (Note) 0001 = IRQ1 0000 = Disable **Note:** IRQ2 is used for generating SMI events via the serial IRQ's stream. The WDT should not be configured for IRQ2 if the IRQ2 slot is enabled for generating an SMI event.

26.3 Capacitance Values for Pins

The input and output capacitance applies to both the Super I/O Block and the Hardware Monitoring Block digital pins.

TABLE 26-2: CAPACITANCE T_A = 25; FC = 1MHZ; V_{CC} = 3.3V ±10%

Limits						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Test Condition**
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

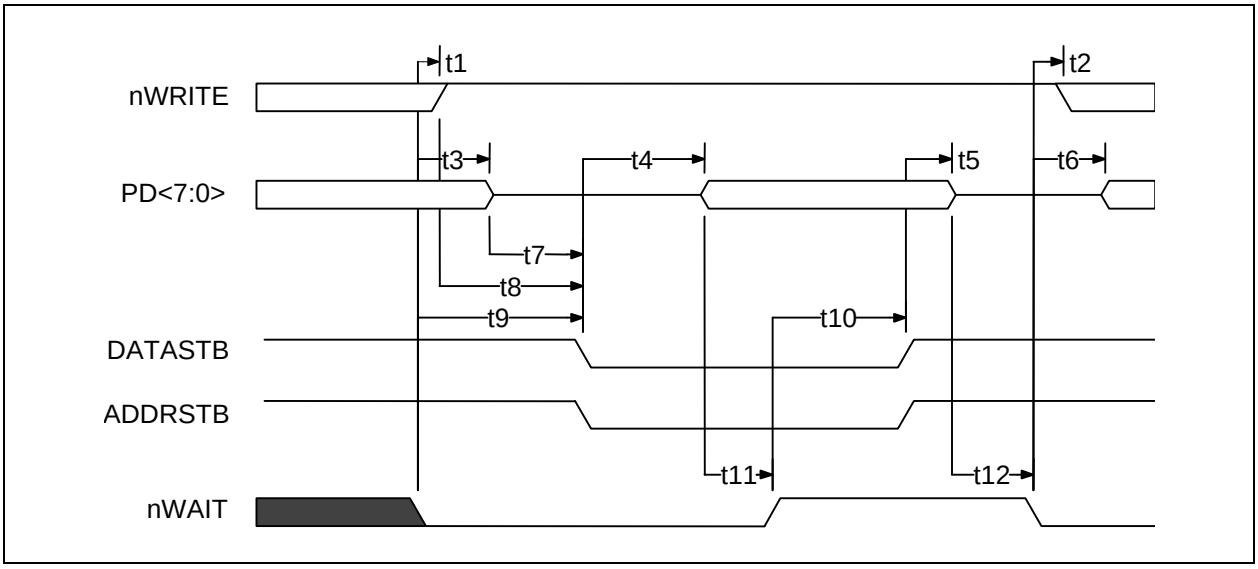
Note: The input capacitance of a port is measured at the connector pins.

26.4 Reset Generators

TABLE 26-3: RESET GENERATORS

Supply	Trip Point	Tolerance
3.3V, 3.3V VTR	2.8V	±100 mV
5.0V	4.45V	±150mV

FIGURE 27-13: EPP 1.9 DATA OR ADDRESS READ CYCLE

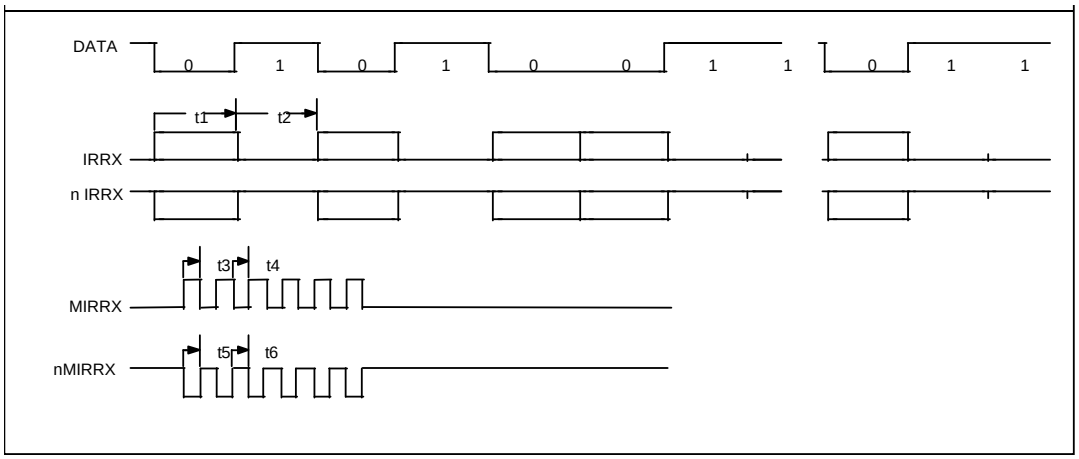


Name	Description	MIN	TYP	MAX	Units
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (Notes 1,2)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (Note 1)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			µs

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.

2: When not executing a write cycle, EPP nWRITE is inactive high.

FIGURE 27-21: AMPLITUDE SHIFT-KEYED IR RECEIVE TIMING



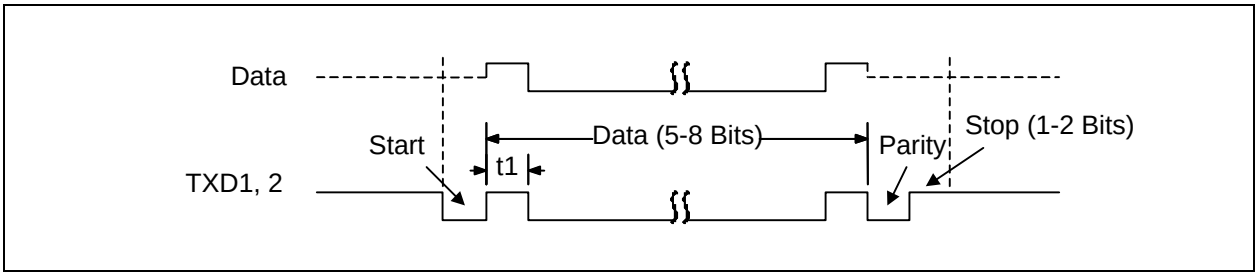
	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

27.7 UART Interface Timing

FIGURE 27-24: SERIAL PORT DATA

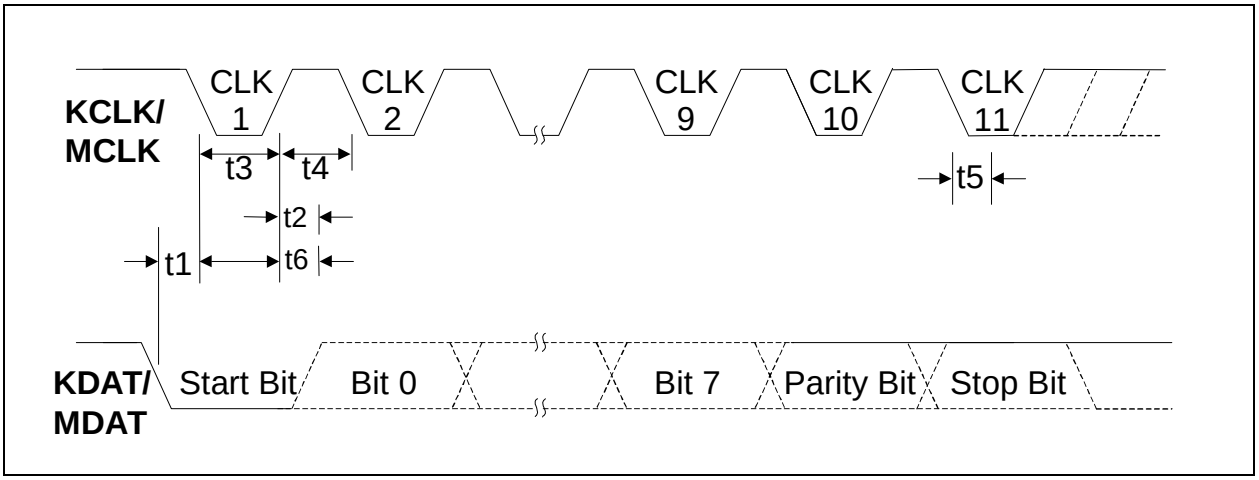


Name	Description	MIN	TYP	MAX	Units
t1	Serial Port Data Bit Time		t_{BR}[1]		nsec

t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

27.8 Keyboard/Mouse Interface Timing

FIGURE 27-25: KEYBOARD/MOUSE RECEIVE/SEND DATA TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Time from DATA transition to falling edge of CLOCK (Receive)	5		25	µsec
t2	Time from rising edge of CLOCK to DATA transition (Receive)	5		T4-5	µsec
t3	Duration of CLOCK inactive (Receive/Send)	30		50	µsec
t4	Duration of CLOCK active (Receive/Send)	30		50	µsec
t5	Time to keyboard inhibit after clock 11 to ensure the keyboard does not start another transmission (Receive)	>0		50	µsec
t6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	µsec

To put the chip in the first XNOR chain test mode, tie LAD0 and LFRAME# low. Then toggle PCI_RESET# from a low to a high state. Once the chip is put into XNOR chain test mode, LAD0 and LFRAME# become part of the chain.

To exit the SIO XNOR chain test mode tie LAD0 or LFRAME# high. Then toggle PCI_RESET# from a low to a high state. A VCC POR will also cause the XNOR chain test mode to be exited. To verify the test mode has been exited, observe the output at TXD1. Toggling any of the input pins in the chain should not cause its state to change.

Setup of Super I/O XNOR Chain

Warning: Ensure power supply is off during setup.

- Connect the VSS, the AVSS, HVSS pins to ground.
- Connect the VCC, the VTR, and HVTR pins to 3.3V.
- Connect an oscilloscope or voltmeter to TXD1.
- All other pins should be tied to ground.

Testing

1. Turn power on.
2. With LAD0 and LFRAME# low, bring PCI_RESET# high. The chip is now in XNOR chain test mode. At this point, all inputs to the first XNOR chain are low. The output, on TXD1 should also be low. Refer to INITIAL CONFIG on Table C-1.
3. Bring the first pin high. The output on TXD1 should go toggle. Refer to STEP ONE in Table C-1.
4. In descending pin order, bring each input high. The output should switch states each time an input is toggled. Continue until all inputs are high. The output on TXD1 should now be low. Refer to END CONFIG in Table C-1.
5. The current state of the chip is now represented by INITIAL CONFIG in Table C-2.
6. Each input should now be brought low, starting at pin one and continuing in ascending order. Continue until all inputs are low. The output on TXD1 should now be low. Refer to Table C-2.
7. To exit test mode, tie LAD0 or LFRAME# high, and toggle PCI_RESET# from a low to a high state.

TABLE C-1: TOGGLING INPUTS IN DESCENDING ORDER

	Last Pin (N)	Pin N-1	Pin N-2	Pin N-3	Pin N-4	Pin ...	First Pin (1 of N)	Output Pin
INITIAL CONFIG	L	L	L	L	L	L	L	H or L
STEP 1	H	L	L	L	L	L	L	Toggles
STEP 2	H	H	L	L	L	L	L	Toggles
STEP 3	H	H	H	L	L	L	L	Toggles
STEP 4	H	H	H	H	L	L	L	Toggles
STEP 5	H	H	H	H	H	L	L	Toggles
…	…	…	…	…	…	…	…	…
STEP N	H	H	H	H	H	H	L	Toggles
END CONFIG	H	H	H	H	H	H	H	Toggles