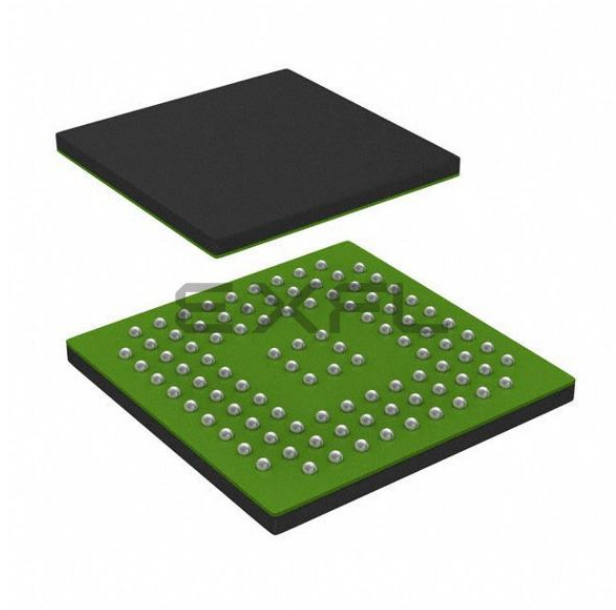

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	24
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3224-sy-tr

TABLE 1-1: DEVICE SPECIFIC SUMMARY

Function	SCH3227	SCH3226	SCH3224	SCH3222
LPC Bus Interface	YES	YES	YES	YES
PnP Config w/ 4 Port Addresses	YES	YES	YES	YES
Serial IRQ and SMI	YES	YES	YES	YES
Keyboard Controller	YES	YES	YES	YES
Watchdog Timer	YES	YES	YES	YES
Parallel Port	YES	NO	YES	NO
Reset Generator	YES	YES	YES	YES
Serial Ports, Full	4	4	2	4
Additional Serial Ports, 4-Pin	2 avail. (by strap option)	2 avail. (by strap option)	2	2
Infrared Port	YES	YES	YES	YES
Programmable Clock Output	YES	YES	YES	YES
IDE / PCI Reset Outputs	By strap option (vs. 4-pin Serial Ports).	By strap option (vs. 4-pin Serial Ports).	NO	NO
Power Button / AC Fail Support	By strap option (vs. 4-pin Serial Ports).	By strap option (vs. 4-pin Serial Ports).	NO	NO
GPIOs	40	40	24	23
GPIO with VID Compatible Inputs	6	6	0	6
Hardware Monitor	YES	YES	YES	NO
WFBGA Package	144-ball	100-ball	100-ball	84-ball

Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
K13	STRAPOPT (=VTR[a])	STRAPOPT (=VSS[a])
M4	RESERVED=VTR[b]	RESERVED=VTR[b]
C3	+12V_IN	+12V_IN
D3	+5V_IN	+5V_IN
E6	GP40	GP40
E3	VTR	VTR
E5	RESERVED=VSS[c]	RESERVED=VSS[c]
F8	TEST=VSS[c]	TEST=VSS[c]
F7	RESERVED=VSS[c]	RESERVED=VSS[c]
F3	VSS	VSS
F6	RESERVED=VSS[c]	RESERVED=VSS[c]
F5	RESERVED=VSS[c]	RESERVED=VSS[c]
G8	RESERVED=VSS[c]	RESERVED=VSS[c]
G6	RESERVED=VSS[c]	RESERVED=VSS[c]
H8	RESERVED=VSS[c]	RESERVED=VSS[c]
G5	RESERVED=VSS[c]	RESERVED=VSS[c]
H7	RESERVED=VSS[c]	RESERVED=VSS[c]
H6	RESERVED=VSS[c]	RESERVED=VSS[c]
H5	RESERVED=VSS[c]	RESERVED=VSS[c]
D2	CLOCKI	CLOCKI
E2	LAD0	LAD0
D1	LAD1	LAD1
E1	LAD2	LAD2
F2	LAD3	LAD3
F1	LFRAME#	LFRAME#
G2	LDRQ#	LDRQ#
H1	PCI_RESET#	PCI_RESET#
G1	PCI_CLK	PCI_CLK
H2	SER_IRQ	SER_IRQ
H3	VSS	VSS
J3	VCC	VCC
J1	GP44 / TXD6	nIDE_RSTDRV / GP44
J2	GP45 / RXD6	nPCIRST1 / GP45
K3	GP46 / nSCIN6	nPCIRST2 / GP46
L3	GP47 / nSCOUT6	nPCIRST3 / GP47
K1	AVSS	AVSS
L1	VBAT	VBAT
K2	GP27 / nIO_SMI / P17	GP27 / nIO_SMI / P17
L2	KDAT / GP21	KDAT / GP21
M1	KCLK / GP22	KCLK / GP22
M2	MDAT / GP32	MDAT / GP32
N1	MCLK / GP33	MCLK / GP33
M3	GP36 / nKBDRST	GP36 / nKBDRST

TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
D12	GP11 / TXD3	GP11 / TXD3
E11	GP14 / nDSR3	GP14 / nDSR3
C13	GP17 / nRTS3	GP17 / nRTS3
B13	GP16 / nCTS3	GP16 / nCTS3
C12	GP42 / nIO_PME	GP42 / nIO_PME
D11	VTR	VTR
A13	GP15 / nDTR3	GP15 / nDTR3
B12	GP61 / nLED2 / CLKO	GP61 / nLED2 / CLKO
C11	GP60 / nLED1 / WDT	GP60 / nLED1 / WDT
A12	GP13 / nRI3	GP13 / nRI3
B11	GP12 / nDCD3	GP12 / nDCD3
A11	GP31 / nRI4	GP31 / nRI4
C10	GP63 / nDCD4	GP63 / nDCD4
B10	CLKI32	CLKI32
A10	nRSMRST	nRSMRST
B9	VSS	VSS
C9	GP64 / RXD4	GP64 / RXD4
A9	GP65 / TXD4	GP65 / TXD4
A8	GP66 / nDSR4	GP66 / nDSR4
B8	GP67 / nRTS4	GP67 / nRTS4
C8	GP62 / nCTS4	GP62 / nCTS4
A7	GP34 / nDTR4	GP34 / nDTR4
B7	PWRGD_OUT	PWRGD_OUT
A6	PWRGD_PS	PWRGD_PS
C7	nFPRST / GP30	nFPRST / GP30
E8	VTR	VTR
E7	VSS	VSS
B6	nTHERMTRIP	nTHERMTRIP
A5	nHWM_INT	nHWM_INT
C6	PWM3	PWM3
B5	PWM2	PWM2
A4	PWM1	PWM1
B4	FANTACH3	FANTACH3
C5	FANTACH2	FANTACH2
C4	FANTACH1	FANTACH1
A3	HVSS	HVSS
B3	HVTR	HVTR
A2	REMOTE2-	REMOTE2-
A1	REMOTE2+	REMOTE2+
B1	REMOTE1-	REMOTE1-
C1	REMOTE1+	REMOTE1+
C2	VCCP_IN	VCCP_IN

2.2 Pin Functions

Table 2-5 lists all possible SCH322x pin functions. See Table 2-1 through Table 2-4 for the pins that apply to specific family members.

These functions are all available only on the SCH3227 device, and then certain functions require specific setting of the STRAPOPT pin, which is new to the SCH322x family. The STRAPOPT pin appears in the SCH3227 (Table 2-1) and SCH3226 (Table 2-2) family members only.

TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
PACKAGE PINOUT STRAP OPTION PIN (SCH3227 AND SCH3226 ONLY)						
	STRAPOPT	Pinout Strap Option		STRAPOPT	No Gate	I
POWER PINS						
2-3, 2-4	VCC	+3.3 Volt Supply Voltage				
2-3, 2-4	VTR	+3.3 Volt Standby Supply Voltage				
2-8	VBAT	+3.0 Volt Battery Supply)				
	VSS	Ground				
	AVSS	Analog Ground				
2-3	HVTR	Analog Power. +3.3V VTR pin dedicated to the Hardware Monitoring block. HVTR is powered by +3.3V Standby power VTR.				
2-3	HVSS	Analog Ground. Internally connected to all of the Hardware Monitoring Block circuitry.				
CLOCK PINS						
	CLKI32	32.768kHz Trickle Clock Input		CLKI32	No Gate	IS
	CLOCKI	14.318MHz Clock Input	CLOCKI			IS
LPC INTERFACE						
	LAD[3:0]	Multiplexed Command Address and Data	LAD[3:0]		GATE/ Hi-Z	PCI_IO
	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	LFRAME#		GATE	PCI_I
	LDRQ#	Encoded DMA Request	LDRQ#		GATE/Hi-Z	PCI_O
	PCI_RESET#	PCI Reset	PCI_RESET#		NO GATE	PCI_I
	PCI_CLK	PCI Clock	PCI_CLK		GATE	PCI_ICLK
	SER_IRQ	Serial IRQ	SER_IRQ		GATE / Hi-Z	PCI_IO
SERIAL PORT 1 INTERFACE						
	RXD1	Receive Data 1	RXD1		GATE	IS
	TXD1 /SIO XNOR_OUT	Transmit Data 1 / XNOR-Chain test mode Output for SIO block	TXD1 /SIO XNOR_OUT		HI-Z	O12/O12
	nDSR1	Data Set Ready 1	nDSR1		GATE	I

TABLE 6-7: REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL (CONTINUED)

Register Address (Note 6-4)	Register Name	Register Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Note 6-4 DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 6-5 Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 6-6 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 6-7 This bit no longer has a pin associated with it.

Note 6-8 When operating in the XT mode, this register is not available.

Note 6-9 These bits are always zero in the non-FIFO mode.

Note 6-10 Writing a one to this bit has no effect. DMA modes are not supported in this chip.

Note 6-11 The UARTs FCR's are shadowed UART FIFO Control Shadow Registers. See Section 24.0, "Runtime Register" for more details.

17.0 BUFFERED PCI OUTPUTS

17.1 Buffered PCI Outputs Interface

The SCH322x family devices provide three software controlled PCIRST# outputs and one buffered IDE Reset.

Table 17-1 describes the interface.

TABLE 17-1: BUFFERED PCI OUTPUTS INTERFACE

Name	Buffer	Power Well	Description
PCI_RESET#	PCI_I	VCC	PCI Reset Input
nIDE_RSTDRV	OD4	VCC	IDE Reset Output
nPCIRST1	O8/OD8	VCC	Buffered PCI Reset Output
nPCIRST2	O8/OD8	VCC	Buffered PCI Reset Output
nPCIRST3	O4/OD4	VCC	Buffered PCI Reset Output

17.1.1 IDE RESET OUTPUT

nIDE_RSTDRV is an open drain buffered copy of PCI_RESET#. This signal requires an external 1KΩ pull-up to VCC or 5V. This pin is an output only pin which floats when VCC=0. The pin function's default state on VTR POR is the nIDE_RST function; however the pin function can be programmed to the a GPO pin function by bit 2 in its GPIO control register.

The nIDE_RSTDRV output has a programmable forced reset. The software control of the programmable forced reset function is located in the GP4 GPIO Data register. When the GP44 bit (bit 4) is set, the nIDE_RSTDRV output follows the PCI_RESET# input; this is the default state on VTR POR. When the GP44 bit is cleared, the nIDE_RSTDRV output stays low.

See GP44 and GP4 for Runtime Register Description (Section 24.0, "Runtime Register," on page 213).

TABLE 17-2: NIDE_RSTDRV TRUTH TABLE

PCI_RESET# (Input)	nIDE_RSTDRV (Output)
0	0
1	Hi-Z

TABLE 17-3: NIDE_RSTDRV TIMING

Name	Description	MIN	TYP	MAX	Units
Tf	nIDE_RSTDRV high to low fall time. Measured form 90% to 10%			15	ns
Tpropf	nIDE_RSTDRV high to low propagation time. Measured from PCI_RESET# to nIDE_RSTDRV.			22	ns
CO	Output Capacitance			25	pF
CL	Load Capacitance			40	pF

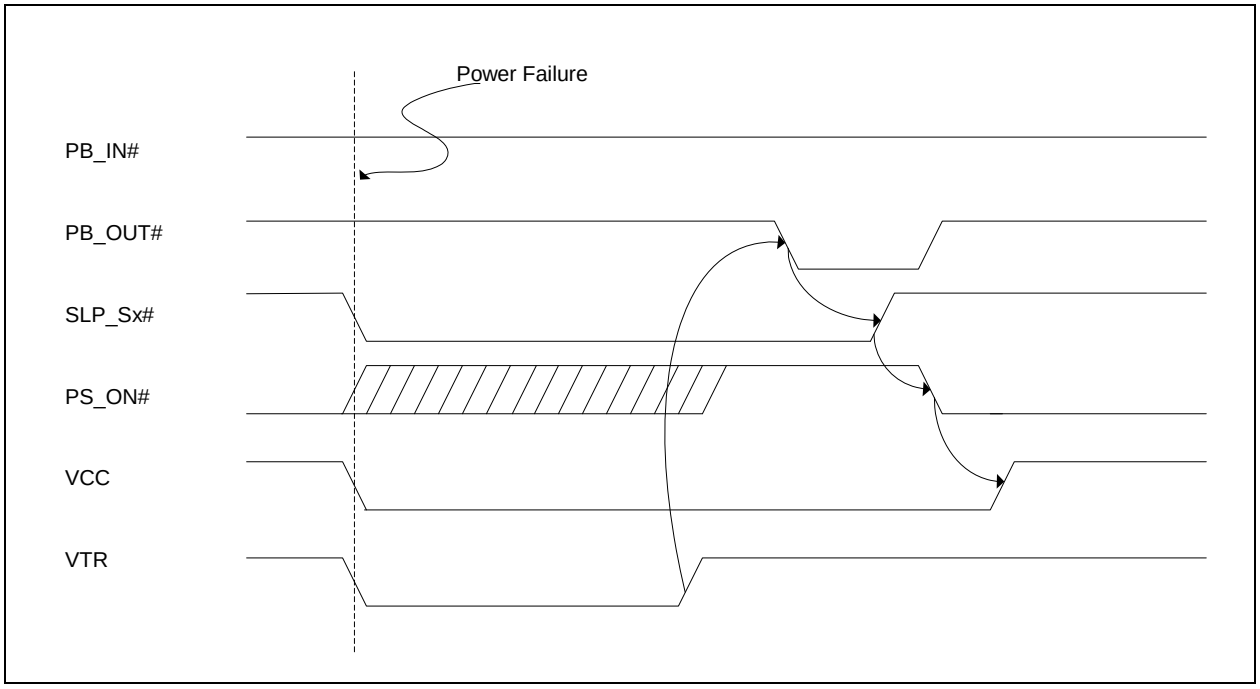
17.1.2 NPCIRSTX OUTPUT LOGIC

The nPCIRST1, nPCIRST2, and nPCIRST3 outputs are 3.3V balance buffer push-pull buffered copies of PCI_RESET# input. Each pin function's default state on VTR POR is the nPCIRSTx function; however, the pin function can be programmed to the a GPO pin (output only) function by bit 2 in the corresponding GPIO control register (GP45, GP46, GP47).

Each nPCIRSTx output has a programmable force reset. The software control of the programmable forced reset function is located in the GP4 GPIO Data register. When the corresponding (GP45, GP46 GP47) bit in the GP4 GPIO Data register is set, the nPCIRSTx output follows the PCI_RESET# input; this is the default state on VTR POR. When the corresponding (GP45, GP46, GP47) bit in the GP4 GPIO Data register is cleared, the nPCIRSTx output stays low.

See GP4 for Runtime Register Description.

FIGURE 18-5: POWER SUPPLY AFTER POWER FAILURE (RETURN TO ON)



18.4 Resume Reset Signal Generation

nRSMRST signal is the reset output for the ICH resume well. This signal is used as a power on reset signal for the ICH.

The SCH322x detects when VTR voltage raises above V_{TRIP} and provides a delay before generating the rising edge of nRSMRST. See Section 27.9, "Resume Reset Signal Generation," on page 275 for a detailed description of how the nRSMRST signal is generated.

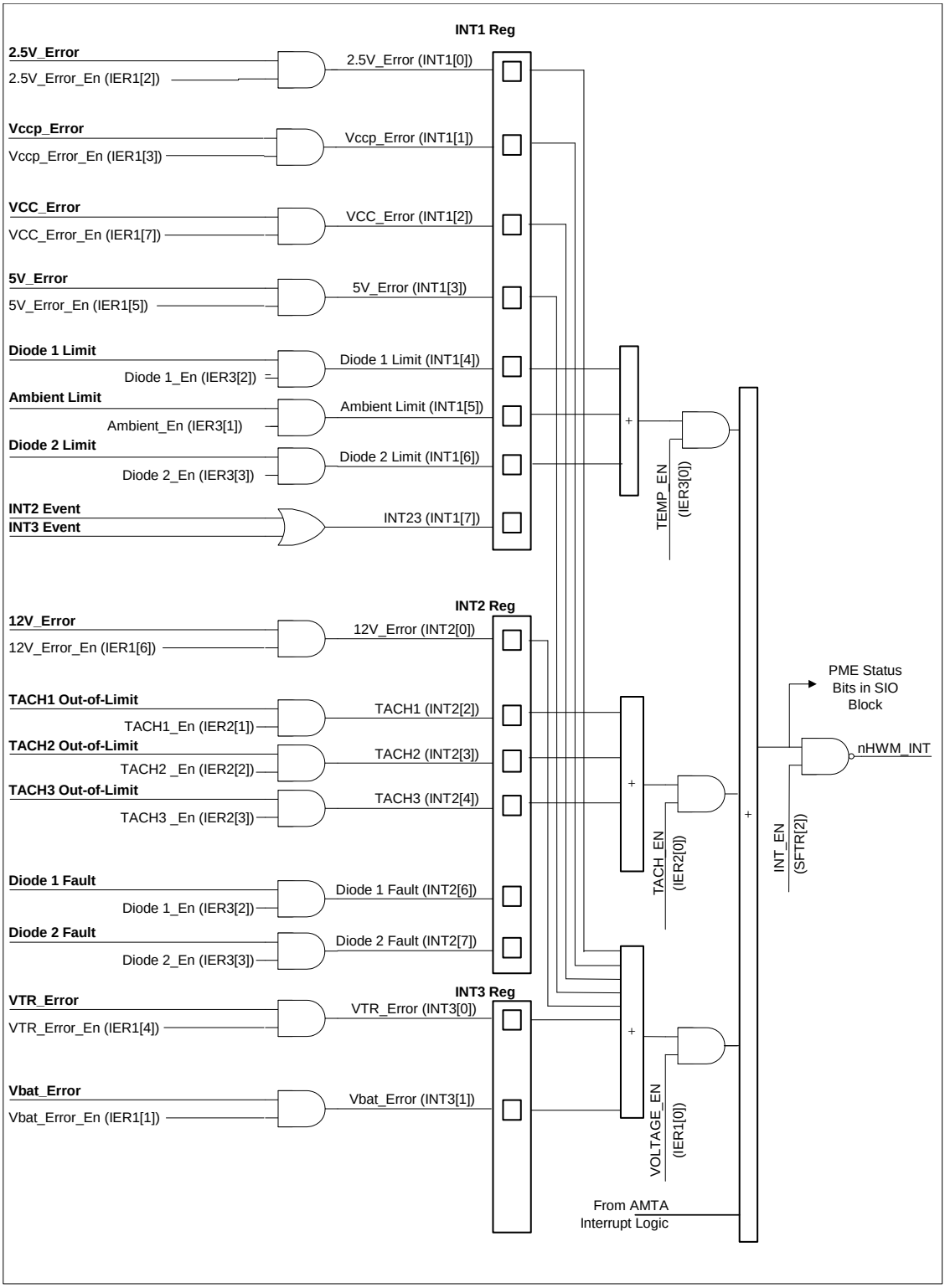
18.5 Keyboard Power Button

The SCH322x has logic to detect a keyboard make/break scan codes that may be used for wakeup (PME generation). The scan codes are programmed in the Keyboard Scan Code Registers, located in the runtime register block, from offset 0x5F to 0x63 from the base address located in the primary base I/O address in Logical Device A. These registers are powered by Vbat and are reset on a Vbat POR.

The following sections will describe the format of the keyboard data, the methods that may be used to decode the make codes, and the methods that may be used to decode the break codes.

The Wake on Specific Key Code feature is enabled for the assertion of the nIO_PME signal when in SX power state or below.

FIGURE 21-3: INTERRUPT CONTROL



The nHWM_INT pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding diode error bit to be set. This will cause the nHWM_INT pin to become active if enabled.

The nHWM_INT pin can be enabled to indicate fan errors. Bit[0] of the Interrupt Enable 2 (Fan Tachs) register (80h) is used to enable this option. This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The nHWM_INT pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the nHWM_INT pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to '1' again.

The nHWM_INT pin may only become active while the monitor block is operational.

21.9.2 INTERRUPT AS A PME EVENT

The hardware monitoring interrupt signal is routed to the SIO PME block. For a description of these bits see the section defining PME events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

The THERM PME status bit is located in the PME_STS1 Runtime Register at offset 04h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM PME status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the PME_EN1 register at offset 0Ah.

21.9.3 INTERRUPT AS AN SMI EVENT

The hardware monitoring interrupt signal is routed to the SIO SMI block. For a description of these bits see the section defining SMI events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

The THERM SMI status bit is located in the SMI_STS5 Runtime Register at offset 14h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM SMI status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the SMI_EN5 register at offset 1Ah.

The SMI is enabled onto the SERIRQ (IRQ2) via bit 6 of the SMI_EN2 register at 17h.

21.9.4 INTERRUPT EVENT ON SERIAL IRQ

The hardware monitoring interrupt signal is routed to the Serial IRQ logic. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

This operation is configured via the Interrupt Select register (0x70) in Logical Device A. This register allows the selection of any serial IRQ frame to be used for the HWM nHWM_INT interrupt (SERIRQ9 slot will be used). See Interrupt Event on Serial IRQ on page 130.

21.10 Low Power Mode

bit The hardware monitor has two modes of operation: Monitoring and Sleep. When the START bit, located in Bit[0] of the Ready/Lock/Start register (0x40), is set to zero the hardware monitor is in Sleep Mode. When this bit is set to one the hardware monitor is fully functional and monitors the analog inputs to this device.
bit Sleep mode is a low power mode in which bias currents are on and the internal oscillator is on, but the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

Note 1: In Sleep Mode the PWM Pins are held high forcing the PWM pins to 100% duty cycle (256/256).

2: The START a bit cannot be modified when the LOCK bit is set.

clear the status bit. Setting or clearing the START bit when the individual enable bit is one has no effect on the status bits.

Note 1: The individual enable bits for D2, AMB, and D1 are located in the Interrupt Enable 3 (Temp) register at offset 82h.

2: Clearing the group Temp enable bit or the global INTEN enable bit has no effect on the status bits.

Bit	Name	R/W	Default	Description
0	2.5V_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the Vccp input voltage is less than or equal to the limit set in the Vccp Low Limit register or greater than the limit set in the Vccp High Limit register.
2	VCC_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the VCC input voltage is less than or equal to the limit set in the VCC Low Limit register or greater than the limit set in the VCC High Limit register.
3	5V_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Remote Diode 1 Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ is less than or equal to the limit set in the Remote Diode 1 Low Temp register or greater than the limit set in Remote Diode 1 High Temp register.
5	Internal Sensor Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal Low Temp register or greater than the limit set in the Internal High Temp register.
6	Remote Diode 2 Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the Remote2- and Remote2+ is less than or equal to the limit set in the Remote Diode 2 Low Temp register or greater than the limit set in the Remote Diode 1 High Temp register.
7	INT2 Event Active	R/WC	0	The device automatically sets this bit to 1 when a status bit is set in the Interrupt Status Register 2.

22.2.11 REGISTER 42H: INTERRUPT STATUS REGISTER 2

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
42h	R/WC	Interrupt Status Register 2	ERR2	ERR1	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	RES	12V	00h

Note 1: This register is reset to its default value when the PWRGD_PS signal transitions high.

2: This is a read/write-to-clear register. The status bits are cleared on a write of one if the event causing the interrupt is no longer active. Writing a zero to these bits has no effect.

The Interrupt Status Register 2 bits is automatically set by the device whenever a tach reading value is above the minimum value set in the tachometer minimum registers or when a remote diode fault occurs. When a remote diode fault occurs (if the start bit is set) 80h will be loaded into the associated temperature reading register, which causes the associated diode limit error bit to be set (see Register 41h: Interrupt Status Register 1 on page 167) in addition to the diode fault bit (ERRx). These individual status bits remain set until the bit is written to one by software or until the individual enable bit is cleared, even if the event no longer persists.

- Clearing the status bits by a write of ‘1’
  - The FANTACHx status bits are cleared (set to 0) automatically by the SCH322x after they are written to one by software, if the FANTACHx reading register no longer violates the programmed FANTACH Limit. (See Registers 28-2Dh: Fan Tachometer Reading on page 164 and Registers 54-59h: Fan Tachometer Low Limit on page 171)

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
9Bh	R/W	VTR Low Limit	7	6	5	4	3	2	1	0	00h
9Ch	R/W	VTR High Limit	7	6	5	4	3	2	1	0	FFh
9Dh	R/W	Vbat Low Limit	7	6	5	4	3	2	1	0	00h
9Eh	R/W	Vbat High Limit	7	6	5	4	3	2	1	0	FFh

Setting the Lock bit has no effect on these registers.

If a voltage input either exceeds the value set in the voltage high limit register or falls below or equals the value set in the voltage low limit register, the corresponding bit will be set automatically in the interrupt status registers (41-42h, 83h). Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each register will read C0h, except for the Vbat input. Vbat is nominally a 3.0V input that is implemented on a +3.3V (nominal) analog input. Therefore, the nominal reading for Vbat is AEh.

Note: Vbat will only be monitored when the Vbat Monitoring Enable bit is set to '1'. Updating the Vbat reading register automatically clears the Vbat Monitoring Enable bit.

TABLE 22-5: VOLTAGE LIMITS VS. REGISTER SETTING

Input	Nominal Voltage	Register Reading at Nominal Voltage	Maximum Voltage	Register Reading at Maximum Voltage	Minimum Voltage	Register Reading at Minimum Voltage
VTR	3.3V	C0h	4.38V	FFh	0V	00h
Vbat (Note 2 2-17)	3.0V	AEh	4.38V	FFh	0V	00h
2.5V	5.0V	C0h	6.64V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

Note 22-17 Vbat is a nominal 3.0V input source that has been implemented on a 3.3V analog voltage monitoring input.

22.2.13 REGISTERS 4E-53H: TEMPERATURE LIMIT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
4Eh	R/W	Remote Diode 1 Low Temp	7	6	5	4	3	2	1	0	81h
4Fh	R/W	Remote Diode 1 High Temp	7	6	5	4	3	2	1	0	7Fh
50h	R/W	Ambient Low Temp	7	6	5	4	3	2	1	0	81h
51h	R/W	Ambient High Temp	7	6	5	4	3	2	1	0	7Fh
52h	R/W	Remote Diode 2 Low Temp	7	6	5	4	3	2	1	0	81h
53h	R/W	Remote Diode 2 High Temp	7	6	5	4	3	2	1	0	7Fh

Setting the Lock bit has no effect on these registers.

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or is less than or equal to the value set in the low limit register, the corresponding bit will be set automatically by the SCH322x in the Interrupt Status Register 1 (41h). For example, if the temperature reading from the Remote1- and Remote1+ inputs exceeds the Remote Diode 1 High Temp register limit setting, Bit[4] D1 of the Interrupt Status Register 1 will be set. The temperature limits in these registers are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 22-6.

Note: The range numbers will be used to calculate the slope of the PWM ramp up. For the fractional entries, the PWM will go on full when the temp reaches the next integer value e.g., for 3.33, PWM will be full on at (min. temp + 4).

22.2.17 REGISTER 62H, 63H: PWM RAMP RATE CONTROL

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
62h	R/W	PWM 1 Ramp Rate Control	RES1	RES1	RES1	RES	RR1E	RR1-2	RR1-1	RR1-0	E0h
63h	R/W	PWM 2, PWM 3 Ramp Rate Control	RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

RES1 bits are set to '1' and are read only, writes are ignored.

Description of Ramp Rate Control bits:

If the Remote1 or Remote2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the part. The auto fan control logic calculates the PWM duty cycle for all temperature readings. If Ramp Rate Control is disabled, the PWM output will jump or oscillate between different PWM duty cycles causing the fan to suddenly change speeds, which creates unwanted fan noise. If enabled, the PWM Ramp Rate Control logic will prevent the PWM output from jumping, instead the PWM will ramp up/down towards the new duty cycle at a pre-determined ramp rate.

Ramp Rate Control

The Ramp Rate Control logic limits the amount of change to the PWM duty cycle over a period of time. This period of time is programmable via the Ramp Rate Control bits. For a detailed description of the Ramp Rate Control bits see Table 22-11.

Note 1: RR1E, RR2E, and RR3E enable PWM Ramp Rate Control for PWM 1, 2, and 3 respectively.

2: RR1-2, RR1-1, and RR1-0 control ramp rate time for PWM 1

3: RR2-2, RR2-1, and RR2-0 control ramp rate time for PWM 2

4: RR3-2, RR3-1, and RR3-0 control ramp rate time for PWM 3

TABLE 22-11: PWM RAMP RATE CONTROL

RRx-[2:0]	PWM Ramp Time (SEC) (Time from 33% Duty Cycle to 100% Duty Cycle)	PWM Ramp Time (SEC) (Time from 0% Duty Cycle to 100% Duty Cycle)	Time per PWM Step (PWM Step Size = 1/255)	PWM Ramp Rate (Hz)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

Note: This assumes the Ramp Rate Enable bit (RRxE) is set.

TABLE 23-3: CONFIGURATION REGISTER SUMMARY (CONTINUED)

Index	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Configuration Register
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 4 Mode Register
LOGICAL DEVICE D CONFIGURATION REGISTERS (SERIAL PORT 5) AVAILABLE IN SCH3224, SCH3222; IF STRAPOPT=1 SCH3227, SCH3226						
0x30	R/W	0x00	0x00	0x00	0x00	Activate Note 23-2
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 5 Mode Register
LOGICAL DEVICE E CONFIGURATION REGISTERS (SERIAL PORT 6) AVAILABLE IN SCH3224, SCH3222; IF STRAPOPT=1 SCH3227, SCH3226						
0x30	R/W	0x00	0x00	0x00	0x00	Activate Note 23-2
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 6 Mode Register
LOGICAL DEVICE F CONFIGURATION REGISTERS (RESERVED)						

Note 23-2 Serial ports 1 and 2 may be placed in the powerdown mode by clearing the associated activate bit located at CR30 or by clearing the associated power bit located in the Power Control register at CR22. Serial ports 3,4,5,6 (if available) may be placed in the powerdown mode by clearing the associated activate bit located at CR30. When in the powerdown mode, the serial port outputs are tristated. In cases where the serial port is multiplexed as an alternate function, the corresponding output will only be tristated if the serial port is the selected alternate function.

23.1.1 GLOBAL CONFIG REGISTERS

The chip-level (global) registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the ADDRESS Port for register selection. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

TABLE 23-4: CHIP-LEVEL (GLOBAL) CONFIGURATION REGISTERS

Register	Address	Description
CHIP (GLOBAL) CONTROL REGISTERS		
	0x00 - 0x01	Reserved - Writes are ignored, reads return 0.
Config Control Default = 0x00 on VCC POR, VTR POR and PCI RESET	0x02 W	The hardware automatically clears this bit after the write, there is no need for software to clear the bits. Bit 0 = 1: Soft Reset. Refer to theTable 23-3, “Configuration Register Summary,” on page 196 for the soft reset value for each register.
	0x03 - 0x06	Reserved - Writes are ignored, reads return 0.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SP34 Option Default = 0x44 on VTR POR (All except SCH3224)	0x13 (R/W)	Bit[0] Automatic Direction Control Select SP3 1=FC on 0=FC off Bits[1] Signal select SP3 1=nRTS control 0=nDTR control Bits[2] Polarity SP3 0= Drive low when enabled 1= Drive 1 when enabled Bits[3] RESERVED Bit[4] Automatic Direction Control Select SP4 1=FC on 0=FC off Bits[5] Signal select SP4 1=nRTS control 0=nDTR control Bits[6] Polarity SP4 0= Drive low when enabled 1= Drive 1 when enabled Bits[7] RESERVED
SMI_STS1 Default = 0x02, or 0x03 On VTR POR. The default will be 0x03 if there is a LOW_BAT event under VBAT power only, or 0x02 if this event does not occur. Bit 0 will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. Bit 1 is set to '1' on VCC POR, VTR POR, PCI Reset and soft reset.	14 Bits[0] are R/WC. Bits[1:4,7] are RO.	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source except as shown. Bit[0] LOW_BAT. Cleared by a write of '1'. When the battery is removed and replaced or if the battery voltage drops below 1.2V (nominal) under battery power only (VBAT POR), then the LOW_BAT SMI status bit is set on VTR POR. When the battery voltage drops below 2.4 volts (nominal) under VTR power (VCC=0) or under battery power only, the LOW_BAT SMI status bit is set on VCC POR. Bit[1] PINT. The parallel port interrupt defaults to '1' when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[2] U2INT Bit[3] U1INT Bit[4] FINT Bit[5] Reserved Bit[6] Reserved Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	15 (R/W) Bits[0,1] are RO Bits[2] is Read-Clear.	SMI Status Register 2 This register is used to read the status of the SMI inputs. Bit[0] MINT. Cleared at source. Bit[1] KINT. Cleared at source. Bit[2] IRINT. This bit is set by a transition on the IR pin (IRRX). Cleared by a read of this register. Bit[3] Reserved Bit[4] SPEMSE_STS (Wake on specific mouse click) - Cleared by writing a '1' Bit[7:5] Reserved

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

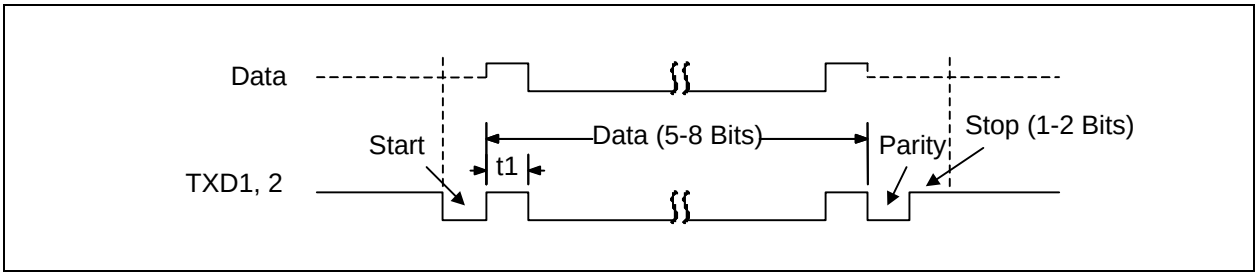
Name	REG Offset (HEX)	Description
GP21 Default =0x8C on VTR POR	2C (R/W)	General Purpose I/O bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KDAT (Default) 10=Either Edge Triggered Interrupt Input 0 (Note 24-20) 01=Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull (Default) **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KDAT function, bit[0] should always be programmed to '0'. The KDAT function will not operate properly when bit[0] is set.
GP22 Default =0x8C on VTR POR	2D (R/W)	General Purpose I/O bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KCLK (Default) 10=Either Edge Triggered Interrupt Input 1 (Note 24-20) 01= Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KCLK function, bit[0] should always be programmed to '0'. The KCLK function will not operate properly when bit[0] is set.
UART5 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2E (R)	Bits[7:0] RESERVED
UART5 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2E (R)	UART FIFO Control Shadow 5 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
UART6 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2F (R)	Bits[7:0] RESERVED
UART6 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2F (R)	Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP2 Default = 0x00 on VTR POR	4C (R/W)	General Purpose I/O Data Register 2 Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] GP27
GP3 Default = 0x00 on VTR POR	4D (R/W)	General Purpose I\O Data Register 3 Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] Reserved Bit[6] GP36 Bit[7] GP37
GP4 Default = 0xF0 on VTR POR	4E (R/W)	General Purpose I/O Data Register 4 Bit[0] GP40 Bit[1] Reserved Bit[2] GP42 Bit[3] Reserved Bit[4] GP44 Bit[5] GP45 Bit[6] GP46 Bit[7] GP47
GP5 Default = 0x00 on VTR POR	4F (R/W)	General Purpose I/O Data Register 5 Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57
GP6 Default = 0x00 on VTR POR	50 (R/W)	General Purpose I/O Data Register 6 Bit[0] GP60 Bit[1] GP61 Bit[2] GP62 Bit[3] GP63 Bit[4] GP64 Bit[5] GP65 Bit[6] GP66 Bit[7] GP67
N/A	51 (R)	Bits[7:0] Reserved – reads return 0

27.7 UART Interface Timing

FIGURE 27-24: SERIAL PORT DATA

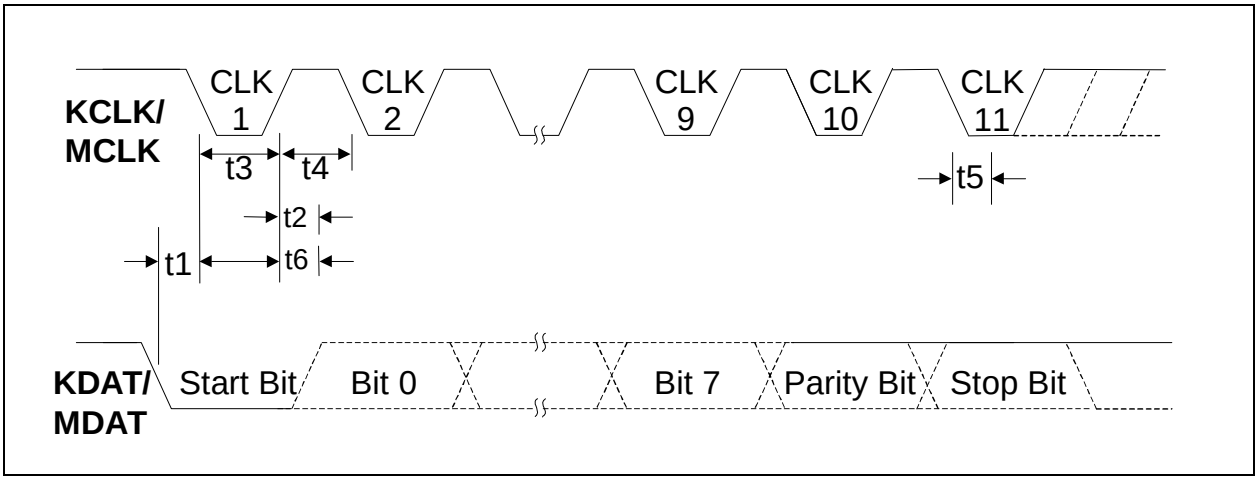


Name	Description	MIN	TYP	MAX	Units
t1	Serial Port Data Bit Time		t_{BR}[1]		nsec

t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

27.8 Keyboard/Mouse Interface Timing

FIGURE 27-25: KEYBOARD/MOUSE RECEIVE/SEND DATA TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Time from DATA transition to falling edge of CLOCK (Receive)	5		25	µsec
t2	Time from rising edge of CLOCK to DATA transition (Receive)	5		T4-5	µsec
t3	Duration of CLOCK inactive (Receive/Send)	30		50	µsec
t4	Duration of CLOCK active (Receive/Send)	30		50	µsec
t5	Time to keyboard inhibit after clock 11 to ensure the keyboard does not start another transmission (Receive)	>0		50	µsec
t6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	µsec

APPENDIX A: ADC VOLTAGE CONVERSION

TABLE A-1: ANALOG-TO-DIGITAL VOLTAGE CONVERSIONS FOR HARDWARE MONITORING BLOCK

Input Voltage					A/D Output	
+12 V	**+5 V** Note 28-1	**+3.3 V** Note 28-2	**+2.5V**	**1.5V**	**Decimal**	**Binary**
<0.062	<0.026	<0.0172	<0.013	<0.008	0	0000 0000
0.062–0.125	0.026–0.052	0.017–0.034	0.013 - 0.031	0.008 - 0.015	1	0000 0001
0.125–0.188	0.052–0.078	0.034–0.052	0.031 - 0.039	0.015 - 0.024	2	0000 0010
0.188–0.250	0.078–0.104	0.052–0.069	0.039 - 0.052	0.024 - 0.031	3	0000 0011
0.250–0.313	0.104–0.130	0.069–0.086	0.052 - 0.065	0.031 - 0.039	4	0000 0100
0.313–0.375	0.130–0.156	0.086–0.103	0.065 - 0.078	0.039 - 0.047	5	0000 0101
0.375–0.438	0.156–0.182	0.103–0.120	0.078 - 0.091	0.047 - 0.055	6	0000 0110
0.438–0.500	0.182–0.208	0.120–0.138	0.091 - 0.104	0.055 - 0.063	7	0000 0111
0.500–0.563	0.208–0.234	0.138–0.155	0.104 - 0.117	0.063 - 0.071	8	0000 1000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
4.000–4.063	1.666–1.692	1.100–1.117	0.833 - 0.846	0.501 - 0.508	64 (1/4 Scale)	0100 0000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
8.000–8.063	3.330–3.560	2.200–2.217	1.665- 1.780	1.001 - 1.009	128 (1/2 Scale)	1000 0000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
12.000–12.063	5.000–5.026	3.300–3.317	2,500 - 2.513	1.502 - 1.509	192 (3/4 Scale)	1100 0000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
15.312–15.375	6.380–6.406	4.210–4.230	3.190 - 3.200	1.916 - 1.925	245	1111 0101
15.375–15.437	6.406–6.432	4.230–4.245	3.200 - 3.216	1.925 - 1.931	246	1111 0110
15.437–15.500	6.432–6.458	4.245–4.263	3.216 - 3.229	1.931 - 1.948	247	1111 0111
15.500–15.563	6.458–6.484	4.263–4.280	3.229 - 3.242	1.948 - 1.947	248	1111 1000
15.625–15.625	6.484–6.510	4.280–4.300	3.242 - 3.255	1.947 - 1.957	249	1111 1001
15.625–15.688	6.510–6.536	4.300–4.314	3.255 - 3.268	1.957 - 1.963	250	1111 1010
15.688–15.750	6.536–6.562	4.314–4.330	3.268 - 3.281	1.963 - 1.970	251	1111 1011
15.750–15.812	6.562–6.588	4.331–4.348	3.281 - 3.294	1.970 - 1.978	252	1111 1100
15.812–15.875	6.588–6.615	4.348–4.366	3.294 - 3.308	1.978 - 1.987	253	1111 1101
15.875–15.938	6.615–6.640	4.366–4.383	3.308 - 3.320	1.987 - 1.994	254	1111 1110
>15.938	>6.640	>4.383	> 3.320	> 1.994	255	1111 1111

Note 28-1 The 5V input is a +5V nominal inputs. 2.5V input is a 2.5V nominal input.

Note 28-2 The VCC, VTR, and Vbat inputs are +3.3V nominal inputs. VCC and VTR are nominal 3.3V power supplies. Vbat is a nominal 3.0V power supply.

APPENDIX C: TEST MODE

The SCH322x provides board test capability through the implementation of one XNOR chain and one XOR chain. The XNOR chain is dedicated to the Super I/O portion and the Hardware Monitoring Block of the device.

Note:	Pins that are not brought out of the package are tied to a determinate voltage internal to the package, and so will not affect the XNOR output, except that its initial state may differ among family members.

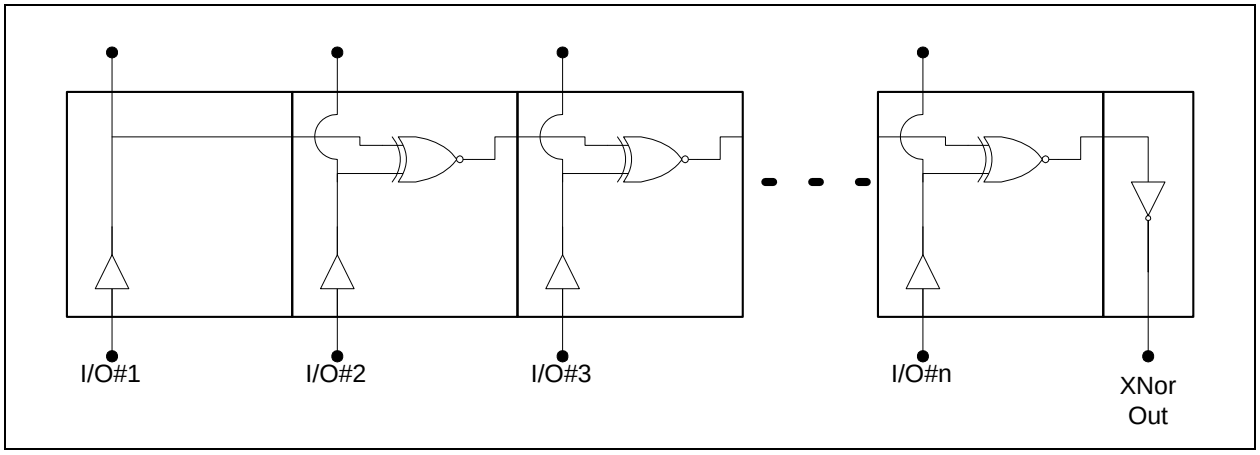
C.1 XNOR-Chain Test Mode Overview

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure C-1. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SCH322x pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

FIGURE C-1: XNOR-CHAIN TEST STRUCTURE



C.1.1 Board Test Mode

Board test mode can be entered as follows:

On the rising (deasserting) edge of PCI_RESET#, drive LFRAME# low and drive LAD[0] low.

Exit board test mode as follows:

On the rising (deasserting) edge of PCI_RESET#, drive either LFRAME# or LAD[0] high.

The PCI_RESET# pin is not included in the XNOR-Chain. The XNOR-Chain output pin# is TXD1. See the following sub-sections for more details.

Pin List of XNOR Chain

All pins on the chip are inputs to the first XNOR chain, with the exception of the following:

- All power supply pins - HVTR, HVSS, VCC, VTR, and Vbat
- VSS and AVSS
- All analog inputs: Remote2-, Remote2+, Remote1-, Remote1+, VCCP_IN, +12V_IN, +5V_IN, +2.5V_IN
- TXD1 This is the chain output.
- PCI_RESET#.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	-	XX	-	[XX]
Device	Temperature Range		Package		Tape and Reel Option

Device:	SCH3227/SCH3226/SCH3224/SCH3222
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)
Package:	SZ = 144-pin WFBGA (SCH3227) SY = 100-pin WFBGA (SCH3226. SCH3224) SX = 84-pin WFBGA (SCH3222)
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel (Note 1)

Examples:

a) SCH3227-SZ
Commercial temperature, 144-pin WFBGA, Tray

b) SCH3227I-SZ-TR
Industrial temperature, 144-pin WFBGA, Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.