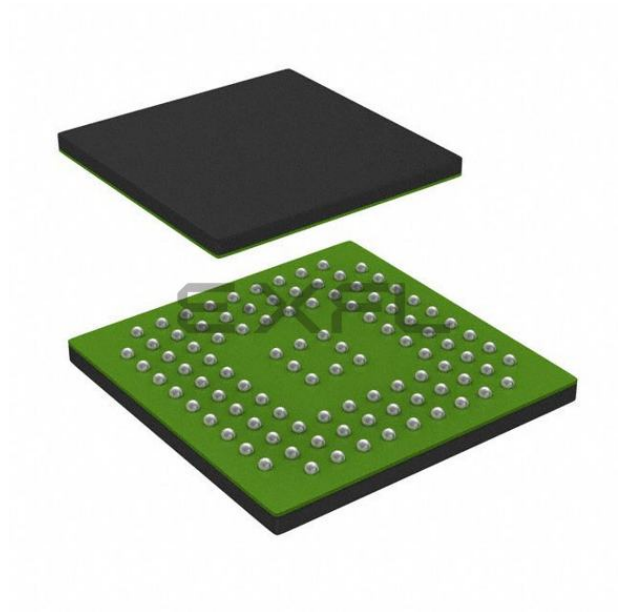

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Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	24
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3224-sy

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FIGURE 2-4: SCH3222 PIN DIAGRAM

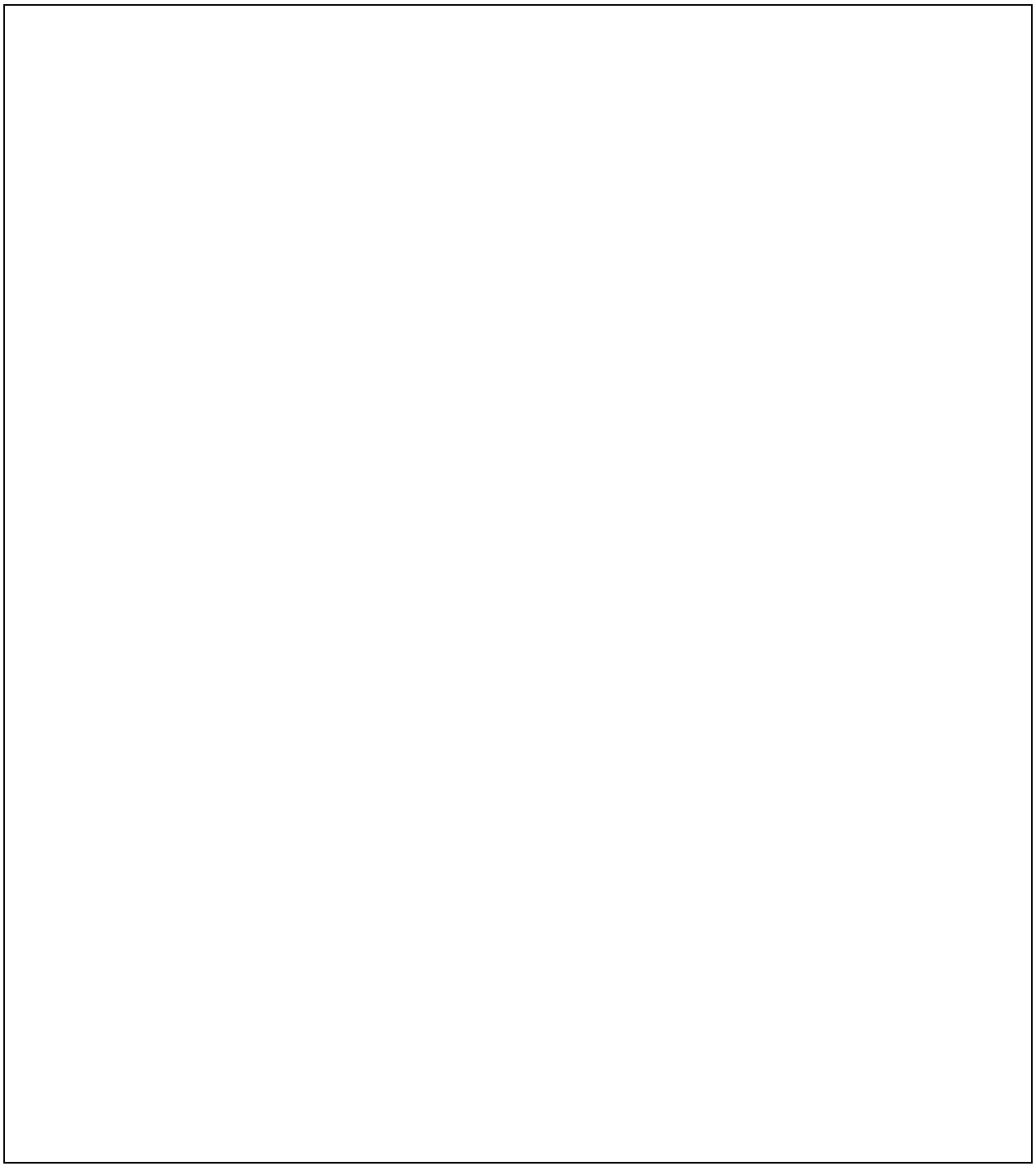


TABLE 5-1: SUPPORTED LPC CYCLES (CONTINUED)

Cycle Type	Transfer Size	Comment
Bus Master I/O Write	2 Byte	Not Supported
Bus Master I/O Write	4 Byte	Not Supported
Bus Master I/O Read	1 Byte	Not Supported
Bus Master I/O Read	2 Byte	Not Supported
Bus Master I/O Read	4 Byte	Not Supported

5.3 Device Specific Information

The LPC interface conforms to the *"Low Pin Count (LPC) Interface Specification"*. The following section will review any implementation specific information for this device.

5.3.1 SYNC PROTOCOL

The SYNC pattern is used to add wait states. For read cycles, the SCH3227/SCH3226/SCH3224/SCH3222 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SCH3227/SCH3226/SCH3224/SCH3222 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SCH3227/SCH3226/SCH3224/SCH3222 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value. The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The SCH3227/SCH3226/SCH3224/SCH3222 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the SCH3227/SCH3226/SCH3224/SCH3222 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

5.3.2 RESET POLICY

The following rules govern the reset policy:

- When PCI_RESET# goes inactive (high), the PCI clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
- When PCI_RESET# goes active (low):

1. The host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
2. The SCH3227/SCH3226/SCH3224/SCH3222 ignores LFRAME#, tristates the LAD[3:0] pins and drives the LDRQ# signal inactive (high).

Host I/F Status Register

The Status register is 8 bits wide.

Table 10-3 shows the contents of the Status register.

TABLE 10-3: STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

Status Register

This register is cleared on a reset. This register is read-only for the Host and read/write by the SCH3227/SCH3226/SCH3224/SCH3222 CPU.

UD Writable by SCH3227/SCH3226/SCH3224/SCH3222 CPU. These bits are user-definable.

C/D (Command Data)-This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to “1” if SA2 = 1 or reset to “0” if SA2 = 0.

IBF (Input Buffer Full)- This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the SCH3227/SCH3226/SCH3224/SCH3222 CPU’s nIBF (MIRQ) interrupt if enabled. When the SCH3227/SCH3226/SCH3224/SCH3222 CPU reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full) - This flag is set to whenever the SCH3227/SCH3226/SCH3224/SCH3222 CPU write to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

10.7 External Clock Signal

The SCH3227/SCH3226/SCH3224/SCH3222 Keyboard Controller clock source is a 12 MHz clock generated from a 14.318 MHz clock. The reset pulse must last for at least 24 16 MHz clock periods. The pulse-width requirement applies to both internally (VCC POR) and externally generated reset signals. In power-down mode, the external clock signal is not loaded by the chip.

10.8 Default Reset Conditions

The SCH3227/SCH3226/SCH3224/SCH3222 has one source of hardware reset: an external reset via the PCI_RESET# pin. Refer to Table 10-4 for the effect of each type of reset on the internal registers.

TABLE 10-4: RESETS

Description	Hardware Reset (PCI_RESET#)
KCLK	Low
KDAT	Low
MCLK	Low
MDAT	Low
Host I/F Data Reg	N/A
Host I/F Status Reg	00H
Note: N/A = Not Applicable	

10.9 GATEA20 and Keyboard Reset

The SCH3227/SCH3226/SCH3224/SCH3222 provides two options for GateA20 and Keyboard Reset: 8042 Software Generated GateA20 and KRESET and Port 92 Fast GateA20 and KRESET.

18.0 POWER CONTROL FEATURES

The SCH322x family devices are able to turn on the power supply when the power button located on the PC chassis is pressed, when the power button located on the keyboard is pressed, or when recovering from a power failure. The signals used to support these features are:

- PB_IN#
- PB_OUT#
- SLP_Sx#
- PS_ON#

Table 18-1 and Figure 18-1 describe the interface and connectivity of the following Power Control Features:

1. Front Panel Reset with Input Debounce, Power Supply Gate, and Powergood Output Signal Generation
2. AC Recovery Circuit
3. Keyboard Wake on Mouse.
4. SLP_Sx# PME wakeup

TABLE 18-1: POWER CONTROL INTERFACE

Name	Direction	Description
PB_IN#	Input	Power Button Input
PB_OUT#	Output	Power Good Output
PS_ON#	Output	Power Supply On output
SLP_SX#	Input	From south bridge
PWRGD_PS	Input	Power Good Input from Power Supply
nFPRST	Input	Reset Input from Front Panel
PWRGD_OUT	Output	Power Good Output – Open Drain
nIO_PME	Output	Power Management Event Output signal allows this device to request wakeup.

20.0 BATTERY BACKED SECURITY KEY REGISTER

Located at the Secondary Base I/O Address of Logical Device A is a 32 byte CMOS memory register dedicated to security key storage. This security key register is battery powered and has the option to be read protected, write protected, and lockable. The Secondary Base I/O Address is programmable at offsets 0x62 and 0x63. See Table 20-1, "Security Key Register Summary" is a complete list of the Security Key registers.

TABLE 20-1: SECURITY KEY REGISTER SUMMARY

Register Offset (HEX)	VBAT POR	Register
00	0x00	Security Key Byte 0
01	0x00	Security Key Byte 1
02	0x00	Security Key Byte 2
03	0x00	Security Key Byte 3
04	0x00	Security Key Byte 4
05	0x00	Security Key Byte 5
06	0x00	Security Key Byte 6
07	0x00	Security Key Byte 7
08	0x00	Security Key Byte 8
09	0x00	Security Key Byte 9
0A	0x00	Security Key Byte 10
0B	0x00	Security Key Byte 11
0C	0x00	Security Key Byte 12
0D	0x00	Security Key Byte 13
0E	0x00	Security Key Byte 14
0F	0x00	Security Key Byte 15
10	0x00	Security Key Byte 16
11	0x00	Security Key Byte 17
12	0x00	Security Key Byte 18
13	0x00	Security Key Byte 19
14	0x00	Security Key Byte 20
15	0x00	Security Key Byte 21
16	0x00	Security Key Byte 22
17	0x00	Security Key Byte 23
18	0x00	Security Key Byte 24
19	0x00	Security Key Byte 25
1A	0x00	Security Key Byte 26
1B	0x00	Security Key Byte 27
1C	0x00	Security Key Byte 28
1D	0x00	Security Key Byte 29
1E	0x00	Security Key Byte 30
1F	0x00	Security Key Byte 31

Access to the Security Key register block is controlled by bits [2:1] of the Security Key Control (SKC) Register located in the Configuration Register block, Logical Device A, at offset 0xF2. The following table summarizes the function of these bits.

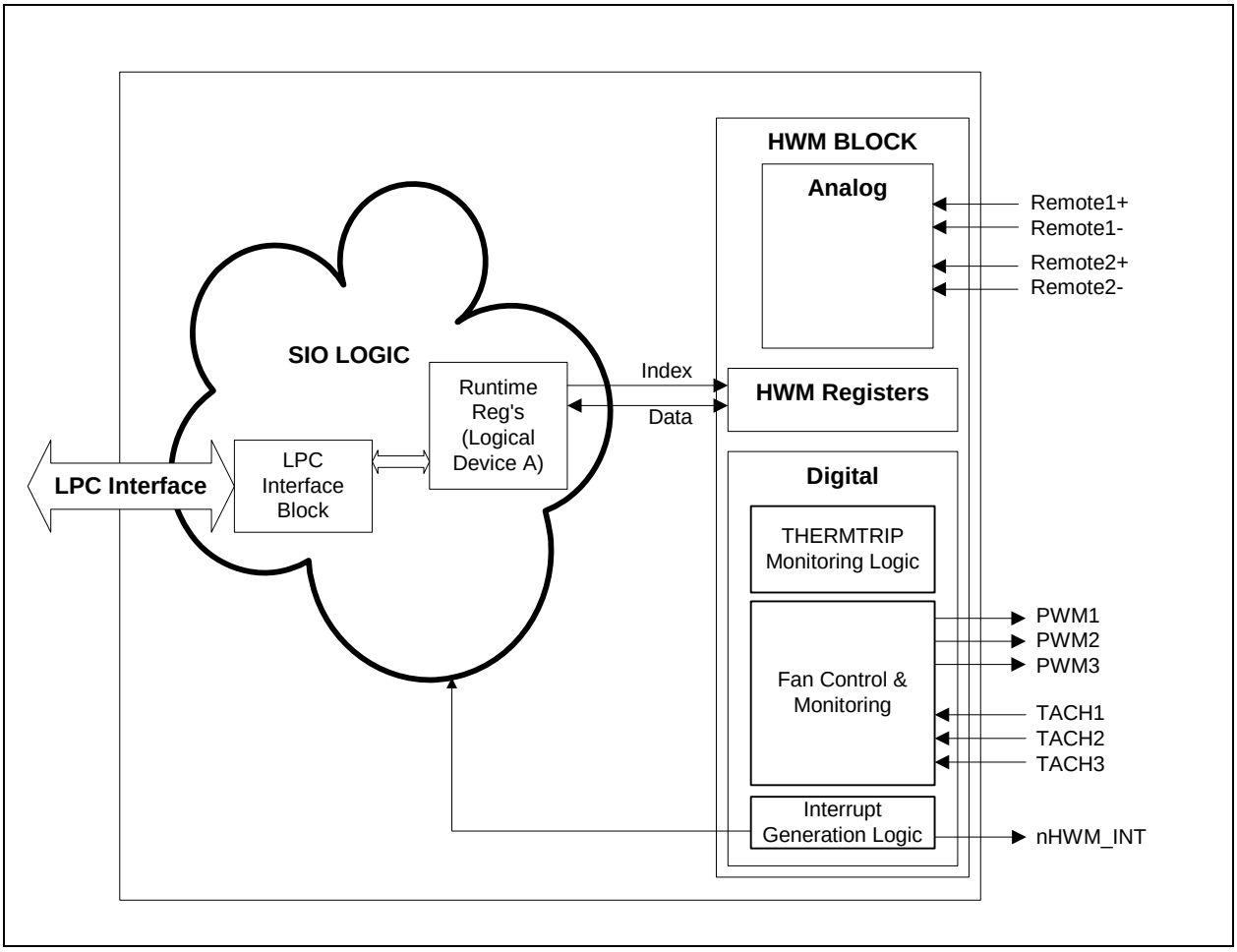
21.0 TEMPERATURE MONITORING AND FAN CONTROL

The Hardware Monitoring (HWM) block contains the temperature monitoring and fan control functions. The following sub-sections describe the HWM block features.

Note:	The SCH3222 device does not bring out these pins, and therefore the HWM block and this chapter are irrelevant to it.

21.1 Block Diagram

FIGURE 21-1: HWM BLOCK EMBEDDED IN SCH322X



21.11 Temperature Measurement

Temperatures are measured internally by bandgap temperature sensor and externally using two sets of diode sensor pins (for measuring two external temperatures). See subsections below.

Note: The temperature sensing circuitry for the two remote diode sensors is calibrated for a 3904 type diode.

21.11.1 INTERNAL TEMPERATURE MEASUREMENT

Internal temperature can be measured by bandgap temperature sensor. The measurement is converted into digital format by internal ADC. This data is converted in two's complement format since both negative and positive temperature can be measured. This value is stored in Internal Temperature Reading register (26h) and compared to the Temperature Limit registers (50h – 51h). If this value violates the programmed limits in the Internal High Temperature Limit register (51h) and the Internal Low Temperature Limit register (50h) the corresponding status bit in Interrupt Status Register 1 is set.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled Auto Fan Control Operating Mode on page 134.

21.11.2 EXTERNAL TEMPERATURE MEASUREMENT

The Hardware Monitor Block also provides a way to measure two external temperatures using diode sensor pins (Remote x+ and Remote x-). The value is stored in the register (25h) for Remote1+ and Remote1- pins. The value is stored in the Remote Temperature Reading register (27h) for Remote2+ and Remote2- pins. If these values violate the programmed limits in the associated limit registers, then the corresponding Remote Diode 1 (D1) or Remote Diode 2 (D2) status bits will be set in the Interrupt Status Register 1.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See Auto Fan Control Operating Mode on page 134.

There are Remote Diode (1 or 2) Fault status bits in Interrupt Status Register 2 (42h), which, when one, indicate a short or open-circuit on remote thermal diode inputs (Remote x+ and Remote x-). Before a remote diode conversion is updated, the status of the remote diode is checked. In the case of a short or open-circuit on the remote thermal diode inputs, the value in the corresponding reading register will be forced to 80h. Note that this will cause the associated remote diode limit exceeded status bit to be set (i.e. Remote Diode x Limit Error bits (D1 and D2) are located in the Interrupt Status 1 Register at register address 41h).

The temperature change is computed by measuring the change in Vbe at two different operating points of the diode to which the Remote x+ and Remote x- pins are connected. But accuracy of the measurement also depends on non-ideality factor of the process the diode is manufactured on.

21.11.3 TEMPERATURE DATA FORMAT

Temperature data can be read from the three temperature registers:

- Internal Temp Reading register (26h)
- Remote Diode 1 Temp Reading register (25h)
- Remote Diode 2 Temp Reading register (27h)

The following table shows several examples of the format of the temperature digital data, represented by an 8-bit, two's complement word with an LSB equal to 1.0 ^{0}C.

TABLE 21-3: TEMPERATURE DATA FORMAT

Temperature	Reading (DEC)	Reading (HEX)	Digital Output
-127^{0}C	-127	81h	1000 0001
⋮	⋮	⋮	⋮
-50 ^{0}C	-50	CEh	1100 1110
⋮	⋮	⋮	⋮
-25 ^{0}C	-25	E7h	1110 0111
⋮	⋮	⋮	⋮
-1 ^{0}C	-1	FFh	1111 1111

22.2.4 REGISTERS 28-2DH: FAN TACHOMETER READING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
28h	R	FANTACH1 LSB	7	6	5	4	3	2	1	0	FFh
29h	R	FANTACH1 MSB	15	14	13	12	11	10	9	8	FFh
2Ah	R	FANTACH2 LSB	7	6	5	4	3	2	1	0	FFh
2Bh	R	FANTACH2 MSB	15	14	13	12	11	10	9	8	FFh
2Ch	R	FANTACH3 LSB	7	6	5	4	3	2	1	0	FFh
2Dh	R	FANTACH3 MSB	15	14	13	12	11	10	9	8	FFh

This register is reset to its default value when PWRGD_PS is asserted.

The Fan Tachometer Reading registers contain the number of 11.111µs periods (90KHz) between full fan revolutions. Fans produce two tachometer pulses per full revolution. These registers are updated at least once every second.

This value is represented for each fan in a 16 bit, unsigned number.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, including when the start bit=0.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

These registers are read only – a write to these registers has no effect.

22.2.5 REGISTERS 30-32H: CURRENT PWM DUTY

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
30h	R/W (Note 22-12)	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
31h	R/W (Note 22-12)	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
32h	R/W (Note 22-12)	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A

Note 22-12 These registers are only writable when the associated fan is in manual mode. These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Current PWM Duty registers store the duty cycle that the chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start Register Start bit is set, this register and the PWM signals are updated based on the algorithm described in the Auto Fan Control Operating Mode section and the Ramp Rate Control logic, unless the associated fan is in manual mode – see below.

Note: When the device is configured for Manual Mode, the Ramp Rate Control logic should be disabled.

When read, the Current PWM Duty registers return the current PWM duty cycle for the respective PWM signal.

These registers are read only – a write to these registers has no effect.

Note: If the current PWM duty cycle registers are written while the part is not in manual mode or when the start bit is zero, the data will be stored in internal registers that will only be active and observable when the start bit is set and the fan is configured for manual mode. While the part is not in manual mode and the start bit is zero, the current PWM duty cycle registers will read back FFh.

Manual Mode (Test Mode)

In manual mode, when the start bit is set to 1 and the lock bit is 0, the current duty cycle registers are writeable to control the PWMs.

Note:	When the lock bit is set to 1, the current duty cycle registers are Read-Only.

The PWM duty cycle is represented as follows:

TABLE 22-4: PWM DUTY VS REGISTER READING

Current Duty	Value (Decimal)	Value (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

During spin-up, the PWM duty cycle is reported as 0%.

Note 1: The PWMx Current Duty Cycle always reflects the current duty cycle on the associated PWM pin.

2: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

22.2.6 REGISTER 3DH: DEVICE ID

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Dh	R	Device ID	7	6	5	4	3	2	1	0	8Ch

The Device ID register contains a unique value to allow software to identify which device has been implemented in a given system.

22.2.7 REGISTER 3EH: COMPANY ID

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	5Ch

The company ID register contains a unique value to allow software to identify Microchip devices that been implemented in a given system.

22.2.8 REGISTER 3FH: REVISION

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Fh	R	Revision	7	6	5	4	3	2	1	0	01h

The Revision register contains the current version of this device.

The register is used by application software to identify which version of the device has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-arounds for bugs found in a specific silicon stepping.

This register is read only – a write to this register has no effect.

TABLE 23-6: LOGICAL DEVICE REGISTERS (CONTINUED)

Logical Device Register	Address	Description
Interrupt Select Defaults: 0x70 = 0x00 or 0x06 (Note 23-6) on VCC POR, VTR POR, PCI RESET and SOFT RESET 0x72 = 0x00, on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x70,0x72)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the keyboard controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.
DMA Channel Select Default = 0x02 or 0x04 (Note 23-6) on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x74,0x75)	Only 0x74 is implemented for Parallel port. 0x75 is not implemented and ignores writes and returns zero when read. Refer to DMA Channel Configuration.
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device Configuration	(0xE0-0xFE)	Reserved – Vendor Defined (see MCHP defined Logical Device Configuration Registers).
Reserved	0xFF	Reserved

Note 23-4 A logical device will be active and powered up according to the following equation unless otherwise specified:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).

The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.

Note 23-5 If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note 23-6 The default value of the DMA Channel Select register for logical devices 3 and 5 is 0x04.

TABLE 23-7: BASE I/O RANGE FOR LOGICAL DEVICES

Logical Device Number	Logical Device	Register Index	Base I/O Range (Note 23-7)	Fixed Base Offsets
0x00	Reserved	n/a	n/a	n/a
0x01	Reserved	n/a	n/a	n/a
0x02	Reserved	n/a	n/a	n/a
0x03	Parallel Port	0x60,0x61	[0x0100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
			(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SMI_STS3 Default = 0x00 on VTR POR	16 (R/WC)	SMI Status Register 3 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] GP54 Bit[4] GP55 Bit[5] GP56 Bit[6] GP57 Bit[7] GP60
SMI_STS4 Default = 0x00 on VTR POR (Note 24-22) (SCH3224)	17 (R/WC)	SMI Status Register 4 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] RESERVED Bit[1] RESERVED Bit[2] GP32 Bit[3] GP33 Bit[4] U5INT Bit[5] GP42 Bit[6] U5INT Bit[7] GP61
SMI_STS4 Default = 0x00 on VTR POR (Note 24-22) (All except SCH3224)	17 (R/WC)	SMI Status Register 4 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] U3INT Bit[1] U4INT Bit[2] GP32 Bit[3] GP33 Bit[4] U5INT (RESERVED if SCH3227/SCH3226 and STRAPOPT=0) Bit[5] GP42 Bit[6] U6INT (RESERVED if SCH3227/SCH3226 and STRAPOPT=0) Bit[7] GP61
SMI_EN1 Default = 0x00 On VTR POR	18 (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the group nIO_SMI output. 1=Enable 0=Disable Bit[0] EN_LOW_BAT Bit[1] EN_PINT Bit[2] EN_U2INT Bit[3] EN_U1INT Bit[4] EN_FINT Bit[5] Reserved Bit[6] Reserved Bit[7] EN_WDT
SMI_EN2 Default = 0x00 on VTR POR	19 (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the group nSMI output, and the group nSMI output onto the nIO_SMI GPI/O pin, the serial IRQ stream or into the PME Logic. Unless otherwise noted, 1=Enable 0=Disable Bit[0] EN_MINT Bit[1] EN_KINT Bit[2] EN_IRINT Bit[3] Reserved Bit[4] EN_SPESME Bit[5] EN_SMI_PME (Enable group SMI into PME logic) Bit[6] EN_SMI_S (Enable group SMI onto serial IRQ) Bit[7] EN_SMI (Enable group SMI onto nIO_SMI pin)

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP21 Default =0x8C on VTR POR	2C (R/W)	General Purpose I/O bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KDAT (Default) 10=Either Edge Triggered Interrupt Input 0 (Note 24-20) 01=Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull (Default) **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KDAT function, bit[0] should always be programmed to '0'. The KDAT function will not operate properly when bit[0] is set.
GP22 Default =0x8C on VTR POR	2D (R/W)	General Purpose I/O bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KCLK (Default) 10=Either Edge Triggered Interrupt Input 1 (Note 24-20) 01= Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KCLK function, bit[0] should always be programmed to '0'. The KCLK function will not operate properly when bit[0] is set.
UART5 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2E (R)	Bits[7:0] RESERVED
UART5 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2E (R)	UART FIFO Control Shadow 5 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
UART6 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2F (R)	Bits[7:0] RESERVED
UART6 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2F (R)	Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

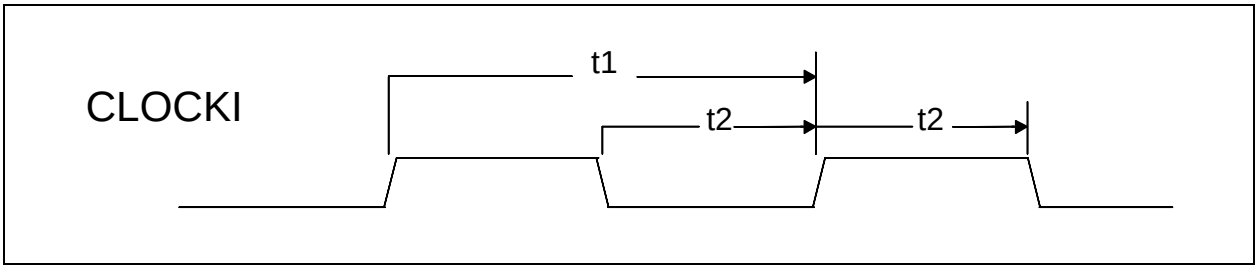
Name	REG Offset (HEX)	Description
GP42 Default =0x01 on VTR POR	3D (R/W)	General Purpose I/O bit 4.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_PME **Note:** Configuring this pin function as output with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP50 Default = 0x01 on VTR POR	3F (R/W)	General Purpose I/O bit 5.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nRI2 (Note 24-18) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP51 Default = 0x01 on VTR POR	40 (R/W)	General Purpose I/O bit 5.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDCD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP52 Default = 0x01 on VTR POR	41 (R/W)	General Purpose I/O bit 5.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=RXD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP53 Default = 0x01 on VTR POR	42 (R/W)	General Purpose I/O bit 5.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=TXD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP54 Default = 0x01 on VTR POR	43 (R/W)	General Purpose I/O bit 5.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDSR2 0=GPIO Bit[3] RESERVED Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP55 Default = 0x01 on VTR POR	44 (R/W)	General Purpose I/O bit 5.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nRTS2 0=GPIO Bit[3] RESERVED Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP56 Default = 0x01 on VTR POR	45 (R/W)	General Purpose I/O bit 5.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nCTS2 0=GPIO Bit[3] RESERVED Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP57 Default = 0x01 on VTR POR	46 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDTR2 0=GPIO Bit[3] RESERVED Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP60 Default = 0x01 on VTR POR	47 (R/W)	General Purpose I/O bit 6.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=WDT 10=Either Edge Triggered Interrupt Input 4 (Note 24-20) 01=LED1 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

27.2 Input Clock Timing

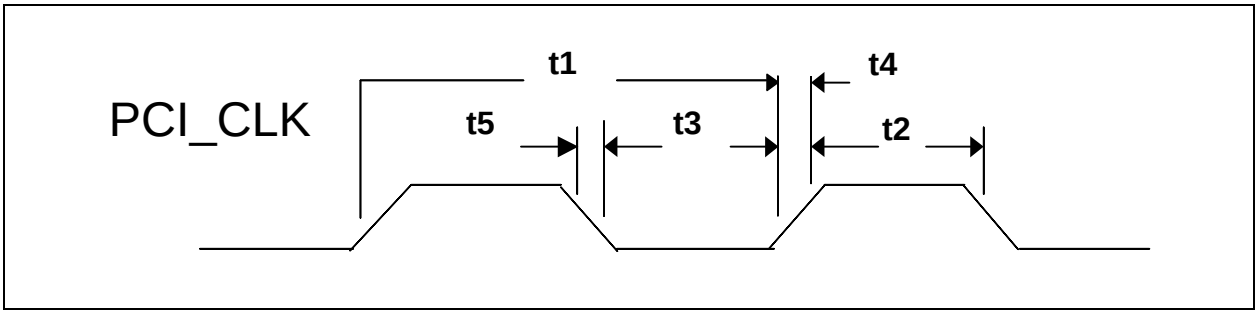
FIGURE 27-2: INPUT CLOCK TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

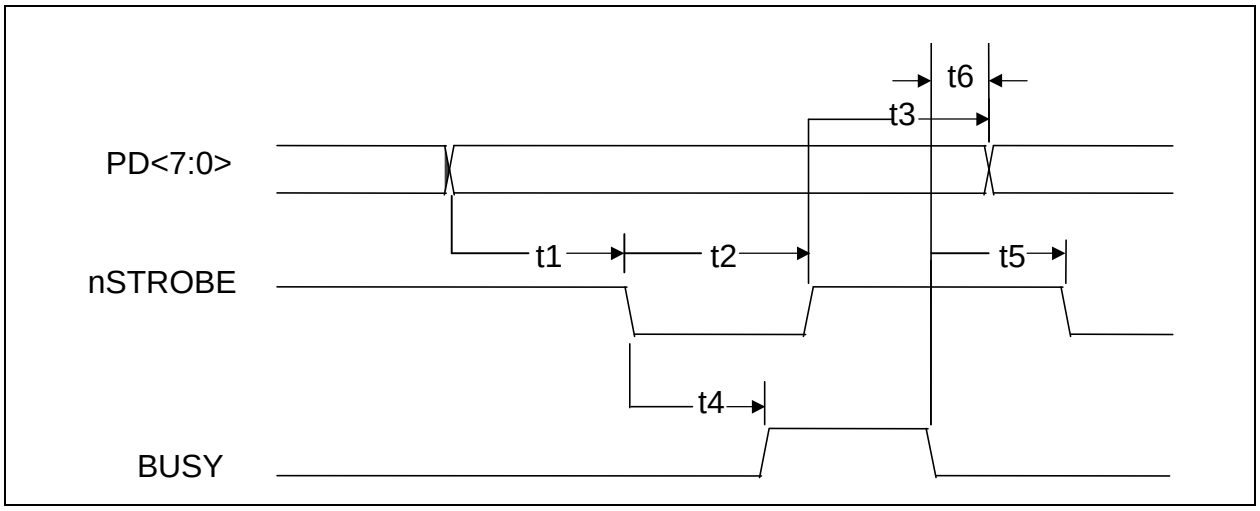
27.3 LPC Interface Timing

FIGURE 27-3: PCI CLOCK TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

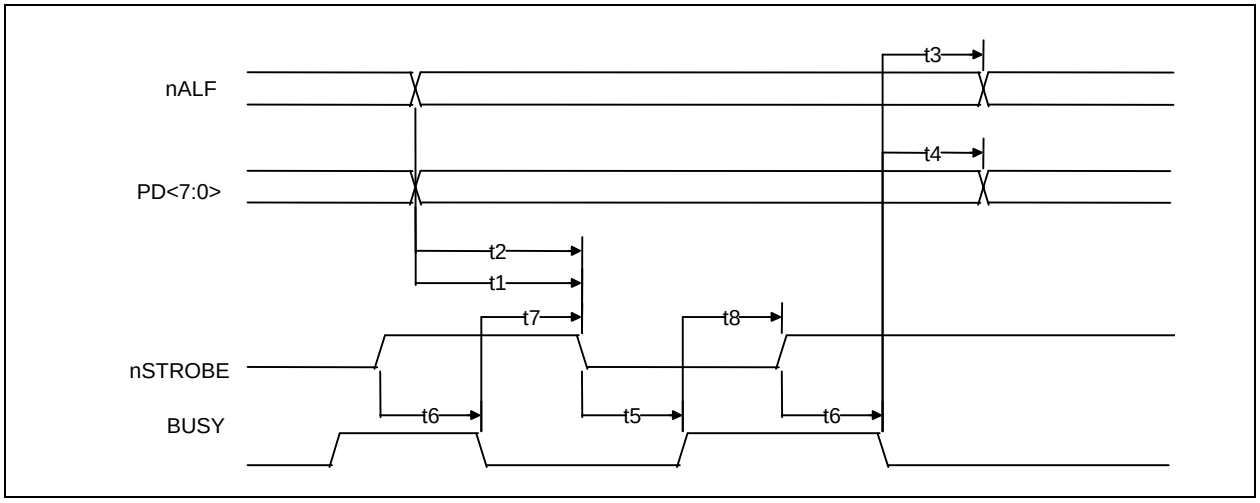
FIGURE 27-16: PARALLEL PORT FIFO TIMING



Name	Description	MIN	TYP	MAX	Units
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (See Note 27-3)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (See Note 27-3)	80			ns

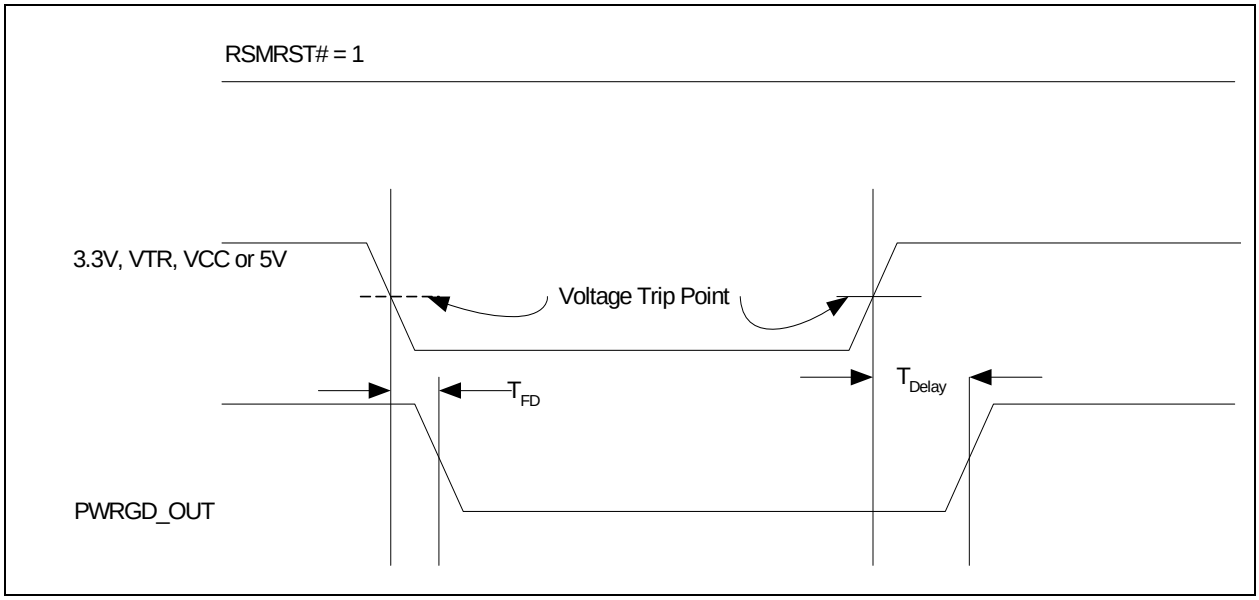
Note 27-3 The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

FIGURE 27-17: ECP PARALLEL PORT FORWARD TIMING



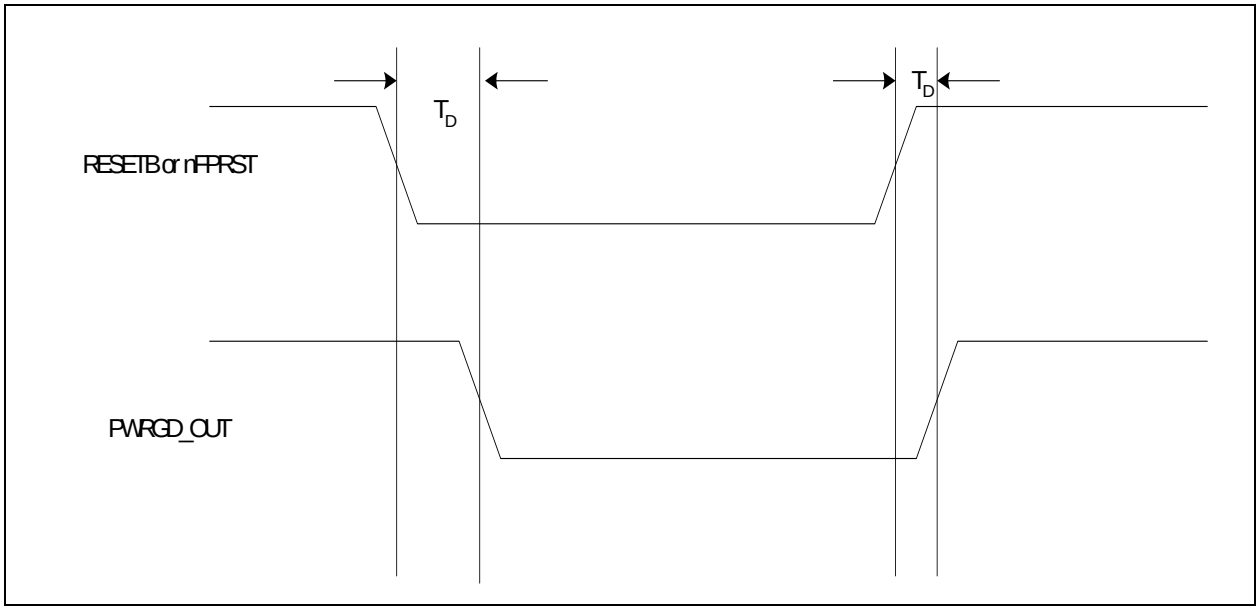
27.10 PWRGD_OUT Signal Generation

FIGURE 27-27: PWRGD_OUT TIMING VS. VOLTAGE 3.3V OR 5V DROP



Symbol	Time			Description
	MIN	TYP	MAX	
T_{Delay}	188ms	200ms	212ms	The delay time is from the rising voltage trip voltage to the rising edge of PWRGD_OUT. This delay is selected via a strapping option. Default value is 200ms.
	470ms	500ms	530ms	
T_{FD}	3ηs		20ηs	

For 3.3V and 5V trip points refer to Table 26-3, “Reset Generators,” on page 259.



Symbol	Time			Description
	MIN	TYP	MAX	
T_D	0	1.6ms	2.0ms	Debounce Delay

APPENDIX D: DATA SHEET REVISION HISTORY

TABLE D-1: SCH3227/SCH3226/SCH3224/SCH3222 REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002121B (03-20-17)	Figure 2-2, "SCH3226 Pin Diagram" and Figure 2-3, "SCH3224 Pin Diagram"	Updated diagrams
	Table 2-2, "SCH3226 Summaries By Strap Option", Table 2-3, "SCH3224 Summary" and Table 2-4, "SCH3222 Summary"	Added footnote to pin TEST, indicating that a connection to VSS is necessary.
DS00002121A (03-02-16)	Document Release	