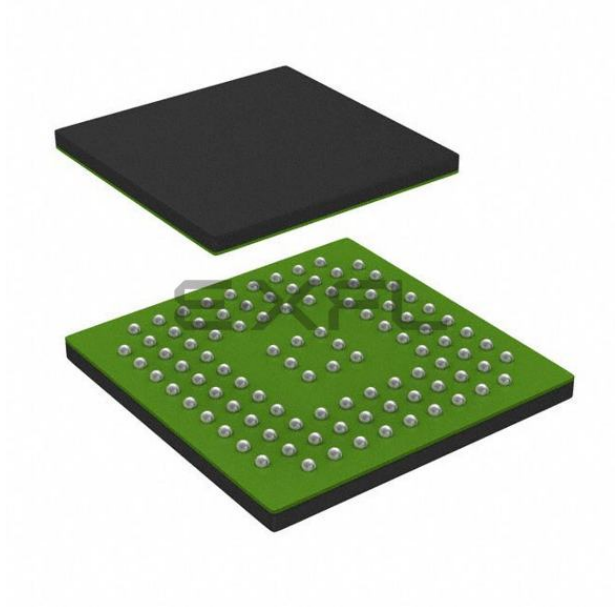


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	24
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3224i-sy-tr

TABLE 11-1: GPIO PIN FUNCTIONALITY (CONTINUED)

GPIO Pin Name (Default Func/ Alternate Funcs)	GPIO PWRWELL	VTR POR	SMI/PME	Note
nPCI_RST1 / GP45 GP45 / RXD6	VTR	0x01		11-3
nPCI_RST2 / GP46 GP46 / nSCIN6	VTR	0x01	PME	11-3, 11-4
nPCI_RST3 / GP47 GP47 / nSCOUT6	VTR	0x01		11-3
GP50/nRI2	VCC	0x01	PME	11-1
GP51/nDCD2	VCC	0x01	PME	11-1
GP52/RXD2(IRRX)	VCC	0x01	PME	11-1
GP53/TXD2 (IRTX)	VCC	0x01	PME	11-1
GP54/nDSR2	VCC	0x01	SMI/PME	11-1
GP55/nRTS2	VCC	0x01	SMI/PME	11-1
GP56/nCTS2	VCC	0x01	SMI/PME	11-1
GP57/nDTR2	VCC	0x01	SMI/PME	11-1
GP60/nLED1/WDT	VTR	0x01	SMI/PME	11-1
GP61/nLED2/ CLKO	VTR	0x01	SMI/PME	11-1
GP62 GP62 / nCTS4	VTR	0x01		11-3
GP63 GP63 / nDCD4	VTR	0x01		11-3
GP64 GP64 / RXD4	VTR	0x01		11-3
GP65 GP65 / TXD4	VTR	0x01		11-3
GP66 GP66 / nDCR4	VTR	0x01		11-3
GP67 GP67 / nRTS4	VTR	0x01		11-3

Note 11-1 These pins are inputs to VCC and VTR powered logic. The logic for the GPIO is on VCC - it is also a wake event which goes to VTR powered logic.

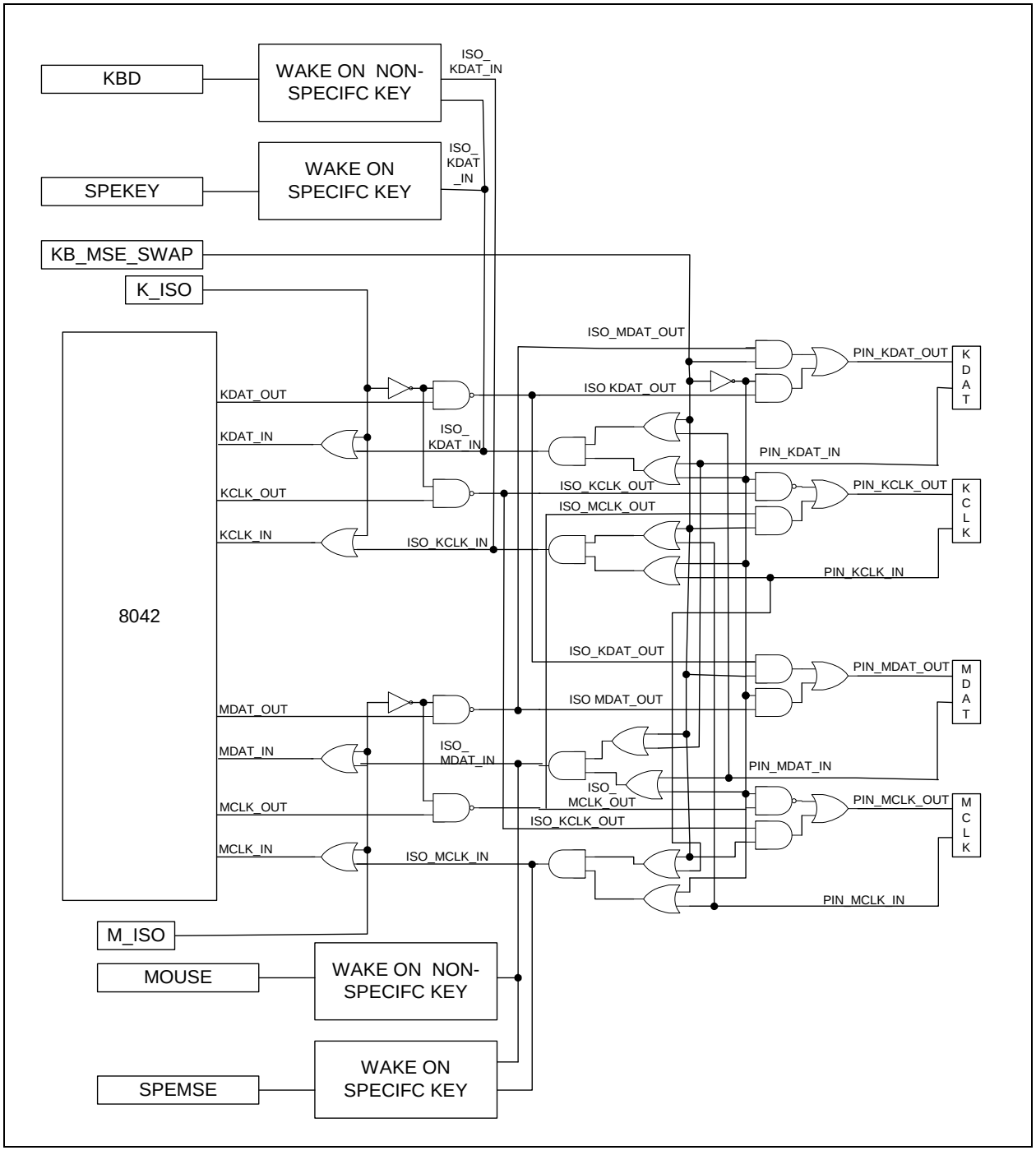
Note 11-2 This pin's primary function (power up default function) is not GPIO function; however, the pin can be configured a GPIO Alternate function.

Note 11-3 Not all pins are available in all family members. Also, in some cases incorrect usage can cause damage. See the CAUTION note at the beginning of this chapter: Section 11.0, General Purpose I/O (GPIO).

Note 11-4 The PME is for the RI signal only. Note that this may not be available for all SCH322x devices. Refer to Table 11-2, "SCH322x General Purpose I/O Port Assignments," on page 88 for more details.

Note 11-5 This pin is an OD type buffer in output mode. It cannot be configured as a Push-Pull Output buffer

FIGURE 13-1: 8042 ISOLATION AND KEYBOARD AND MOUSE PORT SWAP REPRESENTATION



Note: This figure is for illustration purposes only and not meant to imply specific implementation details.

15.0 PROGRAMMABLE CLOCK OUTPUT

A CLK_OUT pin is available on the SCH322x. This will output a programmable frequency between 0.5 Hz to 16 Hz, and have the following characteristics:

- Must run when Vcc if off - could use 32Khz clock
- Accuracy is not an issue
- CLOCK_OUT register at offset 3Ch in runtime registers with the following programming:
  - Options for 0.25, 0.5, 1, 2, 4, 8, or 16 Hz

APPLICATION NOTE: No attempt has been made to synchronize the clock. As a result, glitches will occur on the clock output when different frequencies are selected.

CLOCK Output Control Register VTR POR = 0x00	3C (R/W)	Bit[0] Enable 1= Output Enabled 0= Disable Clock output Bit[3:1] Frequency Select 000= 0.25 Hz 001= 0.50 Hz 010= 1.00 Hz 011= 2.00 Hz 100= 4.00 Hz 101= 8.00 Hz 110= 16 hz 111 = reserved Bit[7:4] Reserved

18.1 nIO_PME Pin use in Power Control

The nIO_PME signal can be used to control the state of the power supply. The nIO_PME signal will be asserted when a PME event occurs and the PME logic is enabled. The following is a summary of the Power control PME events (See Figure 18-1):

1. PB_IN# input signal assertion.
2. When the Wake On Specific Key Logic detects the programmed keyboard event it will generate a wake event (KB_PB_STS).
3. Upon returning from a power failure.

Each PME wake event sets a status bit in the PME_STS6 register. If the corresponding enable bit in the PME_EN6 register is set then the nIO_PME pin will be asserted. The enable bits in the PME_EN6 register default to set and are Vbat powered. Refer to Section 13.0, "PME Support," on page 94 for description of the PME support for this PME event.

18.2 Front Panel Reset

The inputs, PWRGD_PS and nFPRST have hysteresis and are internally pulled to VTR through a 30uA resistor. The nFPRST is debounced internally.

The nFPRST input has internal debounce circuitry that is valid on both edges for at least 16ms before the output is changed. The 32.768kHz is used to meet the timing requirement. See Figure 18-2 for nFPRST debounce timing.

The actual minimum debounce time is 15.8msec

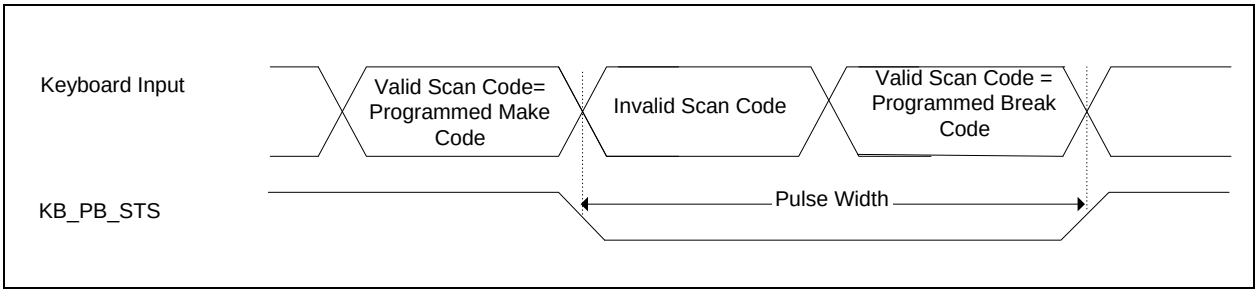
The 32.768 kHz trickle input **must** be connected to supply the clock signal for the nFPRST debounce circuitry. The SCH322x has a legacy feature which is incompatible with use of the nFPRST input signal. An internal 32kHz clock source derived from the 14MHz (VCC powered) can be selected when the external 32kHz clock is not connected.

APPLICATION NOTE: The 32.768 kHz trickle input must be connected to supply the clock signal for the nFPRST debounce circuitry.

TABLE 18-2: INTERNAL PWROK TRUTH TABLE

Inputs		Output
nFPRST	**PWRGD_PS**	**Internal PWROK**
0	0	0
0	1	0
1	0	0
1	1	1

FIGURE 18-10: OPTION 3: DE-ASSERT KB_PB_STS WHEN SCAN CODE EQUAL BREAK CODE.



Note: The SPEKEY ScanCode bits are located in the register Keyboard PWRBTN/SPEKEY located at offset 64h.

TABLE 18-5: DECODING KEYBOARD SCAN CODE FOR BREAK CODE

SPEKEY Scan Code		Scan Code	Number of Bytes in Break Code	Description
Bit[3]	Bit[2]			
0	0	Scan 1	1 Byte	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit.
0	1	Scan 1	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.
1	0	Scan 2	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.

21.4.2 VCC POWER-ON RESET

The PWRGD_PS signal is used by the hardware-monitoring block to determine when a VCC POR has occurred. The PWRGD_PS signal indicates that the VCC power supply is within operation range and the 14.318MHz clock source is valid.

Note: Throughout the description of the hardware monitoring block VCC POR and PWRGD_PS are used interchangeably, since the PWRGD_PS is used to generate a VCC POR.

All the HWM registers will retain their value through a sleep cycle unless otherwise specified. If a VCC POR is preceded by a VTR POR the registers will be reset to their default values. The following is a list of the registers and bits that are reset to their default values following a VCC POR.

- FANTACH1 LSB register at offset 28h
- FANTACH1 MSB register at offset 29h
- FANTACH2 LSB register at offset 2Ah
- FANTACH2 MSB register at offset 2Bh
- FANTACH3 LSB register at offset 2Ch
- FANTACH3 MSB register at offset 2Dh
- Bit[1] LOCK of the Ready/Lock/Start register at offset 40h
- Zone 1 Low Temp Limit at offset 67h
- Zone 2 Low Temp Limit at offset 68h
- Zone 3 Low Temp Limit at offset 69h
- Bit[3] TRDY of the Configuration register at offset 7Fh
- Top Temperature Remote diode 1 (Zone 1) register at offset AEh
- Top Temperature Remote diode 2 (Zone 3) register at offset AFh
- Top Temperature Ambient (Zone 2) register at offset B3h

21.4.3 SOFT RESET (INITIALIZATION)

Setting bit 7 of the Configuration Register (7Fh) performs a soft reset on all the Hardware Monitoring registers except the reading registers. This bit is self-clearing.

21.5 Clocks

The hardware monitor logic operates on a 90kHz nominal clock frequency derived from the 14MHz clock input to the SIO block. The 14MHz clock source is also used to derive the high PWM frequencies.

21.6 Input Monitoring

The SCH322x device's monitoring function is started by writing a '1' to the START bit in the **Ready/Lock/Start** Register (0x40). Measured values from the temperature sensors are stored in Reading Registers. The values in the reading registers can be accessed via the LPC interface. These values are compared to the programmed limits in the Limit Registers. The out-of-limit and diode fault conditions are stored in the Interrupt Status Registers.

Note: All limit and parameter registers must be set before the START bit is set to '1'. Once the start bit is set, these registers become read-only.

21.7 Monitoring Modes

The Hardware Monitor Block supports two Monitoring modes: Continuous Mode and Cycle Mode. These modes are selected using bit 1 of the Special Function Register (7Ch). The following subsections contain a description of these monitoring modes.

The time to complete a conversion cycle depends upon the number of inputs in the conversion sequence to be measured and the amount of averaging per input, which is selected using the AVG[2:0] bits in the Special Function register (see the Special Function Register, 7Ch).

For each mode, there are four options for the number of measurements that are averaged for each temperature reading. These options are selected using bits[7:5] of the Special Function Register (7Ch). These bits are defined as follows:

21.11 Temperature Measurement

Temperatures are measured internally by bandgap temperature sensor and externally using two sets of diode sensor pins (for measuring two external temperatures). See subsections below.

Note: The temperature sensing circuitry for the two remote diode sensors is calibrated for a 3904 type diode.

21.11.1 INTERNAL TEMPERATURE MEASUREMENT

Internal temperature can be measured by bandgap temperature sensor. The measurement is converted into digital format by internal ADC. This data is converted in two's complement format since both negative and positive temperature can be measured. This value is stored in Internal Temperature Reading register (26h) and compared to the Temperature Limit registers (50h – 51h). If this value violates the programmed limits in the Internal High Temperature Limit register (51h) and the Internal Low Temperature Limit register (50h) the corresponding status bit in Interrupt Status Register 1 is set.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled Auto Fan Control Operating Mode on page 134.

21.11.2 EXTERNAL TEMPERATURE MEASUREMENT

The Hardware Monitor Block also provides a way to measure two external temperatures using diode sensor pins (Remote x+ and Remote x-). The value is stored in the register (25h) for Remote1+ and Remote1- pins. The value is stored in the Remote Temperature Reading register (27h) for Remote2+ and Remote2- pins. If these values violate the programmed limits in the associated limit registers, then the corresponding Remote Diode 1 (D1) or Remote Diode 2 (D2) status bits will be set in the Interrupt Status Register 1.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See Auto Fan Control Operating Mode on page 134.

There are Remote Diode (1 or 2) Fault status bits in Interrupt Status Register 2 (42h), which, when one, indicate a short or open-circuit on remote thermal diode inputs (Remote x+ and Remote x-). Before a remote diode conversion is updated, the status of the remote diode is checked. In the case of a short or open-circuit on the remote thermal diode inputs, the value in the corresponding reading register will be forced to 80h. Note that this will cause the associated remote diode limit exceeded status bit to be set (i.e. Remote Diode x Limit Error bits (D1 and D2) are located in the Interrupt Status 1 Register at register address 41h).

The temperature change is computed by measuring the change in Vbe at two different operating points of the diode to which the Remote x+ and Remote x- pins are connected. But accuracy of the measurement also depends on non-ideality factor of the process the diode is manufactured on.

21.11.3 TEMPERATURE DATA FORMAT

Temperature data can be read from the three temperature registers:

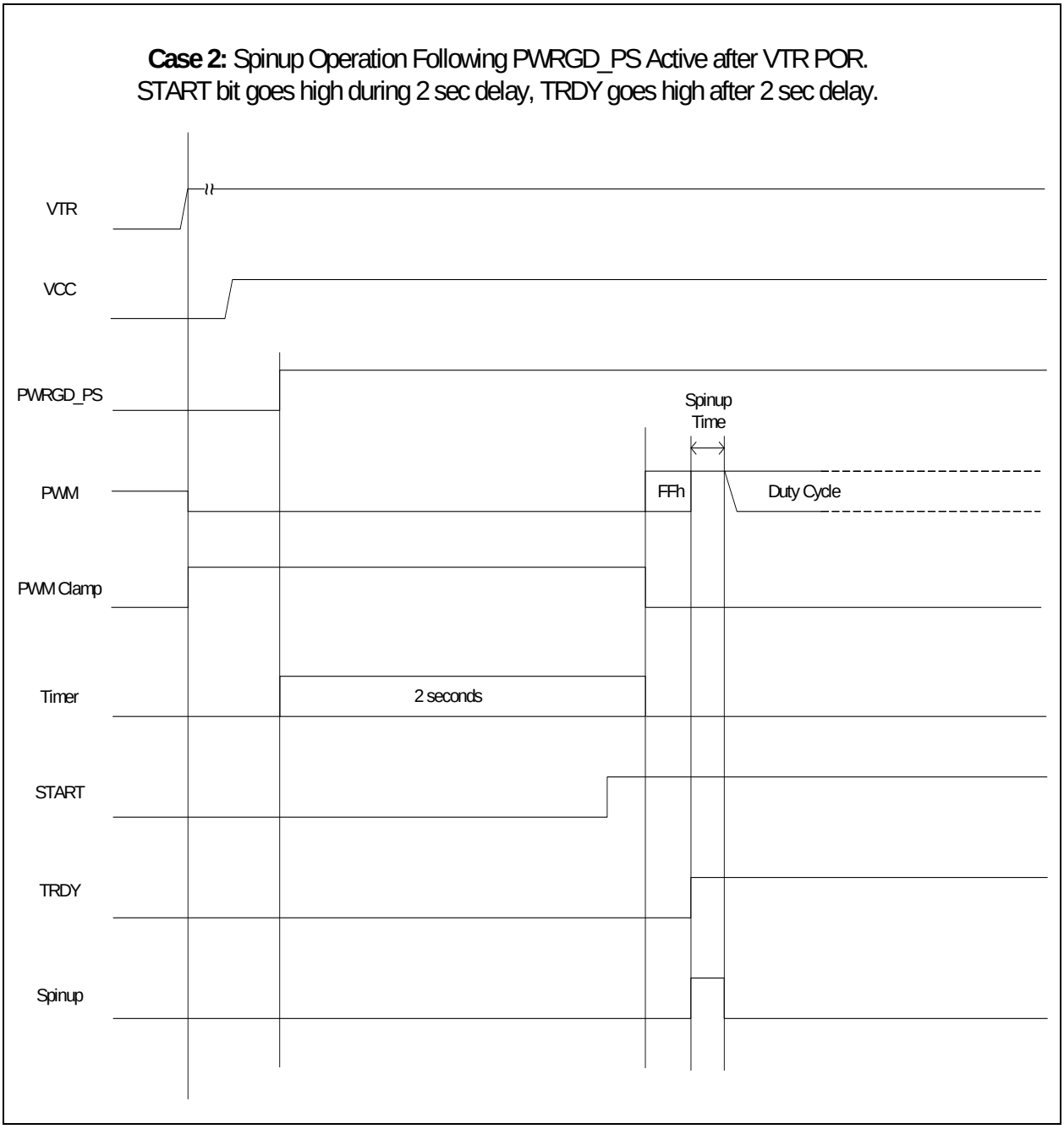
- Internal Temp Reading register (26h)
- Remote Diode 1 Temp Reading register (25h)
- Remote Diode 2 Temp Reading register (27h)

The following table shows several examples of the format of the temperature digital data, represented by an 8-bit, two's complement word with an LSB equal to 1.0 ^{0}C.

TABLE 21-3: TEMPERATURE DATA FORMAT

Temperature	Reading (DEC)	Reading (HEX)	Digital Output
-127^{0}C	-127	81h	1000 0001
⋮	⋮	⋮	⋮
-50 ^{0}C	-50	CEh	1100 1110
⋮	⋮	⋮	⋮
-25 ^{0}C	-25	E7h	1110 0111
⋮	⋮	⋮	⋮
-1 ^{0}C	-1	FFh	1111 1111

FIGURE 21-9: CASE 2 SPINUP OPERATION



3: The fan tachometer reading register stays at FFFFh in the event of a stalled fan. If the fan begins to spin again, the tachometer logic will reset and latch the next valid reading into the tachometer reading register.

21.14.2.11 Fan Interrupt Status Bits

The status bits for the fan events are in Interrupt Status Register 2 (42h). These bits are set when the reading register is above the tachometer minimum and the Interrupt Enable 2 (Fan Tachs) register bits are configured to enable Fan Tach events. No interrupt status bits are set for fan events (even if the fan is stalled) if the associated tachometer minimum is set to FFFFh (registers 54h-5Bh).

Note:	The Interrupt Enable 2 (Fan Tachs) register at offset 80h defaults to enabled for the individual tachometer status events bits. The group Fan Tach nHWM_INT bit defaults to disabled. This bit needs to be set if Fan Tach interrupts are to be generated on the external nHWM_INT pin.

See FIGURE 21-3: Interrupt Control on page 128.

21.14.3 LOCKED ROTOR SUPPORT FOR TACHOMETER INPUTS

All tachometer inputs support locked rotor input mode. In this mode, the tachometer input pin is not used as a tachometer signal, but as a level signal. The active state of this signal (high or low) is the state that the fan's locked rotor signal indicates the locked condition.

The locked rotor signals that are supported are active high level and active low level. They are selectable for each tachometer. If the pin goes to its programmed active state, the associated interrupt status bit will be set. In addition, if properly configured, the nHWM_INT pin can be made to go active when the status bit is set.

The locked rotor input option is configured through the following bits:

- Tach1 Mode, bits[7:6] of Tach 1-3 Mode register
- Tach2 Mode, bits[5:4]of Tach 1-3 Mode register
- Tach3 Mode, bit[3:2] of Tach 1-3 Mode register

These bits are defined as follows:

- 00=normal operation (default)
- 01=locked rotor mode, active high signal
- 10=locked rotor mode, active low signal
- 11=undefined

21.14.4 LINKING FAN TACHOMETERS TO PWMS

The TACH/PWM Association Register at offset 81h is used to associate a Tachometer input with a PWM output. This association has three purposes:

1. The auto fan control logic supports a feature called SpinUp Reduction. If SpinUp Reduction is enabled (SUREN bit), the auto fan control logic will stop driving the PWM output high if the associated TACH input is operating within normal parameters. (Note: SUREN bit is located in the Configuration Register at offset 7Fh)
2. To measure the tachometer input in Mode 2, the tachometer logic must know when the associated PWM is 'ON'.
3. Inhibit fan tachometer interrupts when the associated PWM is 'OFF'.

See the description of the PWM_TACH register. The default configuration is:

PWM1 -> FANTACH1

PWM2 -> FANTACH2

PWM3 -> FANTACH3

Note:	If a FANTACH is associated with a PWM operating in high frequency mode (see the Zonex Range/FANx Frequency registers (5Fh-61h)) the tach monitoring logic must be configured for Mode 1 (see Bit[3] Mode in FANTACHx Option Registers, 90h-92h).

22.2.3 REGISTERS 25-27H: TEMPERATURE READING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
25h	R	Remote Diode 1 (Zone 1) Temp Reading	7	6	5	4	3	2	1	0	N/A
26h	R	Internal Diode (Zone 2) Temp Reading	7	6	5	4	3	2	1	0	N/A
27h	R	Remote Diode 2 (Zone 3) Temp Reading	7	6	5	4	3	2	1	0	N/A

The Temperature Reading registers reflect the current temperatures of the internal and remote diodes. Remote Diode 1 Temp Reading register reports the temperature measured by the Remote1- and Remote1+ pins, Remote Diode 2 Temp Reading register reports the temperature measured by the Remote2- and Remote2+ pins, and the Internal Diode Temp Reading register reports the temperature measured by the internal (ambient) temperature sensor. Current temperatures are represented as 12 bit, 2's complement, signed numbers in Celsius. The 8MSbs are accessible in the temperature reading registers. Table 22-3 shows the conversion for the 8-bit reading value shown in these registers. The extended precision bits for these readings are accessible in the A/D Converter LSBs Register (85h-86h). The Temperature Reading register will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly (this corresponds to the diode fault interrupt status bits). The Temperature Reading registers will be updated automatically by the SCH322x Chip with a minimum frequency of 4Hz.

Note: These registers are read only – a write to these registers has no effect.

Each of the temperature reading registers are mapped to a zone. Each PWM may be programmed to operate in the auto fan control operating mode by associating a PWM with one or more zones. The following is a list of the zone associations.

- Zone 1 is controlled by Remote Diode 1 Temp Reading
- Zone 2 is controlled by Internal Temp Reading (Ambient Temperature Sensor)
- Zone 3 is controlled by Remote Diode 2 Temp Reading

Note: To read a 12-bit reading value, software must read in the order of MSB then LSB. If several readings are being read at the same time, software can read all the MSB registers then the corresponding LSB registers. For example: Read RD1 Reading, RD2 Reading, then A/D Converter LSbs Reg1, which contains the LSbs for RD1 and RD2.

TABLE 22-3: TEMPERATURE VS. REGISTER READING

Temperature	Reading (DEC)	Reading (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh
(SENSOR ERROR)		80h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

22.2.36 REGISTERS 8CH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ch	R	MCHP Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	0Eh

22.2.37 REGISTERS 8DH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Dh	R/W	MCHP Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	0Eh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

22.2.38 REGISTERS 8EH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Eh	R	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an MCHP Test register.

22.2.39 REGISTERS 90H-92H: FANTACHX OPTION REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
90h	R/W	FANTACH1 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
91h	R/W	FANTACH2 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
92h	R/W	FANTACH3 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bit[0] SLOW

0= Force tach reading register to FFFFh if number of tach edges detected is greater than 0, but less than programmed number of edges. (default)

1= Force tach reading register to FFFEh if number of tach edges detected is greater than 0, but less than programmed number of edges.

Bit[2:1] The number of edges for tach reading:

00= 2 edges

01= 3 edges

10= 5 edges (default)

11= 9 edges

Bit[3] Tachometer Reading Mode

0= mode 1 standard (Default)

1= mode 2 enhanced.

Note 1: Unused FANTACH inputs must be configured for Mode 1.

2: Tach inputs associated with PWM outputs that are configured for high frequency mode must be configured for Mode 1.

23.0 CONFIGURATION REGISTERS

The Configuration of the SCH322x is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The SCH322x is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the SCH322x allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder

After a PCI Reset or Vcc Power On Reset the SCH322x is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the SCH322x into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the SCH322x Is in Configuration Mode.

Strap options must be added to allow four Configuration Register Base Address options: 0x002E, 0x004E, 0x162E, or 0x164E. At the deasserting edge of PCIRST# or VCC POR the nRTS1/SYSOPT0 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[7:0]= 0x2E
- 1 = Index Base I/O Address bits A[7:0]= 0x4E

At the deasserting edge of PCIRST# or VCC POR the nDTR1/SYSOPT1 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[15:8]= 0x16;
- 1 = Index Base I/O Address bits A[15:8]= 0x00

bit The above strap options will allow the Configuration Access Ports (CONFIG PORT, the INDEX PORT, and DATA PORT) to be controlled by the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins and by the Configuration Port Base Address registers at offset 0x26 and 0x27. The configuration base address at power-up is determined by the SYSOPT strap option. The SYSOPT strap option is latched state of the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins at the deasserting edge of PCIRST#. The nRTS1/SYSOPT0 pin determines the lower byte of the Base Address and the nDTR1/SYSOPT1 pin determines the upper byte of the Base Address. The following table summarizes the Base Configuration address selected by the SYSOPT strap option.

TABLE 23-1: SYSOPT STRAP OPTION CONFIGURATION ADDRESS SELECT

SYSOPT1	SYSOPT0	Default CONFIG PORT/ Index Port Address	Data Port
1	0	0x002E	INDEX PORT + 1
1	1	0x004E	
0	0	0x162E	
0	1	0x164E	

APPLICATION NOTE: The nRTS1/SYSOPT0 and the nDTR1/SYSOPT1 pins requires external pullup/pulldown resistors to set the default base I/O address for configuration to 0x002E, 0x004E, 0x162E, or 0x164E.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

Note 23-1 The configuration port base address can be relocated through CR26 and CR27.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

TABLE 23-4: CHIP-LEVEL (GLOBAL) CONFIGURATION REGISTERS (CONTINUED)

Register	Address	Description
Configuration Address Byte 0 Default Sysopt0 = 0 0x2E Sysopt0 = 1 0x4E on VCC POR and PCI RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 (Note 23-3)
Configuration Address Byte 1 Default Sysopt1 = 0 0x16 Sysopt1 = 1 0x00 n VCC POR and PCI RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] Bits[15:21] = 0 (Note 23-3)
Default = 0x00 on VCC POR, SOFT RESET and PCI RESET	0x28	Bits[7:0] Reserved - Writes are ignored, reads return 0.

Note 23-3 To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a PCI Reset or Vcc POR.

Note: The default configuration address is specified in Table 23-1, “SYSOPT Strap Option Configuration Address Select,” on page 194.

23.1.2 TEST REGISTERS

The following test registers are used in the SCH322x devices.

TABLE 23-5: TEST REGISTER SUMMARY

Register	Address	Description
TEST 8 Default = 0x00, on VCC POR and VTR POR	0x19 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 9 Default = 0x00, on VCC POR and VTR POR	0x25 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST Default = 0x00 Note on VTR_POR BIT0/7 are reset BIT1-6 reset on TST_PORB from resgen block	0x29 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PME_STS6 Default = 0x00 or 0x01 on VTR POR The default will be 0x01 if there is a LOW_BAT event under VBAT power only, 0x00 if the event does not occurs. Bit[0] will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	07 (R/WC)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME pin. Bit[0] LOW_BAT, Cleared by a write of '1'. When the battery is removed and replaced or the if the battery voltage drops below 1.2V under battery power, then the LOW_BAT PME status bit is set on VTR POR. When the battery voltage drops below 2.4 volts under VTR power (VCC=0) or under battery power only, the LOW_BAT PME status bit is set on VCC POR. The corresponding enable bit must be set to generate a PME. The low battery event is not a PME wakeup event. Bit[1] RESERVED. Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_STS (Wake on specific mouse click) Bit[5] SPEKEY_STS (Wake on specific key) Bit[6] PB_STS Bit[7] Reserved The PME Status register is not affected by VCC POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Status Register has no effect.
PME_EN1 Default = 0x00 on VTR POR	08 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_EN bit is "1", the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] Reserved Bit[6] IRINT Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PME_EN3 Default = 0x00 on VTR POR	09 (R/W)	PME Wake Status Register 3 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_EN bit is "1", the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] WDT Bit[1] GP21 Bit[2] GP22 Bit[3] DEVINT_EN (Enable bit for group SMI signal for PME) Bit[4] GP27 Bit[5] GP32 Bit[6] GP33 Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
Keyboard Scan Code – Break Byte 2 Default = 0xF0 on Vbat POR	62 (R/W)	Keyboard Scan Code This register is used to decode the second byte received in multi-byte break codes. Bit[0] LSB of Scan Code . . . . Bit[7] MSB of Scan Code **Note:** • The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). • Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.
Keyboard Scan Code – Break Byte 3 (LSB) Default = 0x37 on Vbat POR	63 (R/W)	Keyboard Scan Code This register is used to decode the third byte received in scan 2 multi-byte break codes. Bit[0] LSB of Scan Code . . . . Bit[7] MSB of Scan Code **Note:** • The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). • Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.
Keyboard PWRBTN/SPEKEY Default = 6Ch on Vbat POR Default = 0xxxxxxxb on VTR POR, VCC POR, and PCI Reset Note: The 'x' indicates bit is not affected by reset	64 R/W when Bit [7] is '0' Read Only when Bit [7] is '1'	Bit[0] MCHP Reserved bit. Must be written as a '0'. Bit[1] MCHP Reserved bit. Must be written as a '0'. Bits[3:2] SPEKEY ScanCode. This bit is used to configure the hardware to decode a particular type of scan code. 00 = Single Byte, Scan Code Set 1 (Ex. make=37h and break=B7h) 01 =Multi-Byte, Scan Code Set 1 (Ex. make = E0h, 37h and break = E0h, B7h) 10 = Single Byte, Scan Code Set 2 (Ex. make=37h and break=F0h 37h) 11 = Multi-Byte, Scan Code Set 2 (Ex. make = E0h, 37h and break = E0h F0h 37h) (Default) Bits[5:4] Keyboard Power Button Release These bits are used to determine the pulse width of the Power Button event from the keyboard (KB_PB_STS). The wake on specific key can be configured to generate a PME event and/or power button event. If it is used to generate a power button event, the following bits will determine when the KB_PB_STS event is de-asserted. 00=De-assert KB_PB_STS 0.5sec after it is asserted (default) 01=De-assert KB_PB_STS after any valid scan code NOT EQUAL to the programmed make code. 10=De-assert KB_PB_STS when scan code received is equal to programmed break code 11=Reserved Bit[6] MCHP Reserved bit. Must be written as a '1'.

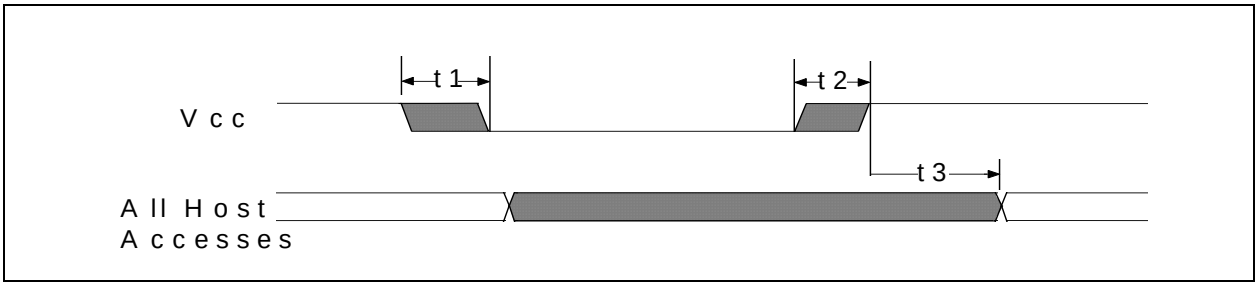
27.0 TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

Name	Capacitance Total (pF)
SER_IRQ	50
LAD [3:0]	50
LDRQ#	50
nDIR	240
nSTEP	240
nDS0	240
PD[0:7]	240
nSTROBE	240
nALF	240
KDAT	240
KCLK	240
MDAT	240
MCLK	240
LED1	50
LED2	50
TXD1	50
TXD2	50
TXD3	50
TXD4	50
TXD5	50
TXD6	50

27.1 Power Up Timing

FIGURE 27-1: POWER-UP TIMING

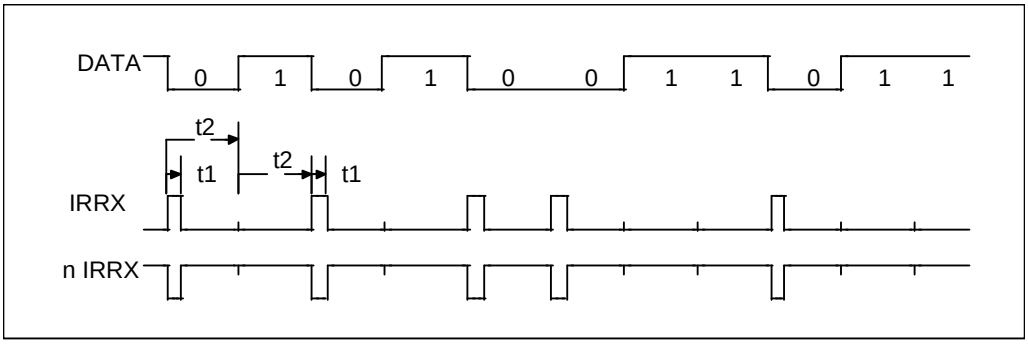


Name	Description	MIN	TYP	MAX	Units
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Power-up (See Note 27-1)	125		500	µs

Note 27-1 Internal write-protection period after Vcc passes 2.7 volts on power-up.

27.5 IR Timing

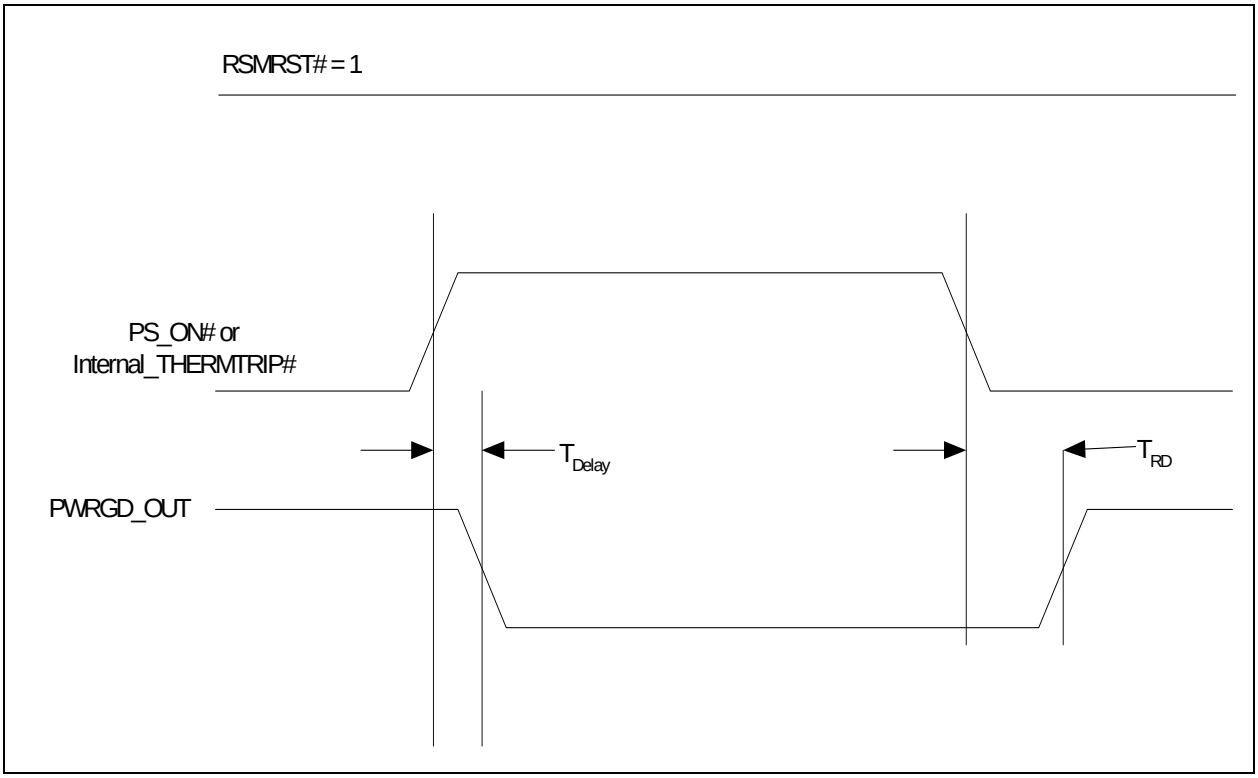
FIGURE 27-19: IRDA RECEIVE TIMING



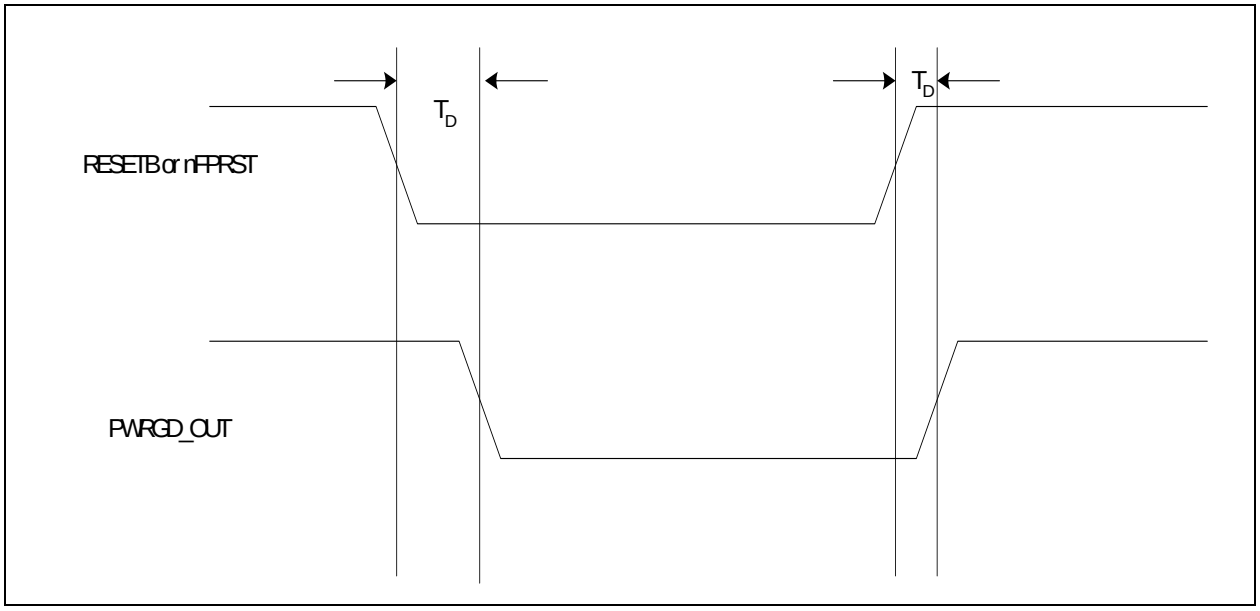
	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

FIGURE 27-28: PWG_OUT VS. PS_ON# SIGNAL NEGATION



Symbol	Time			Description
	MIN	TYP	MAX	
T_{Delay}	188ms	200ms	212ms	The delay time is from the falling edge of PS_ON# to the rising edge of PWRGD_OUT. This delay is selected via a strapping option. Default value is 200ms.
	470ms	500ms	530ms	
T_{FD}	15ηs		30ηs	



Symbol	Time			Description
	MIN	TYP	MAX	
T_D	0	1.6ms	2.0ms	Debounce Delay

FIGURE 28-2: SCH3226, SCH3224 100-BALL WFBGA PACKAGE OUTLINE; 8 X 8 MM BODY, 0.65MM PITCH