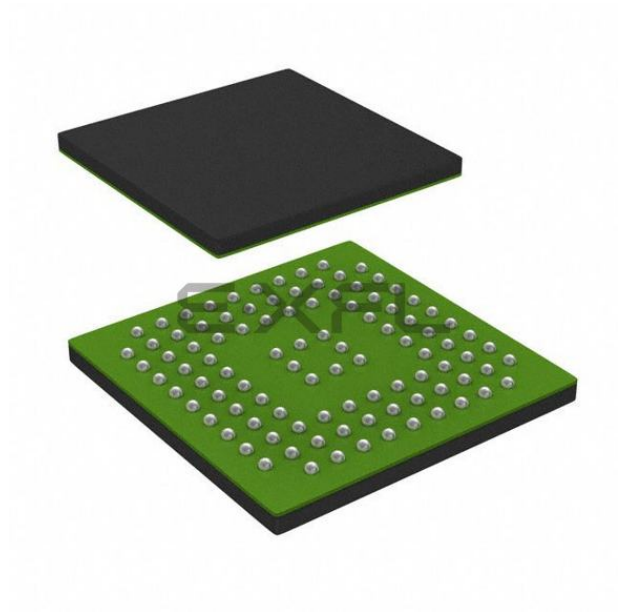

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	24
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3224i-sy

2.0 PIN LAYOUTS

2.1 SCH322x Pin Layout Summary

FIGURE 2-1: SCH3227 PIN DIAGRAM

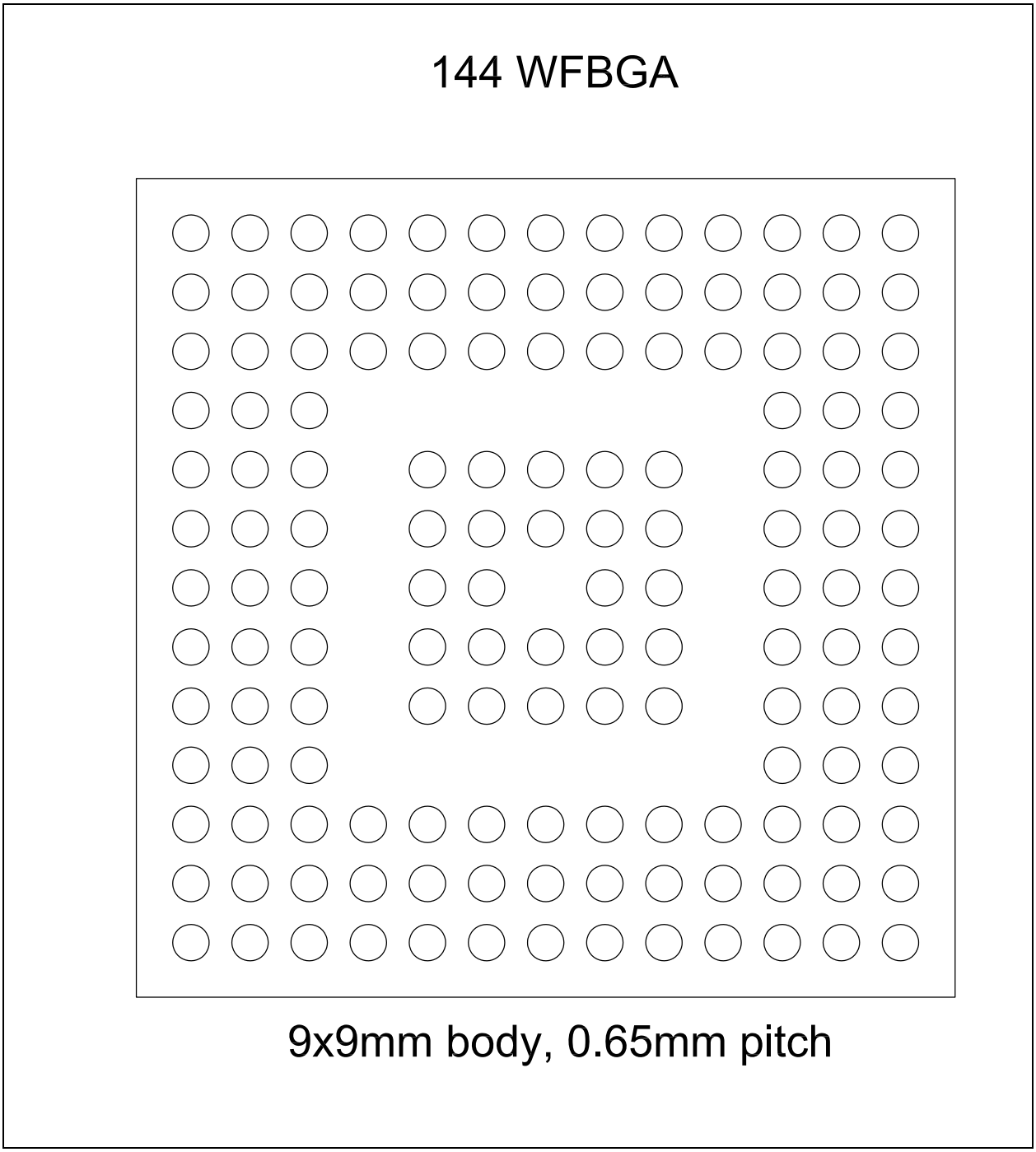


TABLE 2-3: SCH3224 SUMMARY (CONTINUED)

Ball#	Function[a]
B6	PWM2
A6	PWM1
A5	FANTACH3
B5	FANTACH2
C5	FANTACH1
B4	HVSS
C4	HVTR
A4	REMOTE2-
A3	REMOTE2+
A2	REMOTE1-
B1	REMOTE1+
B3	VCCP_IN
B2	+2.5V_IN

a. Device ID register at Plug&Play Index 0x20 holds 0x7F.

b. For correct operation, this lead must always be connected to VSS.

4.0 POWER FUNCTIONALITY

The SCH322x has five power planes: VCC, HVTR, VREF, VTR, and Vbat.

4.1 VCC Power

The SCH322x is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). VCC is the main power supply for the Super I/O Block. See Section 26.2, "DC Electrical Characteristics," on page 252.

4.2 HVTR Power

The SCH322x is family of 3.3 Volt devices. The HVTR supply is 3.3 Volts (nominal). HVTR is a dedicated power supply for the Hardware Monitoring Block. HVTR is connected to the VTR suspend well. See Section 26.2, "DC Electrical Characteristics," on page 252.

Note:	The hardware monitoring logic is powered by HVTR, but only operational when VCC is on. The hardware monitoring block is connected to the suspend well to retain the programmed configuration through a sleep cycle.

4.3 VTR Support

The SCH322x requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See Section 26.0, "Operational Description," on page 252. The maximum VTR current that is required depends on the functions that are used in the part. See Section 26.0.

If the SCH322x is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. VTR powers the IR interface, the PME configuration registers, and the PME interface. The VTR pin generates a VTR Power-on-Reset signal to initialize these components. If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 ms before Vcc begins a power-on cycle. Note that under all circumstances, the hardware monitoring HVTR must be driven as the same source as VTR.

4.3.1 TRICKLE POWER FUNCTIONALITY

When the SCH322x is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP21-GP22, GP27, GP32, GP33, GP50-GP57, GP60, GP61. These GPIOs function as follows (with the exception of GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are PME wakeup as a GPIO (or alternate function).

GP32 and GP33 revert to their non-inverting GPIO input function when VCC is removed from the part.

The other GPIOs function as follows:

GP36, GP37 and GP40:

- Buffers are powered by VCC. In the absence of VCC they are backdrive protected. These pins do not have input buffers into the wakeup logic that are powered by VTR, and are not used for wakeup.

GP42, GP60 and GP61:

- Buffers powered by VTR. GP42 are the nIO_PME pin which is active under VTR. GP60 and GP61 have LED as the alternate function and the logic is able to control the pin under VTR.

6.4 RS485 Auto Direction Control

The purpose of this function is to save the effort to deal with direction control in software. A direction control signal (usually nRTS) is used to tristate the transmitter when no other data is available, so that other nodes can use the shared lines. It is preferred to have this function on all six serial ports.

This will affect the nRTS and nDTR signals for each serial port in the device. Each serial port will have the following additional characteristics:

- An option register for the serial port in the runtime registers with following bits:
  - An enable bit to turn on/off the direction control
  - An enable bit to select which bit nRTS or nDTR, of the serial port is affected.
  - A bit to select the polarity - high or low, that the selected signal is driven to when the output buffer of the corresponding serial port is empty or full.
- When automatic direction control is enabled, the device monitors the local output buffer for not empty and empty conditions. If enabled, the direction control will force the nRTS or nDTR signal (selected via programming) to the desired polarity under the empty or not empty condition. Table 6-9 summarizes the possible programming states.
- Automatic Direction Control of the serial ports is only valid when the FIFO is enabled.
- The multi-function GPIO pins do not automatically set the direction when selected as serial port pins.
- The high speed baud rates will only work if the MSB of the MS divisor is set.

TABLE 6-9: NRTS/NDTR AUTOMATIC DIRECTION CONTROL OPTIONS

Local TX Buffer State	Flow Count EN Bit	NRTS/NDTR SEL Bit	Polarity SEL Bit	NRTS	NDTR
X	0	X	X	N/A	N/A
empty	1	1	0	0	N/A
empty	1	1	1	1	N/A
not empty	1	1	0	1	N/A
not empty	1	1	1	0	N/A
empty	1	0	0	N/A	0
empty	1	0	1	N/A	1
not empty	1	0	0	N/A	1
not empty	1	0	1	N/A	0

Note: Note that N/A indicates the signal is not affected under these conditions and maintains normal operation.

A typical application using HW automatic direction control is shown in the following FIGURE 6-4: on page 54. In this figure the nRTS signal is used to control direction.

TABLE 11-4: GPIO READ/WRITE BEHAVIOR

Host Operation	GPIO Input Port	GPIO Output Port
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

11.5 GPIO PME and SMI Functionality

The SCH3227/SCH3226/SCH3224/SCH3222 provides GPIOs that can directly generate a PME. The polarity bit in the GPIO control registers select the edge on these GPIO pins that will set the associated status bit in a PME Status. For additional description of PME behavior see Section 13.0, "PME Support," on page 94. The default is the low-to-high transition. In addition, the SCH3227/SCH3226/SCH3224/SCH3222 provides GPIOs that can directly generate an SMI.

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP21-GP22,GP27, GP32-GP33 are controlled by PME_STS1, PME_STS3, PME_EN1, PME_EN3 registers.

GP50-GP57 are controlled by PME_STS5, PME_EN5 registers.

GP60, GP61 are controlled by PME_STS6, and PME_EN6 registers.

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP21, GP22, GP54, GP55, GP56, GP57, GP60 are controlled by SMI_STS3, and SMI_EN3 registers.

GP32, GP33, GP42, GP61 are controlled by SMI_STS4, and SMI_EN4 registers.

The following GPIOs have "either edge triggered interrupt" (EETI) input capability: GP21, GP22, GP60, GP61. These GPIOs can generate a PME and an SMI on both a high-to-low and a low-to-high edge on the GPIO pin. These GPIOs have a status bit in the PME_STS6 status register that is set on both edges. The corresponding bits in the PME and SMI status registers are also set on both edges.

11.6 Either Edge Triggered Interrupts

Three GPIO pins are implemented such that they allow an interrupt (PME or SMI) to be generated on both a high-to-low and a low-to-high edge transition, instead of one or the other as selected by the polarity bit.

The either edge triggered interrupts (EETI) function as follows: If the EETI function is selected for the GPIO pin, then the bits that control input/output, polarity and open drain/push-pull have no effect on the function of the pin. However, the polarity bit does affect the value of the GP bit.

A PME or SMI interrupt occurs if the PME or SMI enable bit is set for the corresponding GPIO and the EETI function is selected on the GPIO. The PME or SMI status bits are set when the EETI pin transitions (on either edge) and are cleared on a write of '1'. There are also status bits for the EETIs located in the PME_STSX register, which are also cleared on a write of '1'. The MSC_STS register provides the status of all of the EETI interrupts within one register. The PME, SMI or MSC status is valid whether or not the interrupt is enabled and whether or not the EETI function is selected for the pin.

Miscellaneous Status Register (MSC_STS) is for the either edge triggered interrupt status bits. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding MSC status bits. Status bits are cleared on a write of '1'. See Section 24.0, "Runtime Register," on page 213 for more information.

The configuration register for the either edge triggered interrupt status bits is defined in Section 24.0.

11.7 LED Functionality

The SCH3227/SCH3226/SCH3224/SCH3222 provides LED functionality on two GPIOs, GP60 and GP61. These pins can be configured to turn the LED on and off and blink independent of each other through the LED1 and LED2 runtime registers at offset 0x5D and 0x5E from the base address located in the primary base I/O address in Logical Device A.

The LED pins (GP60 and GP61) are able to control the LED while the part is under VTR power with VCC removed. In order to control a LED while the part is under VTR power, the GPIO pin must be configured for the LED function and either open drain or push-pull buffer type. In the case of open-drain buffer type, the pin is capable of sinking current to control the LED. In the case of push-pull buffer type, the part will source current. The part is also able to blink the LED under VTR power. The LED will not blink under VTR power (VCC removed) if the external 32KHz clock is not connected.

TABLE 16-3: WDT OPERATION FOLLOWING VCC_POR OR WDT2_CTL WRITING

WDT2_CTL	VCC_PORB	RST_WDT2B	Counter Reset	Condition
x	0	x	Yes	Power On
0	1	1	No	State after VCC_PORB. Counter starts Counting
0->1	1	1	Yes	Write 1 to WDT2_CTL. Counter reset and starts counting.
1->0	1	1	No	Write 0 to WDT2_CTL. No affect - counter running.
x	1	0	Yes	Counter timeout under normal conditions.

16.2 Voltage Scaling and Reset Generator Tolerances

The 5V supply is scaled internally. The input resistance is 20kohms (min). The voltage trip point is 4.45V (nominal) with a tolerance of ±0.15V (range: 4.3V-4.6V).

For the 3.3V VTR and 3.3V supplies, the voltage trip point is 2.8V (nominal) with a tolerance of ±0.1V (range: 2.7V-2.9V).

Refer to FIGURE 16-1: on page 102.

19.0 LOW BATTERY DETECTION LOGIC

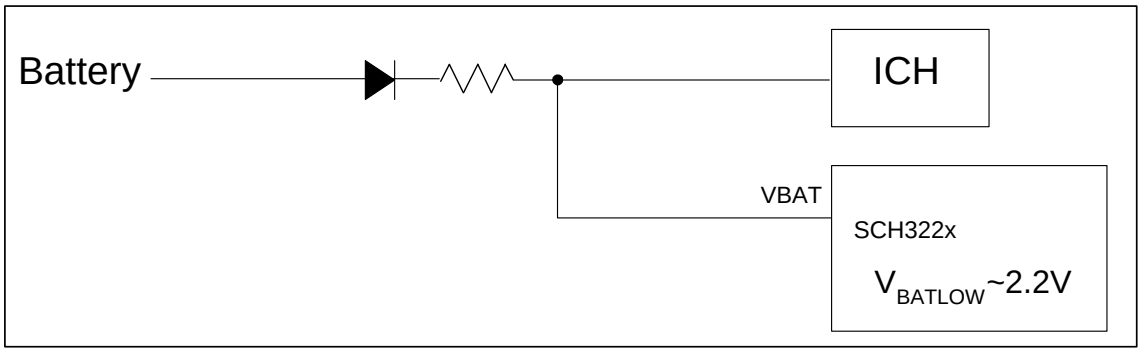
The low battery detection logic monitors the battery voltage to detect if this voltage drops below 2.2V and/or 1.2V. If the device is powered by Vbat only and the battery voltage is below approximately 1.2V, a VBAT POR will occur upon a VTR POR. If the device detects the battery voltage is below approximately 2.2V while it is powered by Vbat only or VTR (VCC=0V) the LOW_BAT PME and SMI Status bits will be set upon a VCC POR. When the external diode voltage drop is taken into account, these numbers become 1.5V and 2.5V, respectively.

The LOW_BAT PME event is indicated and enabled via the appropriate PME registers.

The LOW_BAT SMI event is indicated and enabled via the SMI_STS1 and SMI_EN1 registers. See the Section 24.0, "Runtime Register," on page 213 section for a description of these registers.

The following figure illustrates external battery circuit.

FIGURE 19-1: EXTERNAL BATTERY CIRCUIT



Note that the battery voltage of 2.2V nominal is at the VBAT pin of the device, not at the source.

19.1 VBAT POR

When VBAT drops below approximately 1.2V while both VTR and VCC are off, a VBAT POR will occur upon a VTR POR.

The LOW_BAT PME and SMI Status bits is set to ‘1’ upon a VBAT POR. Since the PME enable bit is not battery backed up and is cleared on VTR POR, the VBAT POR event is not a wakeup event. When VCC returns, if the PME or SMI enable bit (and other associated enable bits) are set, then the corresponding event will be generated.

19.2 Low Battery

19.2.1 UNDER BATTERY POWER

If the battery voltage drops below approximately 2.2V under battery power (VTR and VCC off) then the LOW_BAT PME and SMI Status bits will be set upon a VCC POR. This is due to the fact that the LOW_BAT event signal is only active upon a VCC POR, and therefore the low battery event is not a wakeup event. When VCC returns, if the PME or SMI enable bit (and other associated enable bits) are set, then a corresponding event will be generated.

19.2.2 UNDER VTR POWER

If the battery voltage drops below approximately 2.2V under VTR power (VCC off) then the LOW_BAT PME and SMI Status bits will be set upon a VCC POR. The corresponding enable bit (and other associated enable bits) must be set to generate a PME or an SMI.

If the PME enable bit (and other associated enable bits) were set prior to VCC going away, then the low battery event will generate a PME when VCC becomes active again. It will not generate a PME under VTR power and will not cause a wakeup event.

20.0 BATTERY BACKED SECURITY KEY REGISTER

Located at the Secondary Base I/O Address of Logical Device A is a 32 byte CMOS memory register dedicated to security key storage. This security key register is battery powered and has the option to be read protected, write protected, and lockable. The Secondary Base I/O Address is programmable at offsets 0x62 and 0x63. See Table 20-1, "Security Key Register Summary" is a complete list of the Security Key registers.

TABLE 20-1: SECURITY KEY REGISTER SUMMARY

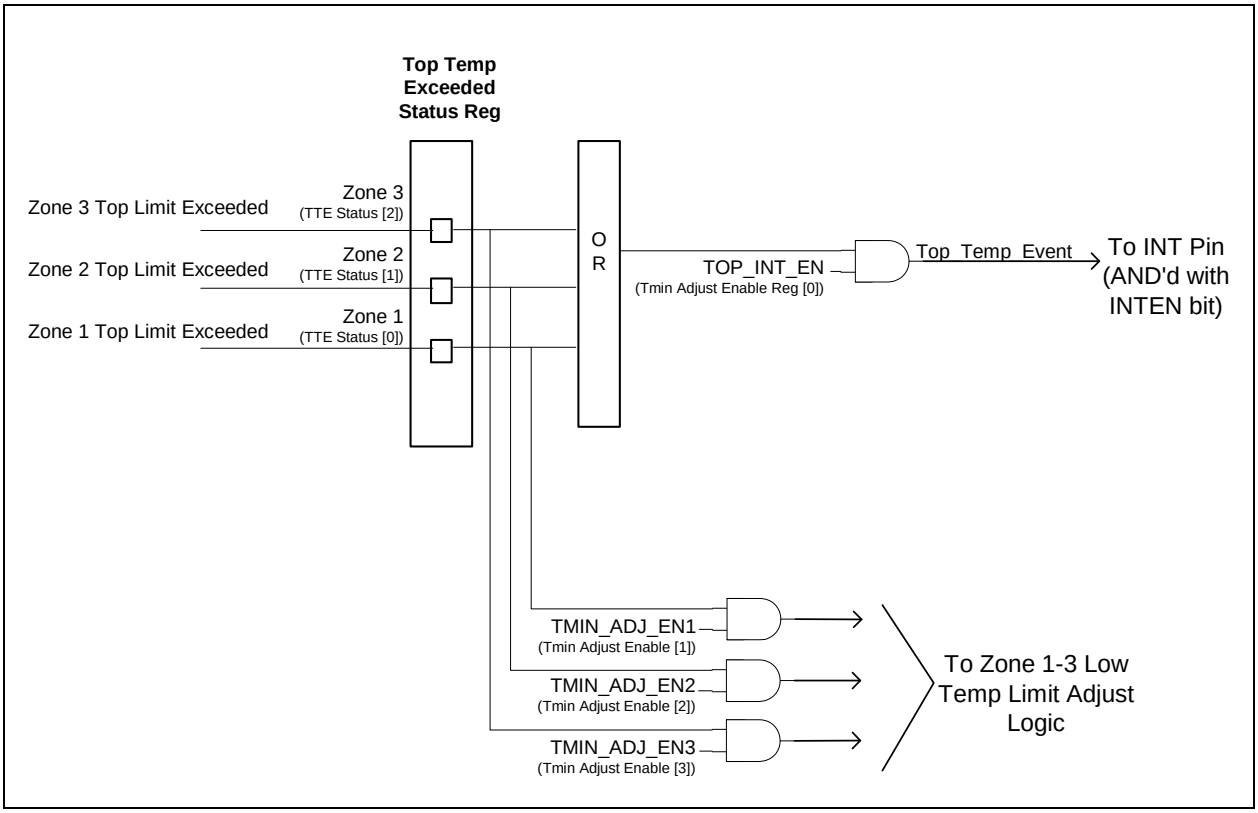
Register Offset (HEX)	VBAT POR	Register
00	0x00	Security Key Byte 0
01	0x00	Security Key Byte 1
02	0x00	Security Key Byte 2
03	0x00	Security Key Byte 3
04	0x00	Security Key Byte 4
05	0x00	Security Key Byte 5
06	0x00	Security Key Byte 6
07	0x00	Security Key Byte 7
08	0x00	Security Key Byte 8
09	0x00	Security Key Byte 9
0A	0x00	Security Key Byte 10
0B	0x00	Security Key Byte 11
0C	0x00	Security Key Byte 12
0D	0x00	Security Key Byte 13
0E	0x00	Security Key Byte 14
0F	0x00	Security Key Byte 15
10	0x00	Security Key Byte 16
11	0x00	Security Key Byte 17
12	0x00	Security Key Byte 18
13	0x00	Security Key Byte 19
14	0x00	Security Key Byte 20
15	0x00	Security Key Byte 21
16	0x00	Security Key Byte 22
17	0x00	Security Key Byte 23
18	0x00	Security Key Byte 24
19	0x00	Security Key Byte 25
1A	0x00	Security Key Byte 26
1B	0x00	Security Key Byte 27
1C	0x00	Security Key Byte 28
1D	0x00	Security Key Byte 29
1E	0x00	Security Key Byte 30
1F	0x00	Security Key Byte 31

Access to the Security Key register block is controlled by bits [2:1] of the Security Key Control (SKC) Register located in the Configuration Register block, Logical Device A, at offset 0xF2. The following table summarizes the function of these bits.

21.13.5.1.1 Interrupt Generation

The following figure illustrates the operation of the interrupt mapping for the AMTA feature in relation to the status bits and enable bits.

FIGURE 21-14: AMTA INTERRUPT MAPPING



21.14 nTHERMTRIP

The nTHERMTRIP output pin can be configured to assert when any of the temperature sensors (remote diodes 1-2, internal) is above its associated temperature limit.

The Thermtrip Enable register at offset CEh selects which reading(s) will cause the nTHERMTRIP signal to be active, when the selected temperature(s) exceed in the associated limit registers (C4h for Remote Diode 1, C5h for Remote diode 2, and C9h for Ambient temp) their pre-programmed limit.

An internal version of this output will also be used by the RESGEN block to generate a system reset pulse. More details can be found in Section 16.0, "Reset Generation," on page 101.

21.14.1 NTHERMTRIP OPERATION

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated nTHERMTRIP temperature limit (THERMTRIP Temp Limit Zone[3:1]). The Thermtrip temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Limit Zone[3:1] registers represent the upper temperature limit for asserting nTHERMTRIP for each zone. These registers are defined as follows: If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit Zone[3:1], the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERM Output Enable register).

Each zone may be individually enabled to assert the nTHERMTRIP pin (as an output).

The zone must exceed the limits set in the associated THERMTRIP Temp Limit Zone [3:1] register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

TABLE 22-1: REGISTER SUMMARY (CONTINUED)

Reg Addr	Read/ Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	
40h	R/W Note 2 2-2	Ready/Lock/Start		RES	RES	RES	Vbat Mon	OVRID	READY	LOCK Note 2 2-9	START	04h	Yes Note 2 2-2	
41h	R/WC Note 2 2-3	Interrupt Status Register 1		INT23	D2	AMB	D1	5V	VCC	Vccp	2.5V	00h Note 22-8	No	
42h	R/WC Note 2 2-3	Interrupt Status Register 2		ERR2	ERR1	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	RES	12V	00h	No	
43h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
44h	R	2.5V Low limit		7	6	5	4	3	2	1	0	00h	N/A	
45h	R	2.5V High limit		7	6	5	4	3	2	1	0	FFh	N/A	
46h	R	Vccp Low limit		7	6	5	4	3	2	1	0	00h	N/A	
47h	R	Vccp High limit		7	6	5	4	3	2	1	0	FFh	N/A	
48h	R	VCC Low limit		7	6	5	4	3	2	1	0	00h	N/A	
49h	R	VCC High limit		7	6	5	4	3	2	1	0	FFh	N/A	
4Ah	R	5V Low limit		7	6	5	4	3	2	1	0	00h	N/A	
4Bh	R	5V High limit		7	6	5	4	3	2	1	0	FFh	N/A	
4Ch	R	12V Low limit		7	6	5	4	3	2	1	0	00h	N/A	
4Dh	R	12V High limit		7	6	5	4	3	2	1	0	FFh	N/A	
4Eh	R/W	Remote Diode 1 Low Temp		7	6	5	4	3	2	1	0	81h	No	
4Fh	R/W	Remote Diode 1 High Temp		7	6	5	4	3	2	1	0	7Fh	No	
50h	R/W	Internal Diode Low Temp		7	6	5	4	3	2	1	0	81h	No	
51h	R/W	Internal Diode High Temp		7	6	5	4	3	2	1	0	7Fh	No	
52h	R/W	Remote Diode 2 Low Temp		7	6	5	4	3	2	1	0	81h	No	
53h	R/W	Remote Diode 2 High Temp		7	6	5	4	3	2	1	0	7Fh	No	
54h	R/W	FANTACH1 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	
55h	R/W	FANTACH1 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	
56h	R/W	FANTACH2 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	
57h	R/W	FANTACH2 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	
58h	R/W	FANTACH3 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No	
59h	R/W	FANTACH3 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No	
5Ah	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
5Bh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
5Ch	R/W	PWM 1 Configuration		ZON2	ZON1	ZON0	INV	SUEN1	SPIN2	SPIN1	SPIN0	62h	Yes	
5Dh	R/W	PWM 2 Configuration		ZON2	ZON1	ZON0	INV	SUEN2	SPIN2	SPIN1	SPIN0	62h	Yes	
5Eh	R/W	PWM 3 Configuration		ZON2	ZON1	ZON0	INV	SUEN3	SPIN2	SPIN1	SPIN0	62h	Yes	
5Fh	R/W	Zone 1 Range/PWM 1 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh	Yes	
60h	R/W	Zone 2 Range/PWM 2 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh	Yes	
61h	R/W	Zone 3 Range/PWM 3 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh	Yes	
62h	R/W	PWM1 Ramp Rate Control		RES1 Note 2 2-7	RES1 Note 2 2-7	RES1 Note 2 2-7	RES	RR1E	RR1-2	RR1-1	RR1-0	00h	Yes	
63h	R/W	PWM 2, PWM3 Ramp Rate Control		RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h	Yes	
64h	R/W	PWM 1 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes	
65h	R/W	PWM 2 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes	
66h	R/W	PWM 3 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes	
67h	R/W	Zone 1 (Remote Diode 1) Low Temp Limit		7	6	5	4	3	2	1	0	80h Note 22-8	Yes	
68h	R/W	Zone 2 (Ambient) Low Temp Limit		7	6	5	4	3	2	1	0	80h Note 22-8	Yes	
69h	R/W	Zone 3 (Remote Diode 2) Low Temp Limit		7	6	5	4	3	2	1	0	80h Note 22-8	Yes	
6Ah	R/W	Zone 1 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes	
6Bh	R/W	Zone 2 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes	
6Ch	R/W	Zone 3 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes	
6Dh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
6Eh	R	MCHP Test Register		7	6	5	4	3	2	1	0	44h	No	
6Fh	R	MCHP Test Register		7	6	5	4	RES	RES	RES	RES	40h	No	

Bit[4] VTR Error Enable

Bit[5] 5V Error Enable

Bit[6] 12V Error Enable

Bit[7] VCC Error Enable

The individual voltage error event bits are defined as follows:

0= disable

1= enable.

See FIGURE 21-3: Interrupt Control on page 128.

22.2.27 REGISTER 7FH: CONFIGURATION REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Fh	R/W	Configuration	INIT	MCHP	MCHP	SUREN	TRDY Note 22 -19	MON_ DN	RES	RES	10h

Note 22-19 TRDY is cleared when the PWRGD_PS signal is asserted.

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register contains the following bits:

Bit[0] Reserved

Bit[1] Reserved

Bit[2] MON_DN: This bit is used to detect when the monitoring cycle is completed following the START bit being set to 0. When the START bit is cleared, the hardware monitoring block always completes the monitoring cycle. 0= monitoring cycle active, 1= monitoring cycle complete.

APPLICATION NOTE: When the START bit is 1, and the device is monitoring, this bit will toggle each time it completes the monitoring cycle. It is intended that the user only read this bit when the START bit is 0.

Bit[3] TRDY: Temperature Reading Ready. This bit indicates that the temperature reading registers have valid values. This bit is used after writing the start bit to ‘1’. 0= not valid, 1=valid.

Bit[4] SUREN: Spin-up reduction enable. This bit enables the reduction of the spin-up time based on feedback from all fan tachometers associated with each PWM. 0=disable, 1=enable (default)

Bit[5] MCHP Reserved

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[5] MCHP Reserved

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[6] MCHP Reserved

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[7] Initialization

Setting the INIT bit to ‘1’ performs a soft reset. This bit is self-clearing. Soft Reset sets all the registers except the Reading Registers to their default values.

22.2.64 REGISTERS C4-C5, C9H: THERMTRIP TEMPERATURE LIMIT ZONE REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C4h	R/W	THERMTRIP Temp Limit ZONE 1 (Remote Diode 1)	7	6	5	4	3	2	1	0	7Fh
C9h	R/W	THERMTRIP Temp Limit ZONE 2 (Ambient)	7	6	5	4	3	2	1	0	7Fh
C5h	R/W	THERMTRIP Temp Limit ZONE 3 (Remote Diode 2)	7	6	5	4	3	2	1	0	7Fh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated THERMTRIP temperature limit (THERMTRIP Temp Limit ZONES 1-3). The THERMTRIP temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Temp Limit ZONE 1-3 registers represent the upper temperature limit for asserting nTHERMTRIP pin for each zone. These registers are defined as follows:

If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit ZONE 1-3 registers, the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERMTRIP Output Enable register).

Note: The zone must exceed the limits set in the associated THERMTRIP Temp Limit ZONE 1-3 register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

22.2.65 REGISTER CAH: THERMTRIP STATUS REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CAh	R/WC	THERMTRIP Status	RES	RES	RES	RES	RES	RD 2	RD 1	AMB	00h
Note:	Each bit in this register is cleared on a write of 1 if the event is not active.										

Note: This register is reset to its default value when the PWRGD_PS signal transitions high.

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to ‘1’ if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

22.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default).

23.0 CONFIGURATION REGISTERS

The Configuration of the SCH322x is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The SCH322x is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the SCH322x allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder

After a PCI Reset or Vcc Power On Reset the SCH322x is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the SCH322x into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the SCH322x Is in Configuration Mode.

Strap options must be added to allow four Configuration Register Base Address options: 0x002E, 0x004E, 0x162E, or 0x164E. At the deasserting edge of PCIRST# or VCC POR the nRTS1/SYSOPT0 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[7:0]= 0x2E
- 1 = Index Base I/O Address bits A[7:0]= 0x4E

At the deasserting edge of PCIRST# or VCC POR the nDTR1/SYSOPT1 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[15:8]= 0x16;
- 1 = Index Base I/O Address bits A[15:8]= 0x00

bit The above strap options will allow the Configuration Access Ports (CONFIG PORT, the INDEX PORT, and DATA PORT) to be controlled by the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins and by the Configuration Port Base Address registers at offset 0x26 and 0x27. The configuration base address at power-up is determined by the SYSOPT strap option. The SYSOPT strap option is latched state of the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins at the deasserting edge of PCIRST#. The nRTS1/SYSOPT0 pin determines the lower byte of the Base Address and the nDTR1/SYSOPT1 pin determines the upper byte of the Base Address. The following table summarizes the Base Configuration address selected by the SYSOPT strap option.

TABLE 23-1: SYSOPT STRAP OPTION CONFIGURATION ADDRESS SELECT

SYSOPT1	SYSOPT0	Default CONFIG PORT/ Index Port Address	Data Port
1	0	0x002E	INDEX PORT + 1
1	1	0x004E	
0	0	0x162E	
0	1	0x164E	

APPLICATION NOTE: The nRTS1/SYSOPT0 and the nDTR1/SYSOPT1 pins requires external pullup/pulldown resistors to set the default base I/O address for configuration to 0x002E, 0x004E, 0x162E, or 0x164E.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

Note 23-1 The configuration port base address can be relocated through CR26 and CR27.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

TABLE 23-4: CHIP-LEVEL (GLOBAL) CONFIGURATION REGISTERS (CONTINUED)

Register	Address	Description
Configuration Address Byte 0 Default Sysopt0 = 0 0x2E Sysopt0 = 1 0x4E on VCC POR and PCI RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 (Note 23-3)
Configuration Address Byte 1 Default Sysopt1 = 0 0x16 Sysopt1 = 1 0x00 n VCC POR and PCI RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] Bits[15:21] = 0 (Note 23-3)
Default = 0x00 on VCC POR, SOFT RESET and PCI RESET	0x28	Bits[7:0] Reserved - Writes are ignored, reads return 0.

Note 23-3 To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a PCI Reset or Vcc POR.

Note: The default configuration address is specified in Table 23-1, “SYSOPT Strap Option Configuration Address Select,” on page 194.

23.1.2 TEST REGISTERS

The following test registers are used in the SCH322x devices.

TABLE 23-5: TEST REGISTER SUMMARY

Register	Address	Description
TEST 8 Default = 0x00, on VCC POR and VTR POR	0x19 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 9 Default = 0x00, on VCC POR and VTR POR	0x25 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST Default = 0x00 Note on VTR_POR BIT0/7 are reset BIT1-6 reset on TST_PORB from resgen block	0x29 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.

TABLE 23-6: LOGICAL DEVICE REGISTERS (CONTINUED)

Logical Device Register	Address	Description
Interrupt Select Defaults: 0x70 = 0x00 or 0x06 (Note 23-6) on VCC POR, VTR POR, PCI RESET and SOFT RESET 0x72 = 0x00, on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x70,0x72)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the keyboard controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.
DMA Channel Select Default = 0x02 or 0x04 (Note 23-6) on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x74,0x75)	Only 0x74 is implemented for Parallel port. 0x75 is not implemented and ignores writes and returns zero when read. Refer to DMA Channel Configuration.
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device Configuration	(0xE0-0xFE)	Reserved – Vendor Defined (see MCHP defined Logical Device Configuration Registers).
Reserved	0xFF	Reserved

Note 23-4 A logical device will be active and powered up according to the following equation unless otherwise specified:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).

The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.

Note 23-5 If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note 23-6 The default value of the DMA Channel Select register for logical devices 3 and 5 is 0x04.

TABLE 23-7: BASE I/O RANGE FOR LOGICAL DEVICES

Logical Device Number	Logical Device	Register Index	Base I/O Range (Note 23-7)	Fixed Base Offsets
0x00	Reserved	n/a	n/a	n/a
0x01	Reserved	n/a	n/a	n/a
0x02	Reserved	n/a	n/a	n/a
0x03	Parallel Port	0x60,0x61	[0x0100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
			(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
WDT_CTRL Default = 0x00 on VCC POR and VTR POR Default = 0000000xb on PCI Reset Note: Bit[0] is not cleared by PCI Reset	68 (R/W) Bit[2] is Write-Only	Watch-dog timer Control Bit[0] Watch-dog Status Bit, R/W =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] P20 Force Timeout Enable, R/W = 1 Allows rising edge of P20, from the Keyboard Controller, to force the WD timeout event. A WD timeout event may still be forced by setting the Force Timeout Bit, bit 2. **Note:** • If the P20 signal is high when the enable bit is set a WD timeout event will be generated. = 0 P20 activity does not generate the WD timeout event. • The P20 signal will remain high for a minimum of 1us and can remain high indefinitely. Therefore, when P20 forced timeouts are enabled, a self-clearing edge-detect circuit is used to generate a signal which is OR'ed with the signal generated by the Force Timeout Bit. Bit[7:4] Reserved. Set to 0
TEST Default=0x00 on Vbat POR	6D (R/W)	Test Register. Test Registers are reserved for MCHP. Users should not write to this register, may produce undesired results.
GP44 Default = 0x80 on VTR POR (SCH3227 or SCH3226, and STRAPOPT=0)	6Eh (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=GPIO 0=nIDE_RSTDRV (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP44 Default = 0x01 on VTR POR (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	6Eh (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=TXD6 0=GPIO (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP45 Default = 0x00 on VTR POR (SCH3227 or SCH3226, and STRAPOPT=0)	6Fh (R/W)	General Purpose I/O bit 4.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=GPIO 0=nPCI_RST1 (Default) Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

27.4.1 ECP PARALLEL PORT TIMING

Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500KBytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK and begins the next transfer based on Busy. Refer to FIGURE 27-16: on page 268.

ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in FIGURE 27-17: on page 268.

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

Reverse Data Transfer Phase

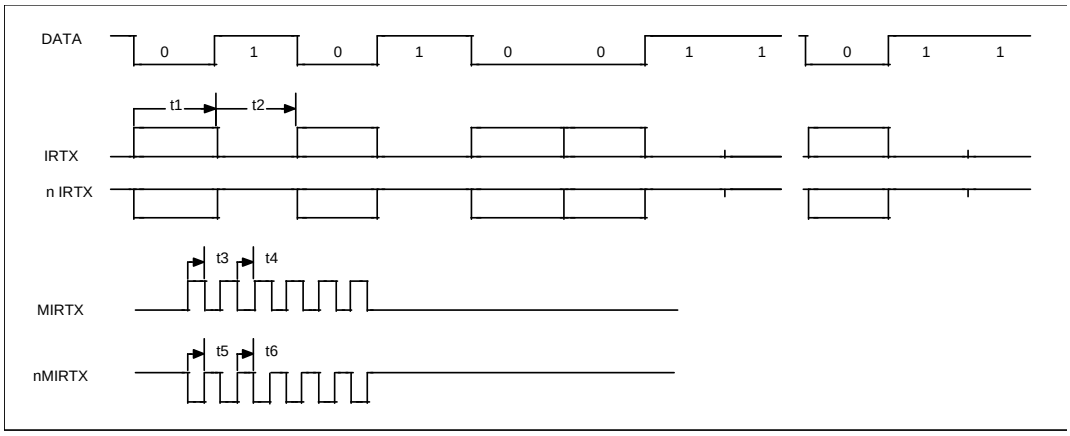
The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has been accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready to accept a byte it sets HostAck (nALF) high to acknowledge the handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data, it sets HostAck (nALF) low, completing the transfer. This sequence is shown in FIGURE 27-18: on page 269.

Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used in ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-drain), the drivers are dynamically changed from open-drain to push-pull. The timing for the dynamic driver change is specified in the *IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14*, July 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

FIGURE 27-22: AMPLITUDE SHIFT-KEYED IR TRANSMIT TIMING



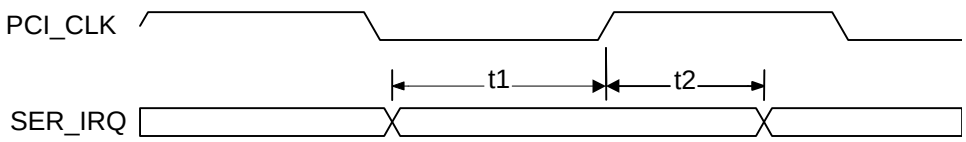
	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µ s
t2	Off Bit Time				µ s
t3	Modulated Output "On"	0.8	1	1.2	µ s
t4	Modulated Output "Off"	0.8	1	1.2	µ s
t5	Modulated Output "On"	0.8	1	1.2	µ s
t6	Modulated Output "Off"	0.8	1	1.2	µ s

Notes:

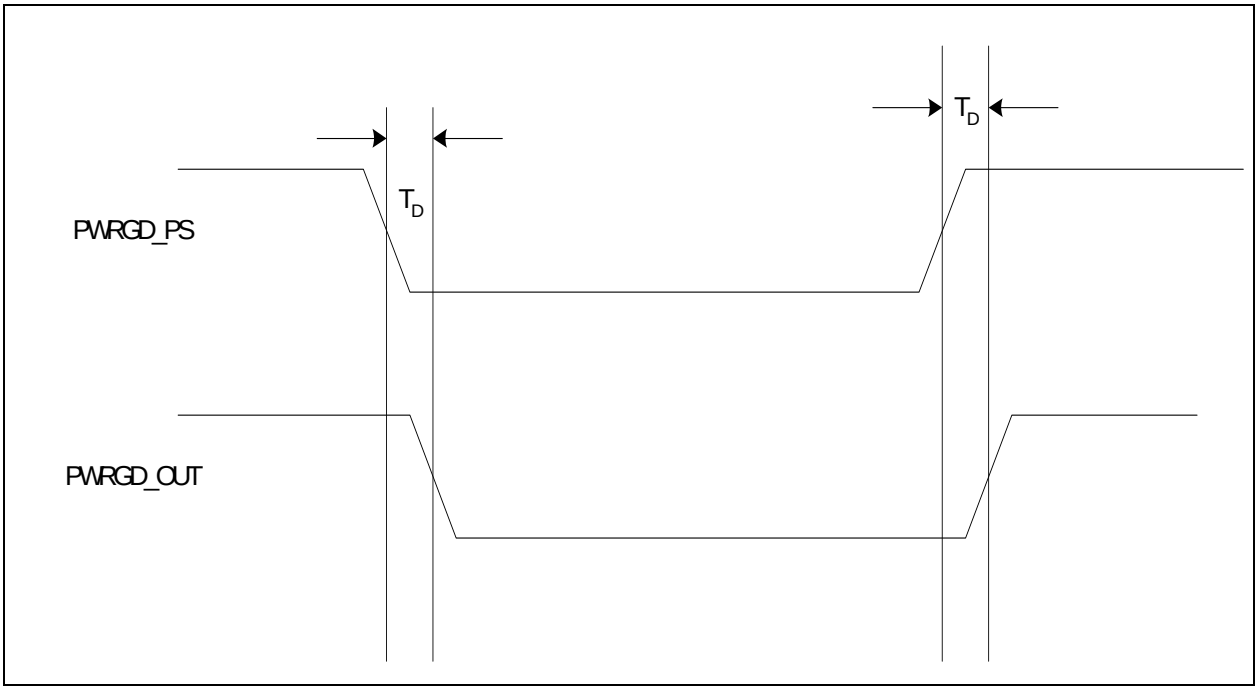
1. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0
   MIRTX, nMIRTX are the modulated outputs

27.6 Serial IRQ Timing

FIGURE 27-23: SETUP AND HOLD TIME



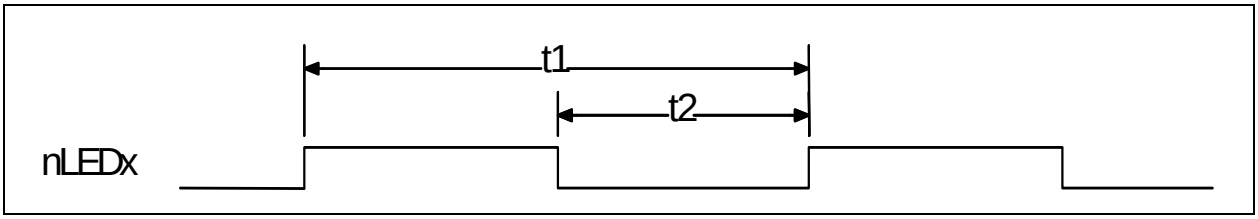
Name	Description	MIN	TYP	MAX	Units
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec



Symbol	Time			Description
	MIN	TYP	MAX	
T_D	1ηs	10ηs	20ηs	Gate Delay

27.11 nLEDx Timing

FIGURE 27-29: NLEDX TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Period		1 or 2[2]	5.88[1]	sec
t2	Blink ON Time	0	0.5[2]	1.52[1]	sec

1. These Max values are due to internal Ring Oscillator. If 1Hz blink rate is selected for LED1 pin, the range will vary from 0.33Hz to 1.0Hz. If 0.5Hz blink rate is selected for LED1 pin, the range will vary from 0.17Hz to 0.5Hz.

2. The blink rate is programmed through Bits[1:0] in LEDx register. When Bits[1:0]=00, LED is OFF. Bits[1:0]=01 indicates LED blink at 1Hz rate with a 50% duty cycle (0.5 sec ON, 0.5 sec OFF). Bits[1:0]=10 indicates LED blink at ½ Hz rate with a 25% duty cycle (0.5 sec ON, 1.5 sec OFF). When Bits[1:0]=11, LED is ON.

APPENDIX C: TEST MODE

The SCH322x provides board test capability through the implementation of one XNOR chain and one XOR chain. The XNOR chain is dedicated to the Super I/O portion and the Hardware Monitoring Block of the device.

Note:	Pins that are not brought out of the package are tied to a determinate voltage internal to the package, and so will not affect the XNOR output, except that its initial state may differ among family members.

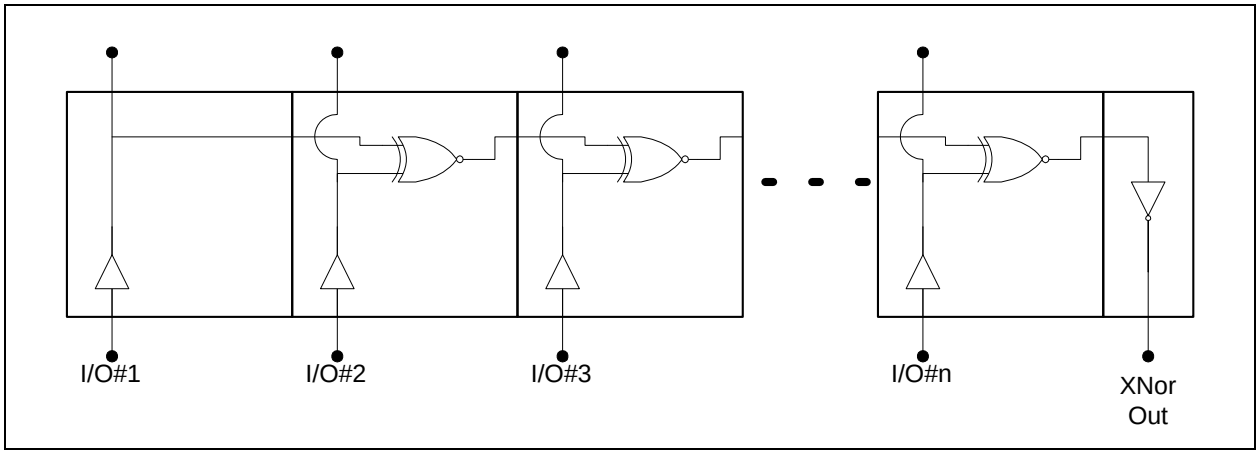
C.1 XNOR-Chain Test Mode Overview

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure C-1. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SCH322x pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

FIGURE C-1: XNOR-CHAIN TEST STRUCTURE



C.1.1 Board Test Mode

Board test mode can be entered as follows:

On the rising (deasserting) edge of PCI_RESET#, drive LFRAME# low and drive LAD[0] low.

Exit board test mode as follows:

On the rising (deasserting) edge of PCI_RESET#, drive either LFRAME# or LAD[0] high.

The PCI_RESET# pin is not included in the XNOR-Chain. The XNOR-Chain output pin# is TXD1. See the following sub-sections for more details.

Pin List of XNOR Chain

All pins on the chip are inputs to the first XNOR chain, with the exception of the following:

- All power supply pins - HVTR, HVSS, VCC, VTR, and Vbat
- VSS and AVSS
- All analog inputs: Remote2-, Remote2+, Remote1-, Remote1+, VCCP_IN, +12V_IN, +5V_IN, +2.5V_IN
- TXD1 This is the chain output.
- PCI_RESET#.