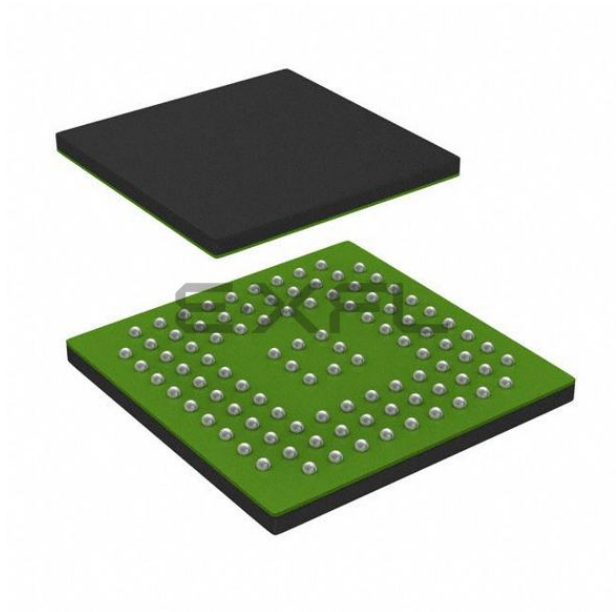

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3226-sy-tr

TABLE 2-4: SCH3222 SUMMARY

BALL#	FUNCTION[a]
B1	+5V_IN
A1	GP40
C1	VTR
A2	TEST=VSS[b]
D1	VSS
E1	CLOCKI
B2	LAD0
C2	LAD1
B3	LAD2
D2	LAD3
F1	LFRAME#
F2	PCI_RESET#
F3	PCI_CLK
E3	SER_IRQ
G2	VSS
G1	VCC
H1	GP44 / TXD6
J1	GP45 / RXD6
J2	GP46 / nSCIN6
K1	GP47 / nSCOUT6
K2	AVSS
H2	VBAT
K3	GP27 / nIO_SMI / P17
J3	KDAT / GP21
J4	KCLK / GP22
F4	MDAT / GP32
E4	MCLK / GP33
J5	GP36 / nKBDRST
K4	GP37 / A20M
K6	VSS
K5	VTR
K7	VSS
K8	nRI1
H5	nDCD1
K10	RXD1
J10	TXD1 / SIOXNOROUT
K9	nDSR1
J9	nRTS1 / SYSOPT0
H10	nCTS1
H9	nDTR1 / SYSOPT1
J8	GP50 / nRI2
G9	VTR
J7	VSS
G5	GP51 / nDCD2

4.0 POWER FUNCTIONALITY

The SCH322x has five power planes: VCC, HVTR, VREF, VTR, and Vbat.

4.1 VCC Power

The SCH322x is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). VCC is the main power supply for the Super I/O Block. See Section 26.2, "DC Electrical Characteristics," on page 252.

4.2 HVTR Power

The SCH322x is family of 3.3 Volt devices. The HVTR supply is 3.3 Volts (nominal). HVTR is a dedicated power supply for the Hardware Monitoring Block. HVTR is connected to the VTR suspend well. See Section 26.2, "DC Electrical Characteristics," on page 252.

Note:	The hardware monitoring logic is powered by HVTR, but only operational when VCC is on. The hardware monitoring block is connected to the suspend well to retain the programmed configuration through a sleep cycle.

4.3 VTR Support

The SCH322x requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See Section 26.0, "Operational Description," on page 252. The maximum VTR current that is required depends on the functions that are used in the part. See Section 26.0.

If the SCH322x is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. VTR powers the IR interface, the PME configuration registers, and the PME interface. The VTR pin generates a VTR Power-on-Reset signal to initialize these components. If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full minimum potential at least 10 ms before Vcc begins a power-on cycle. Note that under all circumstances, the hardware monitoring HVTR must be driven as the same source as VTR.

4.3.1 TRICKLE POWER FUNCTIONALITY

When the SCH322x is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP21-GP22, GP27, GP32, GP33, GP50-GP57, GP60, GP61. These GPIOs function as follows (with the exception of GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are PME wakeup as a GPIO (or alternate function).

GP32 and GP33 revert to their non-inverting GPIO input function when VCC is removed from the part.

The other GPIOs function as follows:

GP36, GP37 and GP40:

- Buffers are powered by VCC. In the absence of VCC they are backdrive protected. These pins do not have input buffers into the wakeup logic that are powered by VTR, and are not used for wakeup.

GP42, GP60 and GP61:

- Buffers powered by VTR. GP42 are the nIO_PME pin which is active under VTR. GP60 and GP61 have LED as the alternate function and the logic is able to control the pin under VTR.

6.1.16 NOTES ON SERIAL PORT OPERATION

FIFO Mode Operation:

General

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

6.1.16.1 TX and RX FIFO Operation

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

6.1.16.2 TXD2 Pin

The TXD2 signal is located on the GP53/TXD2(IRTX) pin. The operation of this pin following a power cycle is defined in Section 6.2.1, "IR Transmit Pin," on page 51.

6.2 Infrared Interface

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two IR implementations have been provided for the second UART in this chip (logical device 5), IrDA and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TXD2 and RXD2 pins. These can be selected through the configuration registers.

IrDA 1.0 allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows asynchronous serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

7.1.3 CONTROL PORT

ADDRESS OFFSET = 02H

The Control Port is located at an offset of ‘02H’ from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

Bit 0 STROBE - Strobe

This bit is inverted and output onto the nSTROBE output.

Bit 1 AUTOFD - Autofeed

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

Bit 2 nINIT - Initiate Output

This bit is output onto the nINIT output without inversion.

Bit 3 SLCTIN - Printer Select Input

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

Bit 4 IRQE - Interrupt Request Enable

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

Bit 5 PCD - PARALLEL CONTROL DIRECTION

Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

7.1.4 EPP ADDRESS PORT

ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of ‘03H’ from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP ADDRESS WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

7.1.5 EPP DATA PORT 0

ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of ‘04H’ from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP DATA WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

7.1.6 EPP DATA PORT 1

ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of ‘05H’ from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.2.5 DEVICE STATUS REGISTER (DSR)

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

Bit 3 nFault

The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

Bit 4 Select

The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

Bit 5 PError

The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

Bit 6 nAck

The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

Bit 7 nBusy

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

7.2.6 DEVICE CONTROL REGISTER (DCR)

ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

Bit 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

Bit 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

Bit 2 nINIT - INITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

Bit 3 SELECTIN

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

Bit 4 ackIntEn - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

Bit 5 DIRECTION

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)

7.2.11 DATA COMPRESSION

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

7.2.12 PIN DEFINITION

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-drain in mode 000 and are push-pull in all other modes.

7.2.13 LPC CONNECTIONS

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

7.2.14 INTERRUPTS

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupts generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

An interrupt is generated when:

1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC cycle is received.
2. For Programmed I/O:
   a) When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.
3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

7.2.15 FIFO OPERATION

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or DMA cycle depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO automatic direction control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a “fast” system. A high value of threshold (i.e. 12) is used with a “sluggish” system by affording a long latency period after a service request, but results in more frequent service requests.

11.2 Description

Each GPIO port has a 1-bit data register and an 8-bit configuration control register. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP6. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. All of the GPIO registers are located in the PME block see Section 24.0, "Runtime Register," on page 213. The GPIO ports with their alternate functions and configuration state register addresses are listed in Table 11-2.

TABLE 11-2: SCH322X GENERAL PURPOSE I/O PORT ASSIGNMENTS

Run-Time REG Offset (HEX)	DEF	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	GP Data REG	GP Data Bit
23	GPIO10	RXD3			GP1 OFFSET 4B	0
24	GPIO11	TXD3				1
25	GPIO12	nDCD3				2
26	GPIO13	nRI3				3
27	GPIO14	nDSR3				4
29	GPIO15	nDTR3				5
2A	GPIO16	nCTS3				6
2B	GPIO17	nRTS3				7
	Reserved				GP2 OFFSET 4C	0
2C	KDAT (See Note 11-6)	GPIO21				1
2D	KCLK (See Note 11-6)	GPIO22				2
	Reserved					4:3
	Reserved					5
	Reserved					6
32	GPIO27	SMI Output	P17 (See Note 11-6)			7
33	nFPRST	GPIO30			GP3 OFFSET 4D	0
34	GPIO31	nRI4				1
35	MDAT (See Note 11-6)	GPIO32				2
36	MCLK (See Note 11-6)	GPIO33				3
37	GPIO34	nDTR4				4
	Reserved					5
39	GPIO36	Keyboard Reset				6
3A	GPIO37	Gate A20				7
3B	GPIO40	Drive Density Select 0			GP4 OFFSET 4E	0
	Reserved					1
3D	GPIO42	nIO_PME				2
	Reserved					3
6E	GPIO44	TXD6				4
6F	GPIO45	RXD6				5
72	GPIO46	nSCIN6				6
73	GPIO47	nSCOUT6				7

14.0 WATCHDOG TIMER

The SCH322x contains a Watchdog Timer (WDT). The Watchdog Time-out status bit may be mapped to an interrupt through the WDT_CFG Runtime Register.

The SCH322x WDT has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 seconds with 1 second resolution. The units of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register. The WDT time-out value is set through the WDT_VAL Runtime register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Runtime register.

Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

Note 14-1 To set the WDT for time X minutes, the value of X+1 minutes must be programmed. To set the WDT for X seconds, the value of X+1 seconds must be programmed.

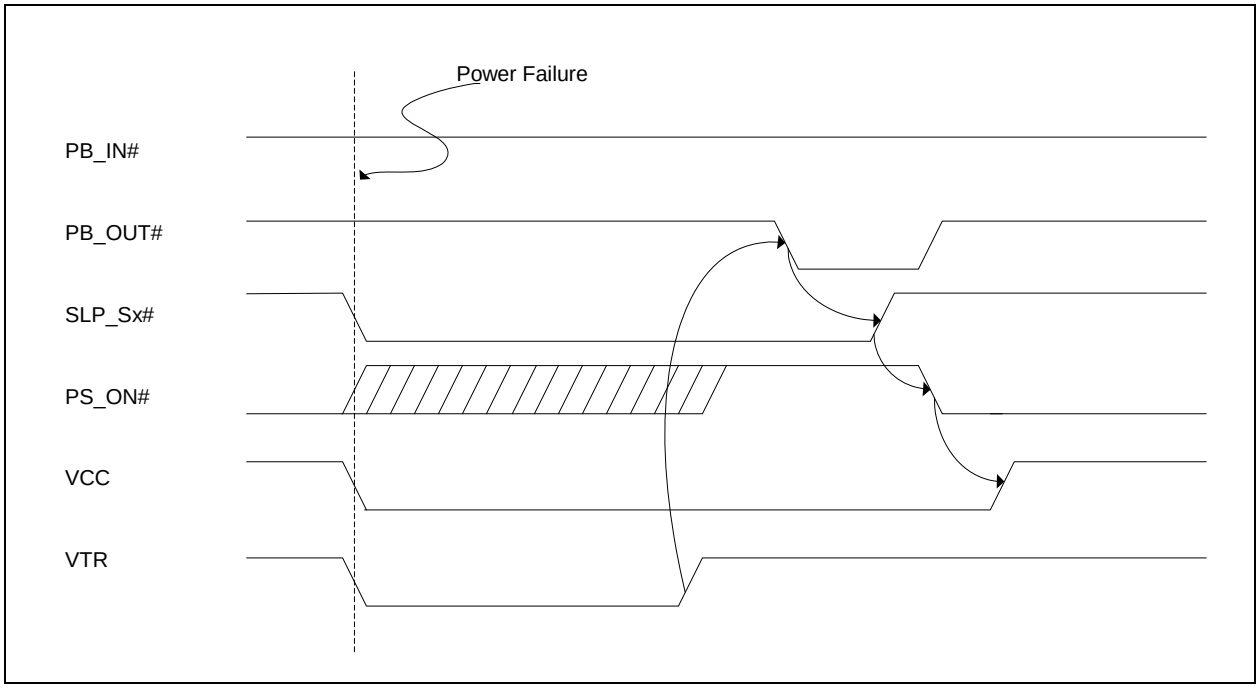
Two system events can reset the WDT: a Keyboard Interrupt or a Mouse Interrupt. The effect on the WDT for each of these system events may be individually enabled or disabled through bits in the WDT_CFG Runtime register. When a system event is enabled through the WDT_CFG register, the occurrence of that event will cause the WDT to reload the value stored in WDT_VAL and reset the WDT time-out status bit if set. If both system events are disabled, the WDT_VAL register is not re-loaded.

The Watchdog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. The WDT interrupt is mapped to an interrupt channel through the WDT_CFG Runtime register. When mapped to an interrupt the interrupt request pin reflects the value of the WDT time-out status bit.

The host may force a Watchdog time-out to occur by writing a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Runtime register. Writing a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watchdog Status). Bit 2 of the WDT_CTRL is self-clearing.

See the Section 24.0, "Runtime Register" for description of these registers.

FIGURE 18-5: POWER SUPPLY AFTER POWER FAILURE (RETURN TO ON)



18.4 Resume Reset Signal Generation

nRSMRST signal is the reset output for the ICH resume well. This signal is used as a power on reset signal for the ICH.

The SCH322x detects when VTR voltage raises above V_{TRIP} and provides a delay before generating the rising edge of nRSMRST. See Section 27.9, "Resume Reset Signal Generation," on page 275 for a detailed description of how the nRSMRST signal is generated.

18.5 Keyboard Power Button

The SCH322x has logic to detect a keyboard make/break scan codes that may be used for wakeup (PME generation). The scan codes are programmed in the Keyboard Scan Code Registers, located in the runtime register block, from offset 0x5F to 0x63 from the base address located in the primary base I/O address in Logical Device A. These registers are powered by Vbat and are reset on a Vbat POR.

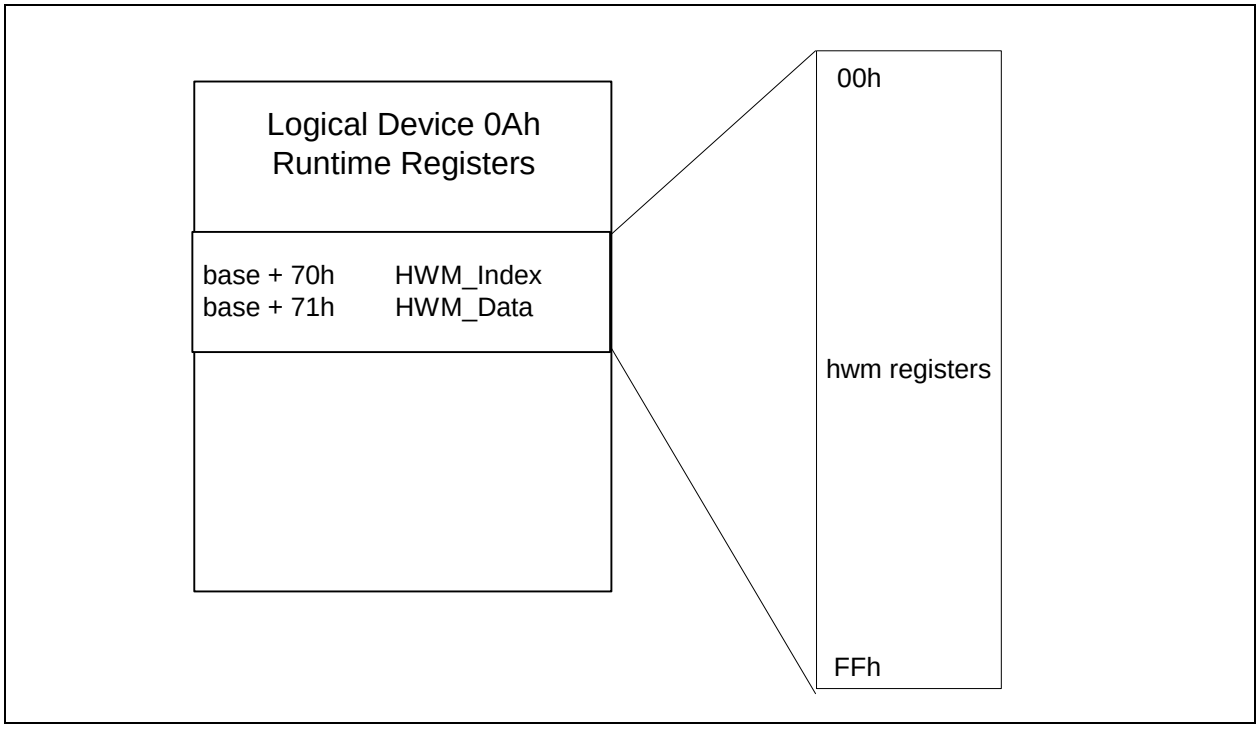
The following sections will describe the format of the keyboard data, the methods that may be used to decode the make codes, and the methods that may be used to decode the break codes.

The Wake on Specific Key Code feature is enabled for the assertion of the nIO_PME signal when in SX power state or below.

21.2 HWM Interface

The SCH322x HWM block registers are accessed through an index and data register located at offset 70h and 71h, respectively, from the address programmed in the Base I/O Address in Logical Device A (also referred to as the Runtime Register set).

FIGURE 21-2: HWM REGISTER ACCESS



21.3 Power Supply

The HWM block is powered by standby power, HVTR, to retain the register settings during a main power (sleep) cycle. The HWM block does not operate when VCC=0 and HVTR is on. In this case, the H/W Monitoring logic will be held in reset and no monitoring or fan control will be provided. Following a VCC POR, the H/W monitoring logic will begin to operate based on programmed parameters and limits.

The fan tachometer input pins are protected against floating inputs and the PWM output pins are held low when VCC=0.

Note:	The PWM pins will be forced to “spinup” (if enabled) when PWRGD_PS goes active. See “PWM Fan Speed Control” on page 134.

21.4 Resetting the SCH322x Hardware Monitor Block

21.4.1 VTR POWER-ON RESET

All the registers in the Hardware Monitor Block, except the reading registers, reset to a default value when VTR power is applied to the block. The default state of the register is shown in the Register Summary Table. The default state of Reading Registers are not shown because these registers have indeterminate power on values.

Note:	Usually the first action after power up is to write limits into the Limit Registers.

The nHWM_INT pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding diode error bit to be set. This will cause the nHWM_INT pin to become active if enabled.

The nHWM_INT pin can be enabled to indicate fan errors. Bit[0] of the Interrupt Enable 2 (Fan Tachs) register (80h) is used to enable this option. This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The nHWM_INT pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the nHWM_INT pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to '1' again.

The nHWM_INT pin may only become active while the monitor block is operational.

21.9.2 INTERRUPT AS A PME EVENT

The hardware monitoring interrupt signal is routed to the SIO PME block. For a description of these bits see the section defining PME events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

The THERM PME status bit is located in the PME_STS1 Runtime Register at offset 04h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM PME status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the PME_EN1 register at offset 0Ah.

21.9.3 INTERRUPT AS AN SMI EVENT

The hardware monitoring interrupt signal is routed to the SIO SMI block. For a description of these bits see the section defining SMI events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

The THERM SMI status bit is located in the SMI_STS5 Runtime Register at offset 14h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM SMI status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the SMI_EN5 register at offset 1Ah.

The SMI is enabled onto the SERIRQ (IRQ2) via bit 6 of the SMI_EN2 register at 17h.

21.9.4 INTERRUPT EVENT ON SERIAL IRQ

The hardware monitoring interrupt signal is routed to the Serial IRQ logic. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

This operation is configured via the Interrupt Select register (0x70) in Logical Device A. This register allows the selection of any serial IRQ frame to be used for the HWM nHWM_INT interrupt (SERIRQ9 slot will be used). See Interrupt Event on Serial IRQ on page 130.

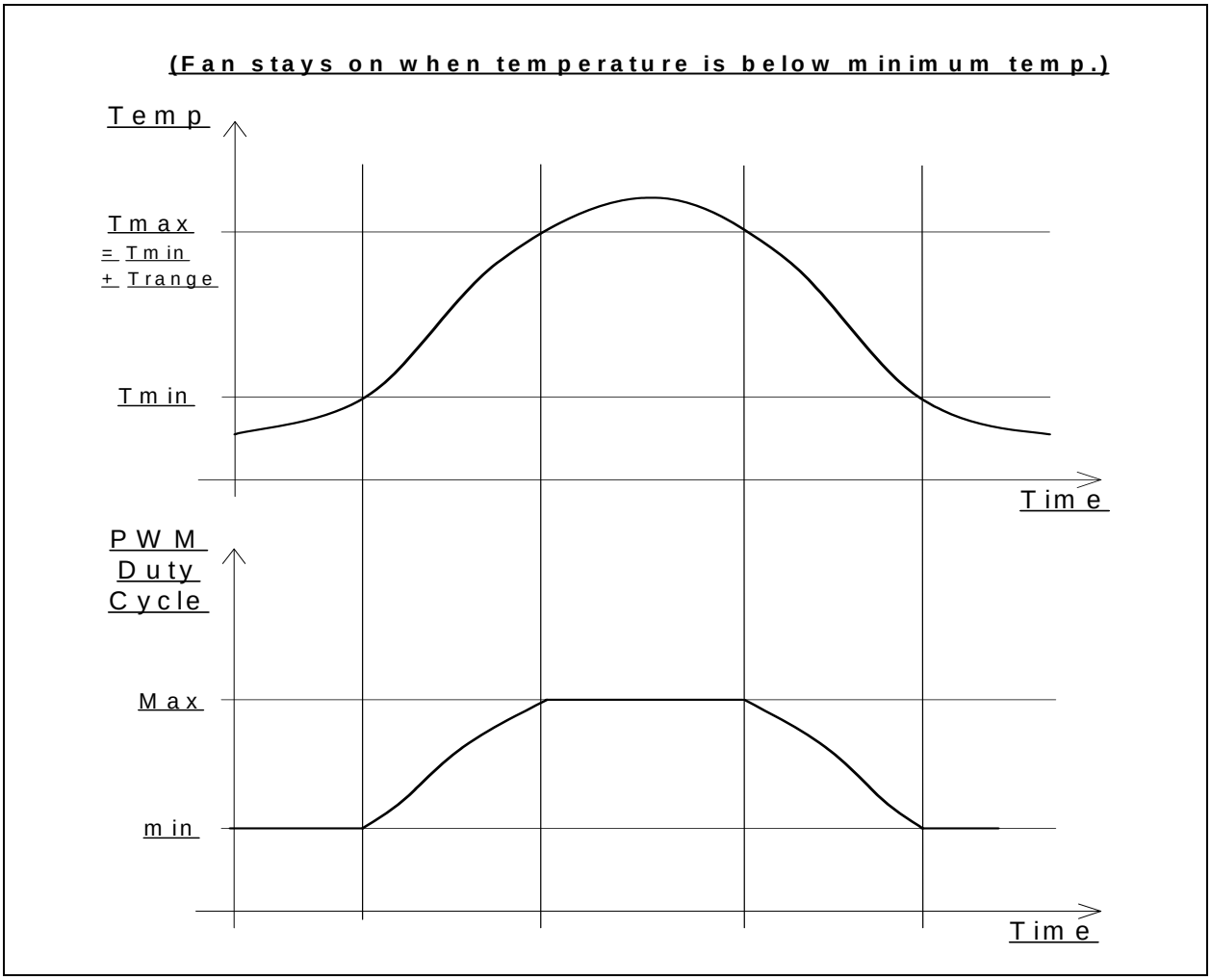
21.10 Low Power Mode

bit The hardware monitor has two modes of operation: Monitoring and Sleep. When the START bit, located in Bit[0] of the Ready/Lock/Start register (0x40), is set to zero the hardware monitor is in Sleep Mode. When this bit is set to one the hardware monitor is fully functional and monitors the analog inputs to this device.
bit Sleep mode is a low power mode in which bias currents are on and the internal oscillator is on, but the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

Note 1: In Sleep Mode the PWM Pins are held high forcing the PWM pins to 100% duty cycle (256/256).

2: The START a bit cannot be modified when the LOCK bit is set.

FIGURE 21-5: AUTOMATIC FAN CONTROL



21.13.3.3 Spin Up

When a fan is being started from a stationary state (PWM duty cycle =00h), the part will cause the fan to “spin up” by going to 100% duty cycle for a programmable amount of time to overcome the inertia of the fan (i.e., to get the fan turning). Following this spin up time, the fan will go to the duty cycle computed by the auto fan algorithm.

During spin-up, the PWM duty cycle is reported as 0%.

To limit the spin-up time and thereby reduce fan noise, the part uses feedback from the tachometers to determine when each fan has started spinning properly. The following tachometer feedback is included into the auto fan algorithm during spin-up.

Auto Fan operation during Spin Up:

The PWM goes to 100% duty cycle until the tachometer reading register is below the minimum limit (see Figure 21-6), or the spin-up time expires, whichever comes first. This causes spin-up to continue until the tachometer enters the valid count range, unless the spin up time expires. If the spin up expires before the tachometer enters the valid range, an interrupt status bit will be set once spin-up expires. Note that more than one tachometer may be associated with a PWM, in which case all tachometers associated with a PWM must be in the valid range for spin-up to end.

Following PWRGD_PS being asserted the PWM Pin will be held low until either the TRDY signal is asserted or the delay counter expires, whichever comes first. The delay counter performs two functions when set to the 2 second delay option.

1. Following a VTR POR & VCC POR, the BIOS has up to 2 seconds to program the hwm registers and enable autofan before the fans are turned on full. This is a noise reduction feature
2. Following a VCC POR only (return from sleep) the hardware requires 150.8 ms (default - see Table 21-2) to load the temperature reading registers. The TRDY signal is used to indicate when these values have been updated. TRDY is reset to zero on a VCC POR, which forces the Fans to be set to FFh. If the delay counter is enabled for up to a 2 second delay, the PWMs will be held low until the reading registers are valid. Once the registers are updated, the hardware will initiate a forced spinup (if enabled) and enter automode. See Forced Spinup on page 141.

The timing diagrams in the section titled Timing Diagrams for PWM Clamp and Forced Spinup Operation on page 142 show the effect of the 2 second PWM hold-off counter on the PWM pin.

21.13.4.2 Forced Spinup

Spinup is a feature of the auto fan control mode. Any time the PWM pin transitions from a 0% duty cycle to a non zero duty cycle the PWM pin will be forced high for the duration of spinup or until the fan are spinning within normal operating parameters as determined by the Tach Limit registers. See Spin Up on page 137 for a more detailed description of spinup. This feature can also be initiated by the PWRGD_PS signal transitioning high following a main (VCC) power cycle if the TRDY bit is set to one before the PWM Clamp is released.

Note 1: In this device, a forced spinup will be generated the first time TRDY is detected as a '1' following the PWRGD_PS signal transitioning from low to high (if enabled). To enable this feature, set bit[3] of the PWMx Configuration registers to one. These registers are located at offsets 5Ch, 5Dh, and 5Eh.

2: If the TRDY bit is '1' and cleared by software after being set to and then set again while the PWRGD_PS signal is high, the act of TRDY being asserted will not cause a forced spinup event.

- The duration of the forced spin-up time is controlled by the SPIN[2:0] bits located in the PWM x Configuration registers (5Ch - 5Eh). The forced spinup enable bit is located in Bit[3] SUENx of the PWMx Configuration registers. Forced Spinup defaults to disabled on a VTR POR.

21.13.4.2.1 Start of Spin-up on main (VCC) power cycle

The PWM spin-up supports the scenario where the part is powered by VTR and the fans are powered by a main power rail. If the start bit is not cleared on a main power cycle, then the PWM will remain at a level that may not start the fan when the main supply ramps up. This spinup will force each PWM into spin-up (if enabled) when the TRDY bit goes active.

21.13.4.2.2 Start of Spin-up on Standby (VTR) Power Cycle

The two second PWM Clamping feature may be used to delay the fans from being turned on full until the BIOS has the opportunity to program the limit and configuration registers for the auto fan control mode. (See PWM Clamp on page 140) This is a noise reduction feature. Once the TRDY bit goes high the clamp will be released and the fans will be forced into spinup.

Note:	If the two second PWM Clamping period expires before TRDY is asserted, the PWMs will be set to Full On.

22.2.28 REGISTER 80H: INTERRUPT ENABLE 2 REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
80h	R/W	Interrupt Enable 2 (Fan Tachs)	RES	RES	RES	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	FAN-TACH	1Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual fan tach error events to set the corresponding status bits in the interrupt status registers. This register also contains the group fan tach enable bit (Bit[0] TACH), which is used to enable fan tach events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] FANTACH (Group TACH Enable)

0= Out-of-limit tachometer readings do not affect the state of the nHWM_INT pin (default)

1= Enable out-of-limit tachometer readings to make the nHWM_INT pin active low

Bit[1] Fantach 1 Event Enable

Bit[2] Fantach 2 Event Enable

Bit[3] Fantach 3 Event Enable

Bit[4] Reserved

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual fan tach error event bits are defined as follows:

0= disable

1= enable.

22.2.29 REGISTER 81H: TACH_PWM ASSOCIATION REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
81h	R/W	TACH_PWM Association	RES	RES	T3H	T3L	T2H	T2L	T1H	T1L	24h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to associate a PWM with a tachometer input. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers.

The fan tachometer will not cause a bit to be set in the interrupt status register:

a) if the current value in Current PWM Duty registers is 00h or
b) if the fan is disabled via the Fan Configuration Register.

Note: A bit will never be set in the interrupt status for a fan if its tachometer minimum is set to FFFFh.

See bit definition below.

Bits[1:0] Tach1. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[3:2] Tach2. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[5:4] Tach3. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[7:6] Reserved

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PME_EN7 Default = 0x00 on Vbat POR (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	10 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_EN bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] RI3 Bit[1] RI4 Bit[2] RI5 Bit[3] RI6 Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
SP12 Option Default = 0x44 on VTR POR	0x12 (R/W)	SP Options for SP1 and SP2 Bit[0] Automatic Direction Control Select SP1 1=FC on 0=FC off Bits[1] Signal select SP1 1=nRTS control 0=nDTR control Bits[2] Polarity SP1 0= Drive low when enabled 1= Drive 1 when enabled Bits[3] RESERVED Bit[4] Automatic Direction Control Select SP2 1=FC on 0=FC off Bits[5] Signal select SP2 1=nRTS control 0=nDTR control Bits[6] Polarity SP2 0= Drive low when enabled 1= Drive 1 when enabled Bits[7] RESERVED
SP34 Option Default = 0x44 on VTR POR (SCH3224)	0x13 (R/W)	Bits[7:0] RESERVED

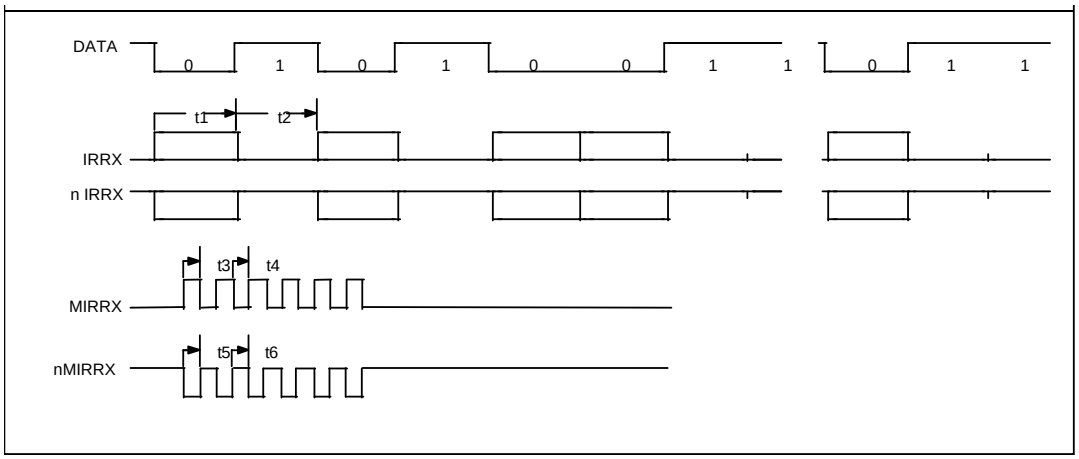
TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP42 Default =0x01 on VTR POR	3D (R/W)	General Purpose I/O bit 4.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_PME **Note:** Configuring this pin function as output with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP50 Default = 0x01 on VTR POR	3F (R/W)	General Purpose I/O bit 5.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nRI2 (Note 24-18) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP51 Default = 0x01 on VTR POR	40 (R/W)	General Purpose I/O bit 5.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDCD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP52 Default = 0x01 on VTR POR	41 (R/W)	General Purpose I/O bit 5.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=RXD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP53 Default = 0x01 on VTR POR	42 (R/W)	General Purpose I/O bit 5.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=TXD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

TABLE 26-1: BUFFER OPERATIONAL RATINGS (CONTINUED)

SUPER I/O BLOCK (T_A INDUSTRIAL = -40°C – +85°C, V_{CC} = +3.3 V ± 10%) OR (T_A COMMERCIAL = 0°C – +70°C, V_{CC} = +3.3 V ± 10%)						
Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**Units**	**Comments**
IO12 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IOP14 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
IOD16 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
High Output Level	V_{OH}			5.5	V	Open Drain;
OD_PH Type Buffer	VOL			0.3	V	RLOAD is 40ohms to 1.2V Max Output impedance is 10ohms
PCI Type Buffers (PCI_ICLK, PCI_I, PCI_O, PCI_IO)	3.3V PCI 2.1 Compatible.					
Leakage Current (ALL)						(Note 26-1)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Backdrive Protect/ChiProtect (All signal pins excluding LAD[3:0], LDRQ#, LFRAME#)						
Input High Current	$ILEAK_{IH}$			10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V

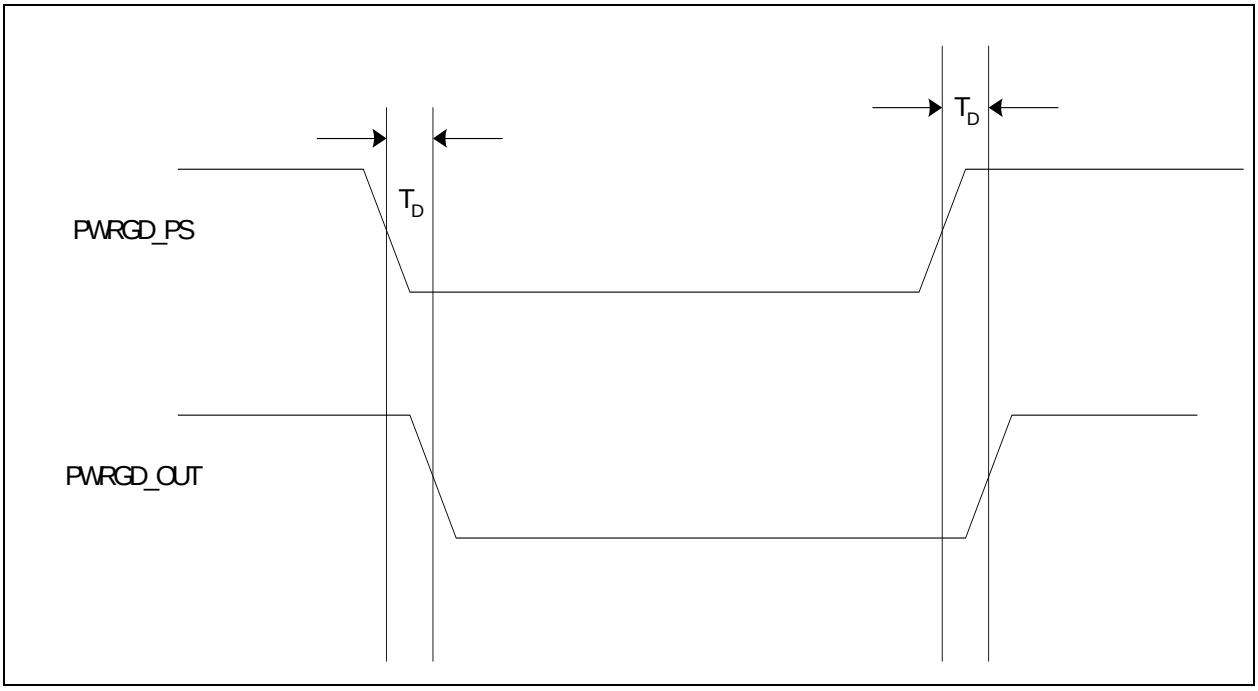
FIGURE 27-21: AMPLITUDE SHIFT-KEYED IR RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

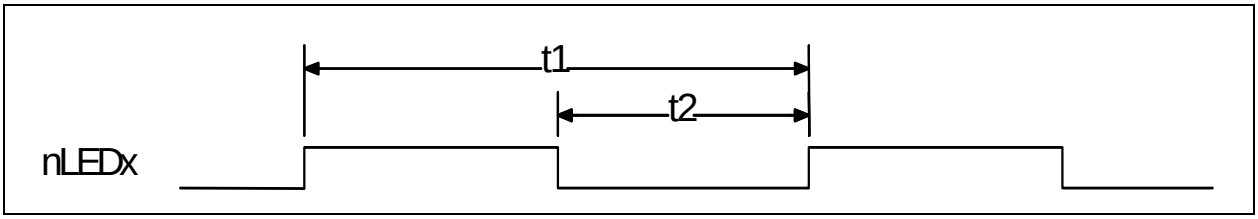
1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs



Symbol	Time			Description
	MIN	TYP	MAX	
T_D	1ηs	10ηs	20ηs	Gate Delay

27.11 nLEDx Timing

FIGURE 27-29: NLEDX TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Period		1 or 2[2]	5.88[1]	sec
t2	Blink ON Time	0	0.5[2]	1.52[1]	sec

1. These Max values are due to internal Ring Oscillator. If 1Hz blink rate is selected for LED1 pin, the range will vary from 0.33Hz to 1.0Hz. If 0.5Hz blink rate is selected for LED1 pin, the range will vary from 0.17Hz to 0.5Hz.

2. The blink rate is programmed through Bits[1:0] in LEDx register. When Bits[1:0]=00, LED is OFF. Bits[1:0]=01 indicates LED blink at 1Hz rate with a 50% duty cycle (0.5 sec ON, 0.5 sec OFF). Bits[1:0]=10 indicates LED blink at ½ Hz rate with a 25% duty cycle (0.5 sec ON, 1.5 sec OFF). When Bits[1:0]=11, LED is ON.

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