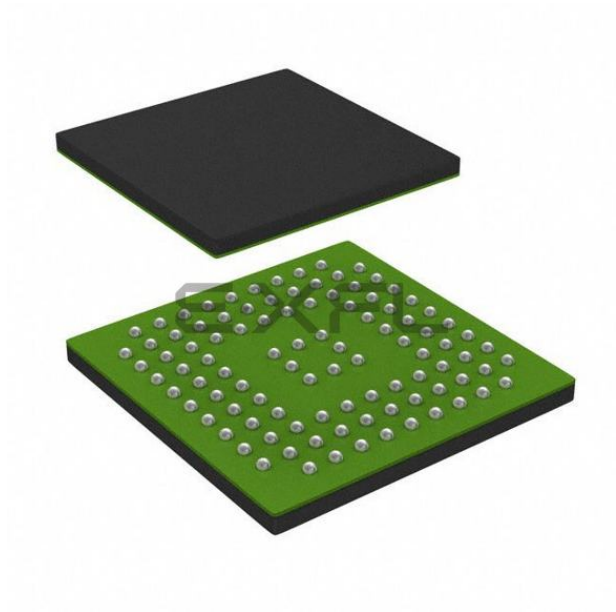

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3226-sy

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TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
B2	+2.5V_IN	+2.5V_IN
--	RESERVED=N/C[d]: E9, F9, G9, H9, J5, J6, J7, J8, J9, G3, J11, K11, L4, L10	

a. The STRAPOPT connection defines pin functions for this package, and also the contents of the Device ID register at Plug&Play Index 0x20:
When connected to VTR, the table column STRAPOPT=1 applies,
and Device ID = 0x7F.
When connected to VSS, the table column STRAPOPT=0 applies,
and Device ID = 0x7D.

b. For correct operation, this lead must always be connected to VTR.

c. For correct operation and minimal current consumption, this lead must always be connected to VSS.

d. Make No Connection to these leads.

TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
2-9	GP63* / nDCD4	GPIO with I_VID buffer Input / Data Carrier Detect 4	nDCD4	GP63*	NO GATE	(I/O8/OD8) / I
2-9	GP64* / RXD4	GPIO with I_VID buffer Input / Receive Data 4	RXD4	GP64*	NO GATE	(IS/O8/OD8) / IS
2-11, 2-9	GP65* / TXD4	GPIO with I_VID buffer Input / Transmit Data 4	TXD4	GP65*	/ HI-Z	(I/O8/OD8) / O8
2-9	GP66* / nDSR4	GPIO with I_VID buffer Input / Data Set Ready 4	nDSR4	GP66*	NO GATE	(I/O8/OD8) / I
2-9	GP67* / nRTS4	GPIO with I_VID buffer Input / Request to Send 4	nRTS4	GP67*	/ HI-Z	(I/O8/OD8) / I
2-9	GP62* / nCTS4	GPIO with I_VID buffer Input / Clear to Send 4	nCTS4	GP62*	NO GATE	(I/O8/OD8) / I
2-9	GP34 / nDTR4	GPIO (OD Only in Output Mode)/ Data Terminal Ready 4	nDTR4	GP34	/ HI-Z	(I/OD12) / O12
SERIAL PORT 5 INTERFACE						
	nSCOUT5	Serial Port 5 out control	nSCOUT5		/ HI-Z	(O8/OD8)
2-9	nSCIN5	Serial Port 5 input Control		nSCIN5	NO GATE	I
	RXD5	Receive 5	RXD5		GATE	IS
	TXD5	Serial Port 5 Transmit	TXD5		NO GATE / HI-Z	(O12.OD12)
SERIAL PORT 6 INTERFACE						
2-12	GP47 / nSCOUT6	GPIO with Schmitt trigger input Serial Port 6 output control	nSCOUT6	GP47 /	HI-Z	(IS/O4/OD4) / (O4/OD4)
2-12	GP46 / nSCIN6	GPIO with Schmitt trigger input Serial Port 6 input Control		GP46 / nSCIN6	NO GATE	(IS/O8/OD8) / (O8/OD8)
2-12	GP45 / RXD6	GPIO with Schmitt trigger input Receive serial port 6	RXD6	GATE	PG	(IS/O8/OD8) / (O8/OD8)
2-12	GP44 / TXD6	GPIO with Schmitt trigger input Serial Port 6 Transmit	TXD6	GP44	NO GATE/ Hi-Z	(IS/O4/OD4) / (O4/OD4)
PARALLEL PORT INTERFACE						
2-12	nINIT	Initiate Output	nINIT		GATE / HI-Z	(OD14/OP14)
2-12	nSLCTIN	Printer Select Input (Output to printer)	nSLCTIN		GATE / HI-Z	(OD14/OP14)
2-12	PD0	Port Data 0	PD0		GATE / HI-Z	IOP14
2-12	PD1	Port Data 1	PD1		GATE / HI-Z	IOP14
2-12	PD2	Port Data 2	PD2 /		GATE / HI-Z	IOP14

TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
2-12	nPCIRST1 / GP45	PCI Reset output 1 GPIO with Schmitt trigger input	nPCIRST1	GP45	NO GATE	(O8/OD8) / (IS/O8/OD8)
2-12	nIDE_RSTDRV / GP44	IDE Reset output GPIO with Schmitt trigger input	nIDE_RSTDRV	GP44	NO GATE	(O4/OD4) / (IS/O4/OD4)
GLUE LOGIC						
	PB_IN#	Power Button In is used to detect a power button event		PB_IN#	NO GATE	I
2-9	SLP_SX#	Sx Sleep State Input Pin.		SLP_SX#	NO GATE	I
	PB_OUT#	Power Button Out		PB_OUT#	NO GATE	O8
	PS_ON#	Power supply On		PS_ON#	NO GATE	O12
MISCELLANEOUS PINS						
	GP42/ nIO_PME	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in either S3 or S5 and below.		GP42/ nIO_PME	NO GATE	(I/O12/OD12) /(O12/OD12)
2-8, 2-9	GP60 /nLED1 /WDT	General Purpose I/O /nLED1 Watchdog Timer Output		GP60 /nLED1 /WDT	NO GATE	(I/O12/OD12) /(O12/OD12) /(O12/OD12)
	nFPRST / GP30	Front Panel Reset / General Purpose IO		nFPRST / GP30	NO GATE	ISPU_400 / (I/O4/OD4)
	PWRGD_PS	Power Good Input from Power Supply		PWRGD_PS	NO GATE	ISPU_400
	PWRGD_OUT	Power Good Output – Open Drain		PWRGD_OUT	NO GATE	OD8
	nRSMRST	Resume Reset Output		nRSMRST	NO GATE	OD24
2-8, 2-9	GP61 /nLED2 / CLKO	General Purpose I/O /nLED2 / Programmable Clock Output		GP61 /nLED2 / CLKO	NO GATE	(I/O12/OD12) / (O12/OD12) / (O12/OD12)
2-9	GP27 /nIO_SMI /P17	General Purpose I/O /System Mgt. Interrupt /8042 P17 I/O	GP27 /nIO_SMI /P17	GP27	/ HI-Z	(I/O12/OD12) /(O12/OD12) /(I/O12/OD12)
HARDWARE MONITORING BLOCK						
	nHWM_INT	Interrupt output for Hardware monitor		nHWM_INT		OD8
2-10	+5V_IN	Analog input for +5V	HVTR			I_{AN}
2-10	+2.5_IN	Analog input for +2.5V	HVTR			I_{AN}
2-10	VCCP_IN	Analog input for +Vccp (processor voltage: 1.5 V nominal).	HVTR			I_{AN}
2-10	+12V_IN	Analog input for +12V	HVTR			I_{AN}

TABLE 2-6: BUFFER DESCRIPTION (CONTINUED)

Buffer	Description
OD12	Open Drain Output, 12mA sink.
OD4	Open Drain Output, 4mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
IOD12	Input/Open Drain Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
OD_PH	Input/Output (Open Drain), See DC Electrical Characteristics on page 252
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
IO16	Input/Output 16mA sink.
IOD16	Input/Output (Open Drain), 16mA sink.
PCI_IO	Input/Output. These pins must meet the PCI 3.3V AC and DC Characteristics.
PCI_O	Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 2-16)
PCI_I	Input. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 2-16)
PCI_ICLK	Clock Input. These pins must meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2-17)
nSW	n Channel Switch (R_{on}~25 Ohms)
ISPU_400	Input with 400mV Schmitt Trigger and 30uA Integrated Pull-Up.
ISPU	Input with Schmitt Trigger and Integrated Pull-Up.

Note 2-16 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2.

Note 2-17 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2 and 4.2.3.

6.1.16 NOTES ON SERIAL PORT OPERATION

FIFO Mode Operation:

General

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

6.1.16.1 TX and RX FIFO Operation

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

6.1.16.2 TXD2 Pin

The TXD2 signal is located on the GP53/TXD2(IRTX) pin. The operation of this pin following a power cycle is defined in Section 6.2.1, "IR Transmit Pin," on page 51.

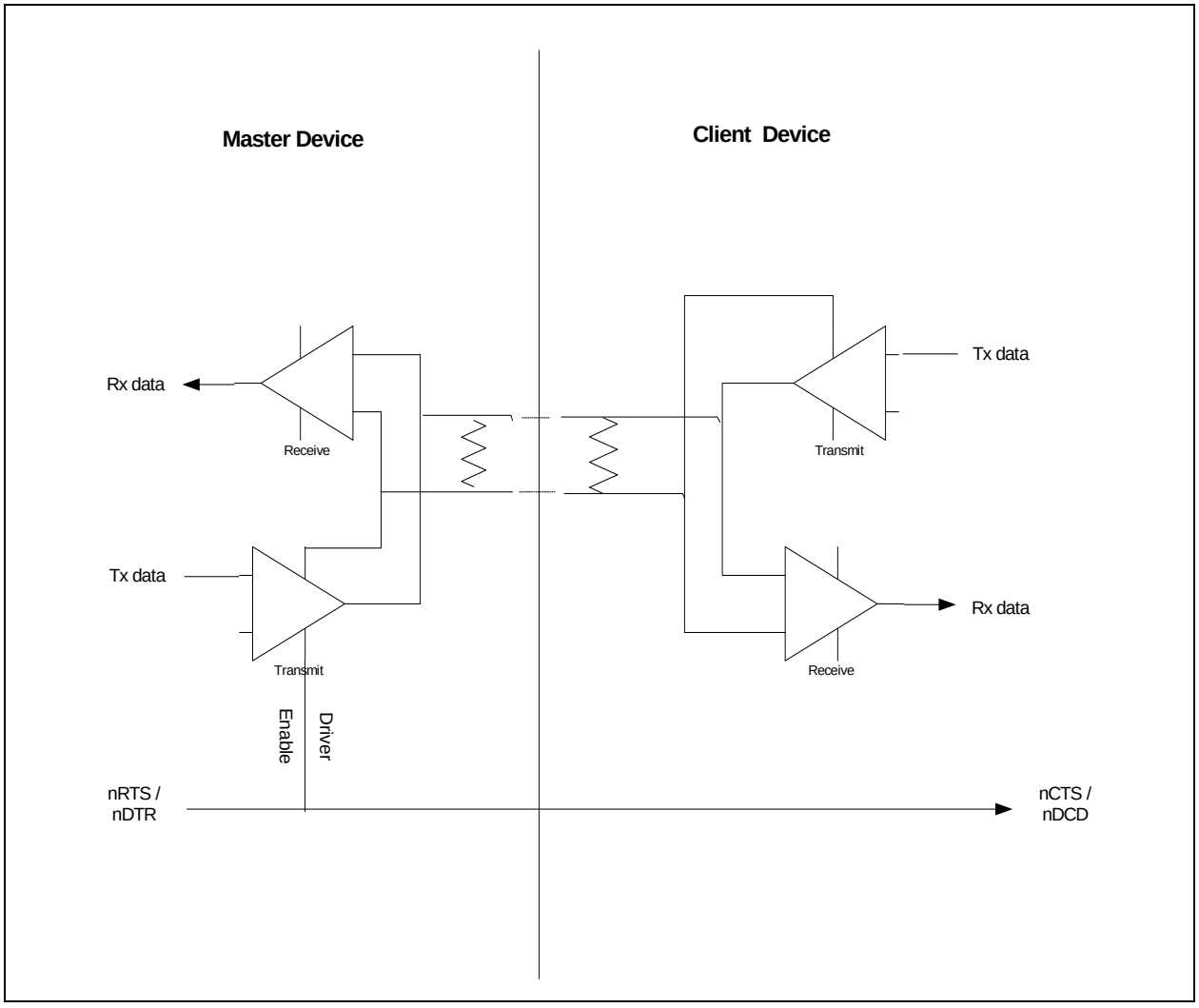
6.2 Infrared Interface

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two IR implementations have been provided for the second UART in this chip (logical device 5), IrDA and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TXD2 and RXD2 pins. These can be selected through the configuration registers.

IrDA 1.0 allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows asynchronous serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

FIGURE 6-4: HALF DUPLEX OPERATION WITH DIRECTION CONTROL



More detail on the programming of the autodirection control can be found in Section 24.0, "Runtime Register," on page 213. SP12 is the option register for Serial Port 1 and 2. SP34 is the option register for Serial Port 3 and 4. SP5 is the option register for Serial Port 5. SP6 is the option register for Serial Port 6.

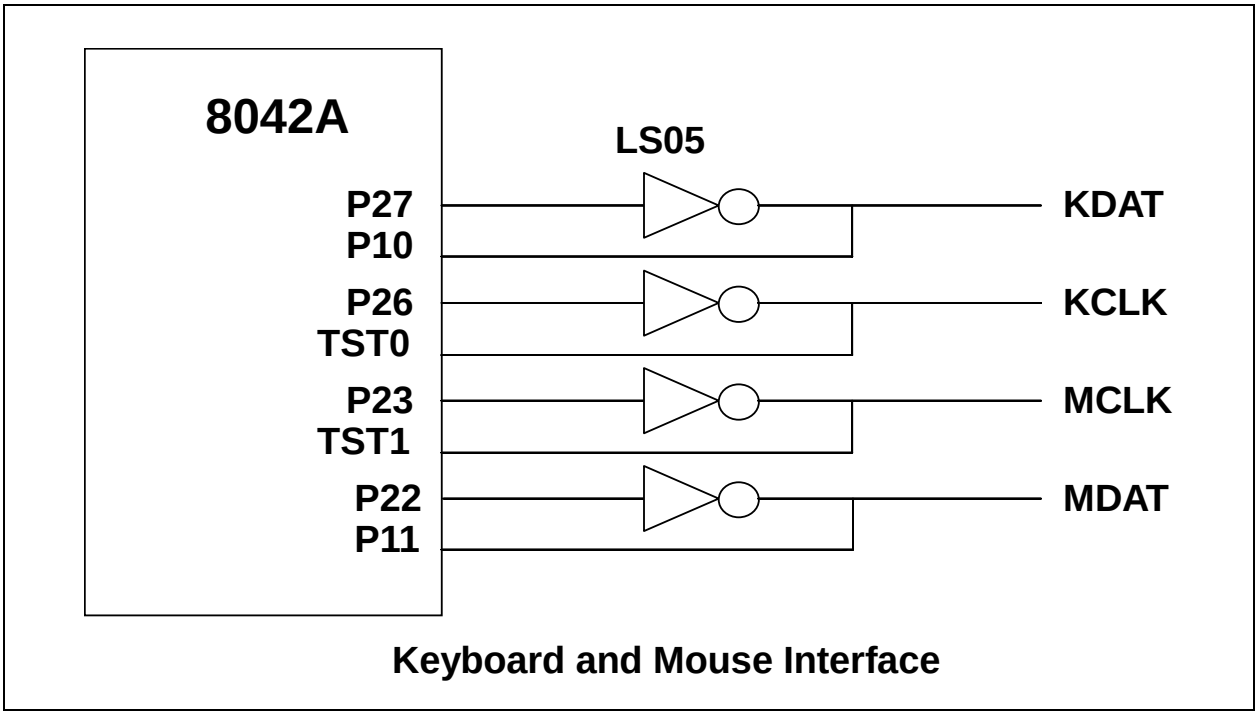
6.5 Reduced Pin Serial Ports

The SCH322x family provides for two, 4 pin serial ports (UARTs 5 and 6), which have multiplexed control signals. For each 4 pin port, there is a transmit, receive, input control and output control. The selection of the input and output control is done via a bit in the SP5/6 option register. Figure 6-5 illustrates the how programming these bits selects the corresponding control signals.

10.0 8042 KEYBOARD CONTROLLER DESCRIPTION

The SCH3227/SCH3226/SCH3224/SCH3222 is a Super I/O and Universal Keyboard Controller that is designed for intelligent keyboard management in desktop computer applications. The Universal Keyboard Controller uses an 8042 microcontroller CPU core. This section concentrates on the SCH3227/SCH3226/SCH3224/SCH3222 enhancements to the 8042. For general information about the 8042, refer to the “Hardware Description of the 8042” in the *8-Bit Embedded Controller Handbook*.

FIGURE 10-1: SCH3227/SCH3226/SCH3224/SCH3222 KEYBOARD AND MOUSE INTERFACE



KIRQ is the Keyboard IRQ

MIRQ is the Mouse IRQ

Port 21 is used to create a GATEA20 signal from the SCH3227/SCH3226/SCH3224/SCH3222.

10.1 Keyboard Interface

The SCH3227/SCH3226/SCH3224/SCH3222 LPC interface is functionally compatible with the 8042 style host interface. It consists of the D0-7 data signals; the read and write signals and the Status register, Input Data register, and Output Data register. Table 10-1 shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQs.

TABLE 10-1: I/O ADDRESS MAP

Address	Command	Block	Function (See Note)
0x60	Write	KDATA	Keyboard Data Write (C/D=0)
	Read	KDATA	Keyboard Data Read
0x64	Write	KDCTL	Keyboard Command Write (C/D=1)
	Read	KDCTL	Keyboard Status Read
Note: These registers consist of three separate 8-bit registers. Status, Data/Command Write and Data Read.			

10.2 External Keyboard and Mouse Interface

Industry-standard PC-AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the SCH3227/SCH3226/SCH3224/SCH3222 provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The SCH3227/SCH3226/SCH3224/SCH3222 has four high-drive, open-drain output, bidirectional port pins that can be used for external serial interfaces, such as external keyboard and PS/2-type mouse interfaces. They are KCLK, KDAT, MCLK, and MDAT. P26 is inverted and output as KCLK. The KCLK pin is connected to TEST0. P27 is inverted and output as KDAT. The KDAT pin is connected to P10. P23 is inverted and output as MCLK. The MCLK pin is connected to TEST1. P22 is inverted and output as MDAT. The MDAT pin is connected to P11.

Note:	External pull-ups may be required.

10.2.1 KEYBOARD/MOUSE SWAP BIT

There is a Kbd/mouse Swap bit in the Keyboard Select configuration register located at 0xF1 in Logical Device 7. This bit can be used to swap the keyboard and mouse clock and data pins into/out of the 8042. The default value of this bit is ‘0’ on VCC POR, VTR POR and PCI Reset.

1=internally swap the KCLK pin and the MCLK pin, and the KDAT pin and the MDAT pin into/out of the 8042.

0=do not swap the keyboard and mouse clock and data pins

10.3 Keyboard Power Management

The keyboard provides support for two power-saving modes: soft power-down mode and hard power-down mode. In soft power-down mode, the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the 8042 is stopped.

Soft Power-Down Mode

This mode is entered by executing a HALT instruction. The execution of program code is halted until either RESET is driven active or a data byte is written to the DBBIN register by a master CPU. If this mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RESET then a normal reset sequence is initiated and program execution starts from program memory location 0.

Hard Power-Down Mode

This mode is entered by executing a STOP instruction. The oscillator is stopped by disabling the oscillator driver cell. When either RESET is driven active or a data byte is written to the DBBIN register by a master CPU, this mode will be exited (as above). However, as the oscillator cell will require an initialization time, either RESET must be held active for sufficient time to allow the oscillator to stabilize. Program execution will resume as above.

10.4 Interrupts

The SCH3227/SCH3226/SCH3224/SCH3222 provides the two 8042 interrupts: IBF and the Timer/Counter Overflow.

10.5 Memory Configurations

The SCH3227/SCH3226/SCH3224/SCH3222 provides 2K of on-chip ROM and 256 bytes of on-chip RAM.

10.6 Register Definitions

Host I/F Data Register

The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register will load the Keyboard Data Read Buffer, set the OBF flag and set the KIRQ output if enabled. A read of this register will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the KIRQ and Status register descriptions for more information.

When using the wake on specific mouse event, it may be necessary to isolate the Mouse Port signals (MCLK, MDAT) from the 8042 prior to entering certain system sleep states. This is due to the fact that the normal operation of the 8042 can prevent the system from entering a sleep state or trigger false PME events. SCH3227/SCH3226/SCH3224/SCH3222 has an “isolation” bit for the mouse signals, which allows the mouse data signals to go into the wake-up logic but block the clock and data signals from the 8042.

When the mouse isolation bit are used, it may be necessary to reset the 8042 upon exiting the sleep state. If M_SIO bit is set prior to entering a sleep state where VCC goes inactive (S3-S5), then the 8042 must be reset upon exiting the sleep mode. Write 0x40 to global configuration register 0x2C to reset the 8042. The 8042 must then be taken out of reset by writing 0x00 to register 0x2C since the bit that resets the 8042 is not self-clearing. Caution: Bit 6 of configuration register 0x2C is used to put the 8042 into reset - do not set any of the other bits in register 0x2C, as this may produce undesired results.

TABLE 16-3: WDT OPERATION FOLLOWING VCC_POR OR WDT2_CTL WRITING

WDT2_CTL	VCC_PORB	RST_WDT2B	Counter Reset	Condition
x	0	x	Yes	Power On
0	1	1	No	State after VCC_PORB. Counter starts Counting
0->1	1	1	Yes	Write 1 to WDT2_CTL. Counter reset and starts counting.
1->0	1	1	No	Write 0 to WDT2_CTL. No affect - counter running.
x	1	0	Yes	Counter timeout under normal conditions.

16.2 Voltage Scaling and Reset Generator Tolerances

The 5V supply is scaled internally. The input resistance is 20kohms (min). The voltage trip point is 4.45V (nominal) with a tolerance of ±0.15V (range: 4.3V-4.6V).

For the 3.3V VTR and 3.3V supplies, the voltage trip point is 2.8V (nominal) with a tolerance of ±0.1V (range: 2.7V-2.9V).

Refer to FIGURE 16-1: on page 102.

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated (Table 21-1). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

TABLE 21-1: AVG[2:0] BIT DECODER

SFTR[7:5]			Measurements per Reading			Nominal Total Conversion Cycle Time (MSEC)
AVG2	AVG1	AVG0	Remote Diode 1	Remote Diode 2	Ambient	
0	0	0	128	128	8	587.4
0	0	1	16	16	1	73.4
0	1	X	16	16	16	150.8
1	X	X	32	32	32	301.5

Note: The default for the AVG[2:0] bits is ‘010’b.

21.7.1 CONTINUOUS MONITORING MODE

In the continuous monitoring mode, the sampling and conversion process is performed continuously for each temperature reading after the Start bit is set high. The time for each temperature reading is shown above for each measurement option.

The continuous monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the START bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown below (see Table 21-2). Sampling of all values occurs in a nominal 150.8 ms (default - see Table 21-2).

TABLE 21-2: ADC CONVERSION SEQUENCE

Sampling Order	Register
1	Remote Diode Temp Reading 1
2	Ambient Temperature reading
3	Remote Diode Temp Reading 2

When the continuous monitoring function is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 150.8 ms (default - see Table 21-2). Each measured value is compared to values stored in the Limit registers. When the measured value violates the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly.

The results of the sampling and conversions can be found in the Reading Registers and are available at any time.

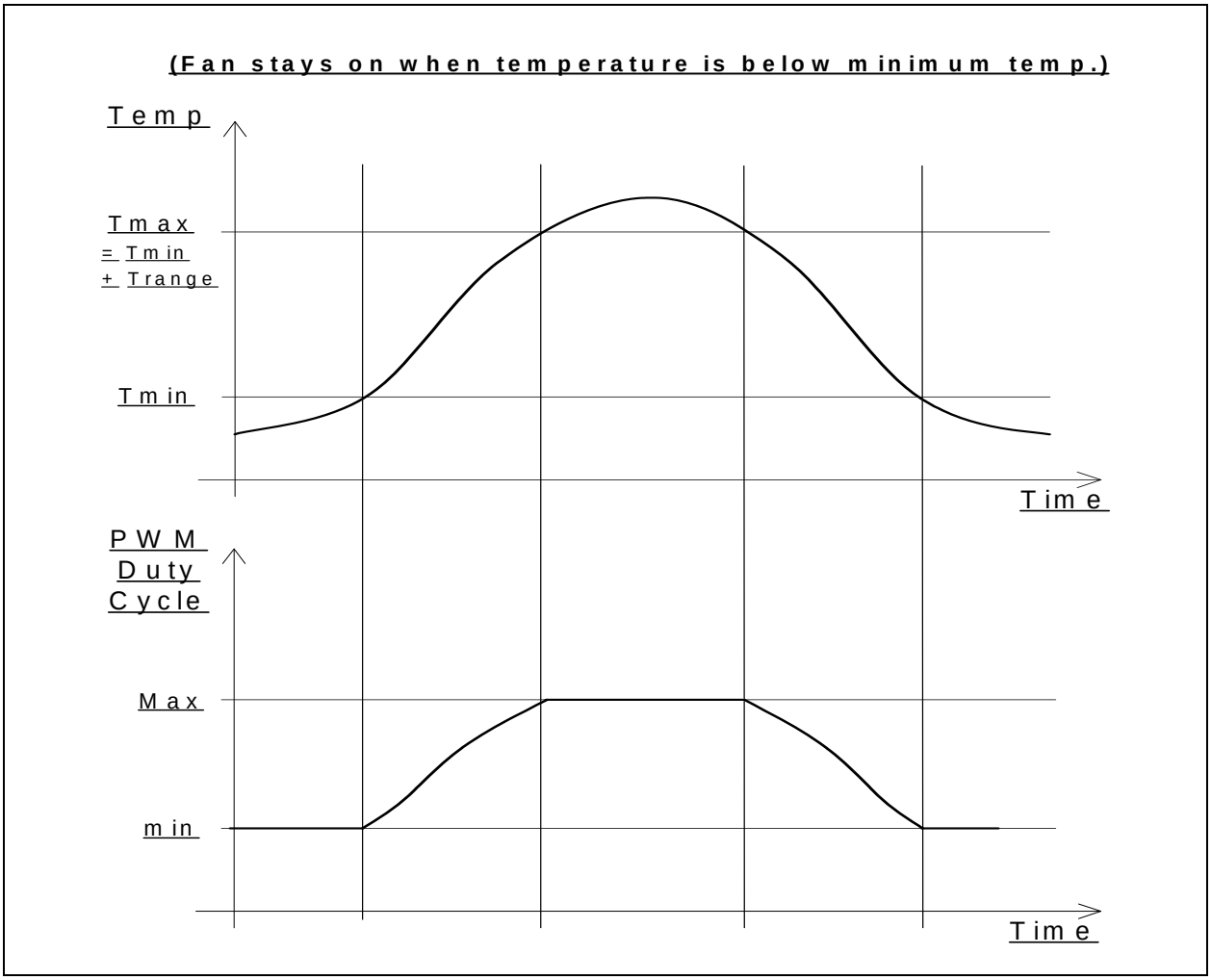
21.7.2 CYCLE MONITORING MODE

In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.151 seconds (1.3 sec max - default averaging enabled). The sampling and conversion of each temperature reading is performed once every monitoring cycle. This is a power saving mode.

The cycle monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown above.

When the cycle monitoring function is started, it cycles through each measurement in sequence, and it produces a converted temperature reading for each input. The state machine waits approximately one second before repeating this process. Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

FIGURE 21-5: AUTOMATIC FAN CONTROL



21.13.3.3 Spin Up

When a fan is being started from a stationary state (PWM duty cycle =00h), the part will cause the fan to “spin up” by going to 100% duty cycle for a programmable amount of time to overcome the inertia of the fan (i.e., to get the fan turning). Following this spin up time, the fan will go to the duty cycle computed by the auto fan algorithm.

During spin-up, the PWM duty cycle is reported as 0%.

To limit the spin-up time and thereby reduce fan noise, the part uses feedback from the tachometers to determine when each fan has started spinning properly. The following tachometer feedback is included into the auto fan algorithm during spin-up.

Auto Fan operation during Spin Up:

The PWM goes to 100% duty cycle until the tachometer reading register is below the minimum limit (see Figure 21-6), or the spin-up time expires, whichever comes first. This causes spin-up to continue until the tachometer enters the valid count range, unless the spin up time expires. If the spin up expires before the tachometer enters the valid range, an interrupt status bit will be set once spin-up expires. Note that more than one tachometer may be associated with a PWM, in which case all tachometers associated with a PWM must be in the valid range for spin-up to end.

duty cycle will be held constant for a minimum of 18 periods (206/11.4 = 18.07) until the Ramp Logic increments/decrements the actual PWM duty cycle by '1'.

- If the period of the PWM output is greater than the step size created by the PWM Ramp Rate, the ramp rate logic will force the PWM output to increment/decrement the actual duty cycle in increments larger than 1/255. For example, if the PWM frequency is 11Hz (1/11Hz = 90.9msec) and the PWM Step time is 5msec, the PWM duty cycle output will be incremented 18 or 19 out of 255 (i.e., 90.9/5 = 18.18) until it reaches the calculated duty cycle. Note that the step size may be less if the calculated duty cycle minus the actual duty cycle is less than 18.

Note: The calculated PWM Duty cycle reacts immediately to a change in the temperature reading value. The temperature reading value may be updated once in 105.8msec (default) (see Table 21-2, "ADC Conversion Sequence," on page 126). The internal PWM duty cycle generated by the Ramp Rate control logic gradually ramps up/down to the calculated duty cycle at a rate pre-determined by the value programmed in the PWM Ramp Rate Control bits. The PWM output latches the internal duty cycle generated by the Ramp Rate Control Block every 1/(PWM frequency) seconds to determine the actual duty cycle of the PWM output pin.

PWM Output Transition from OFF to ON

When the calculated PWM Duty cycle generated by the auto fan control logic transitions from the 'OFF' state to the 'ON' state (i.e., Current PWM duty cycle>00h), the internal PWM duty cycle in the Ramp Rate Control Logic is initialized to the calculated duty cycle without any ramp time and the PWMx Current Duty Cycle register is set to this value. The PWM output will latch the current duty cycle value in the Ramp Rate Control block to control the PWM output.

PWM Output Transition from ON to OFF

Each PWM output has a control bit to determine if the PWM output will transition immediately to the OFF state (default) or if it will gradually step down to Off at the programmed Ramp Rate. These control bits (SZEN) are located in the PWMx Options registers at offsets 94h-96h.

TABLE 21-4: PWM RAMP RATE

RRx-[2:0]	PWM Ramp Time (sec) (Time from 33% Duty Cycle to 100% Duty Cycle)	PWM Ramp Time (sec) (Time from 0% Duty Cycle to 100% Duty Cycle)	Time per PWM Step (PWM Step Size = 1/255)	PWM Ramp Rate (Hz)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

TABLE 22-13: TEMPERATURE LIMIT VS. REGISTER SETTING

Limit	Limit (DEC)	Limit (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh

22.2.20 REGISTERS 6A-6CH: ABSOLUTE TEMPERATURE LIMIT

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan mode, if any zone associated with a PWM output exceeds the temperature set in the Absolute limit register, all PWM outputs will increase their duty cycle to 100% except those that are disabled via the PWM Configuration registers. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event.

If an absolute limit register set to 80h (-128°c), the safety feature is disabled for the associated zone. That is, if 80h is written into the Zone x Temp Absolute Limit Register, then regardless of the reading register for the zone, the fans will not turn on-full based on the absolute temp condition.

Default =100°c=64h.

When any fan is in auto fan mode, then if the temperature in any zone exceeds absolute limit, all fans go to full, including any in manual mode, except those that are disabled. Therefore, even if a zone is not associated with a fan, if that zone exceeds absolute, then all fans go to full. In this case, the absolute limit can be chosen to be 7Fh for those zones that are not associated with a fan, so that the fans won't turn on unless the temperature hits 127 degrees.

TABLE 22-14: ABSOLUTE LIMIT VS. REGISTER SETTING

Absolute Limit	Abs Limit (DEC)	Abs Limit (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h

22.2.64 REGISTERS C4-C5, C9H: THERMTRIP TEMPERATURE LIMIT ZONE REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C4h	R/W	THERMTRIP Temp Limit ZONE 1 (Remote Diode 1)	7	6	5	4	3	2	1	0	7Fh
C9h	R/W	THERMTRIP Temp Limit ZONE 2 (Ambient)	7	6	5	4	3	2	1	0	7Fh
C5h	R/W	THERMTRIP Temp Limit ZONE 3 (Remote Diode 2)	7	6	5	4	3	2	1	0	7Fh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated THERMTRIP temperature limit (THERMTRIP Temp Limit ZONES 1-3). The THERMTRIP temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Temp Limit ZONE 1-3 registers represent the upper temperature limit for asserting nTHERMTRIP pin for each zone. These registers are defined as follows:

If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit ZONE 1-3 registers, the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERMTRIP Output Enable register).

Note: The zone must exceed the limits set in the associated THERMTRIP Temp Limit ZONE 1-3 register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

22.2.65 REGISTER CAH: THERMTRIP STATUS REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CAh	R/WC	THERMTRIP Status	RES	RES	RES	RES	RES	RD 2	RD 1	AMB	00h
Note:	Each bit in this register is cleared on a write of 1 if the event is not active.										

Note: This register is reset to its default value when the PWRGD_PS signal transitions high.

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to ‘1’ if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

22.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default).

23.0 CONFIGURATION REGISTERS

The Configuration of the SCH322x is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The SCH322x is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the SCH322x allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder

After a PCI Reset or Vcc Power On Reset the SCH322x is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the SCH322x into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the SCH322x Is in Configuration Mode.

Strap options must be added to allow four Configuration Register Base Address options: 0x002E, 0x004E, 0x162E, or 0x164E. At the deasserting edge of PCIRST# or VCC POR the nRTS1/SYSOPT0 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[7:0]= 0x2E
- 1 = Index Base I/O Address bits A[7:0]= 0x4E

At the deasserting edge of PCIRST# or VCC POR the nDTR1/SYSOPT1 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[15:8]= 0x16;
- 1 = Index Base I/O Address bits A[15:8]= 0x00

bit The above strap options will allow the Configuration Access Ports (CONFIG PORT, the INDEX PORT, and DATA PORT) to be controlled by the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins and by the Configuration Port Base Address registers at offset 0x26 and 0x27. The configuration base address at power-up is determined by the SYSOPT strap option. The SYSOPT strap option is latched state of the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins at the deasserting edge of PCIRST#. The nRTS1/SYSOPT0 pin determines the lower byte of the Base Address and the nDTR1/SYSOPT1 pin determines the upper byte of the Base Address. The following table summarizes the Base Configuration address selected by the SYSOPT strap option.

TABLE 23-1: SYSOPT STRAP OPTION CONFIGURATION ADDRESS SELECT

SYSOPT1	SYSOPT0	Default CONFIG PORT/ Index Port Address	Data Port
1	0	0x002E	INDEX PORT + 1
1	1	0x004E	
0	0	0x162E	
0	1	0x164E	

APPLICATION NOTE: The nRTS1/SYSOPT0 and the nDTR1/SYSOPT1 pins requires external pullup/pulldown resistors to set the default base I/O address for configuration to 0x002E, 0x004E, 0x162E, or 0x164E.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

Note 23-1 The configuration port base address can be relocated through CR26 and CR27.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

Exiting the Configuration State

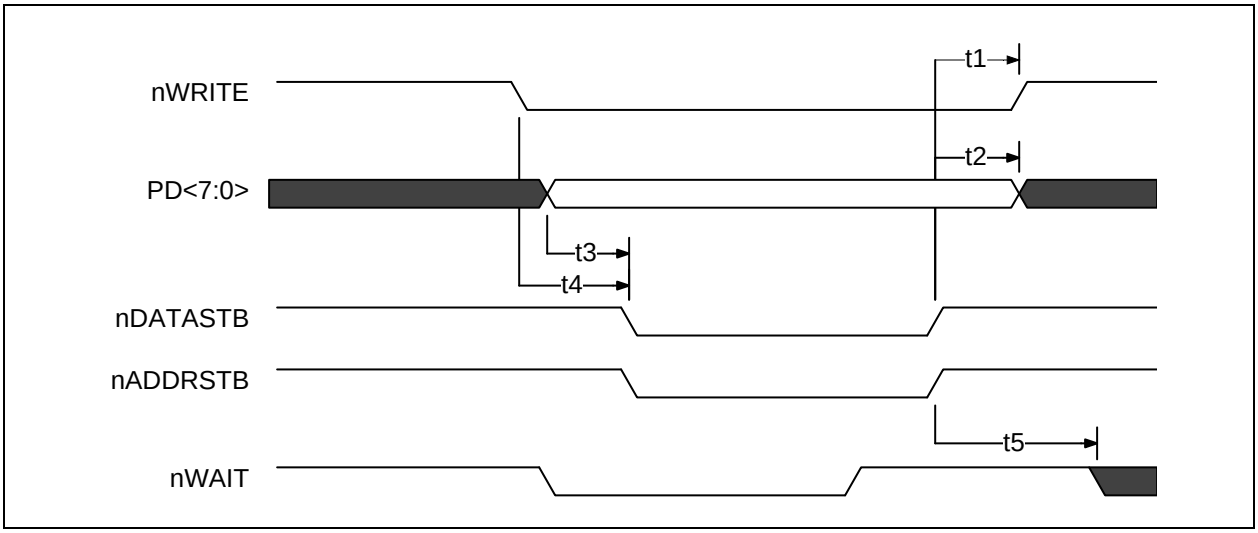
The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

TABLE 23-3: CONFIGURATION REGISTER SUMMARY (CONTINUED)

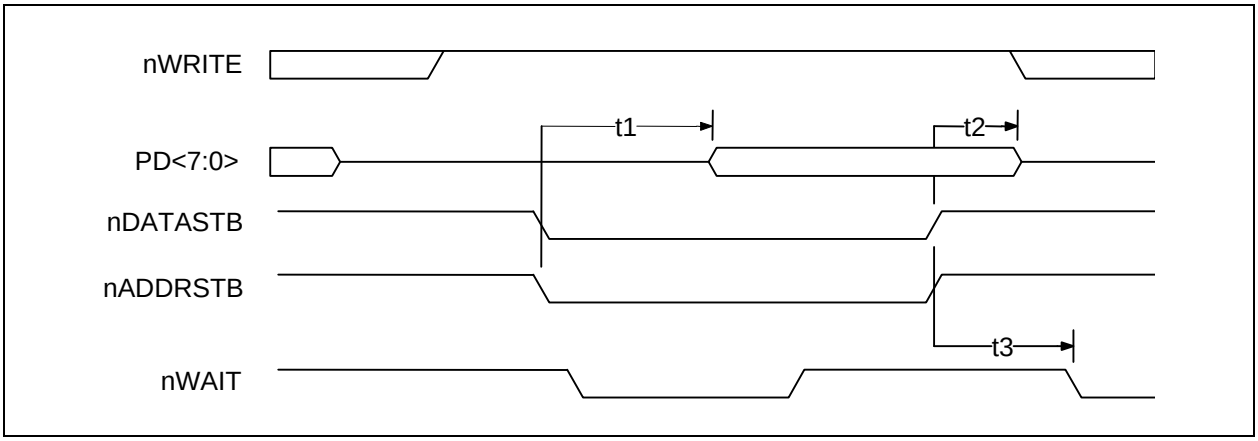
Index	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Configuration Register
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 2 Mode Register
0xF1	R/W	0x02	0x02	0x02	-	IR Options Register
0xF2	R/W	0x03	0x03	0x03	-	IR Half Duplex Timeout
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (KEYBOARD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select (Keyboard)
0x72	R/W	0x00	0x00	0x00	0x00	Secondary Interrupt Select (Mouse)
0xF0	R/W	0x00	0x00	0x00	-	KRESET and GateA20 Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE A CONFIGURATION REGISTERS (RUNTIME REGISTERS)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x62	R/W	0x00	0x00	0x00	0x00	Secondary Base I/O Address High Byte
0x63	R/W	0x00	0x00	0x00	0x00	Secondary Base I/O Address Low Byte
0XF0	R/W	-	-	0X00	-	CLOCKI32
0xF1	R/W	0x00	0x00	0x00	0x00	RESERVED: do not write.
0XF2	RW / R	0x04	0x04	0x04	-	Security Key Control Register
LOGICAL DEVICE B CONFIGURATION REGISTERS (SERIAL PORT 3) AVAILABLE IN SCH3227, SCH3226, SCH3222 RESERVED IN SCH3224						
0x30	R/W	0x00	0x00	0x00	0x00	Activate Note 23-2
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 3 Mode Register
LOGICAL DEVICE C CONFIGURATION REGISTERS (SERIAL PORT 4) AVAILABLE IN SCH3227, SCH3226, SCH3222 RESERVED IN SCH3224						
0x30	R/W	0x00	0x00	0x00	0x00	Activate Note 23-2
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte

FIGURE 27-14: EPP 1.7 DATA OR ADDRESS WRITE CYCLE



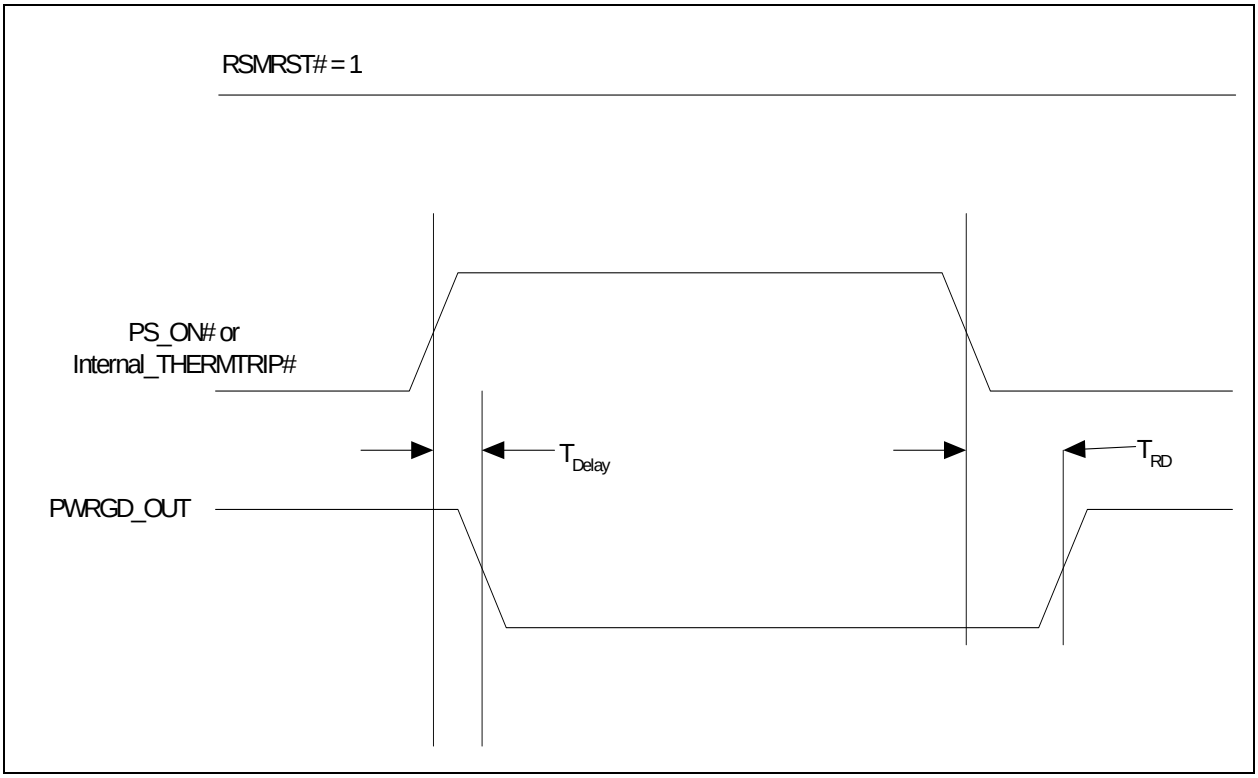
Name	Description	MIN	TYP	MAX	Units
t1	Command Deasserted to nWRITE Change	0		40	ns
t2	Command Deasserted to PDATA Invalid	50			ns
t3	PDATA Valid to Command Asserted	10		35	ns
t4	nWRITE to Command	5		35	ns
t5	Command Deasserted to nWAIT Deasserted	0			ns

FIGURE 27-15: EPP 1.7 DATA OR ADDRESS READ CYCLE



Name	Description	MIN	TYP	MAX	Units
t1	Command Asserted to PDATA Valid	0			ns
t2	Command Deasserted to PDATA Hi-Z	0			ns
t3	Command Deasserted to nWAIT Deasserted	0			ns

FIGURE 27-28: PWG_OUT VS. PS_ON# SIGNAL NEGATION



Symbol	Time			Description
	MIN	TYP	MAX	
T_{Delay}	188ms	200ms	212ms	The delay time is from the falling edge of PS_ON# to the rising edge of PWRGD_OUT. This delay is selected via a strapping option. Default value is 200ms.
	470ms	500ms	530ms	
T_{FD}	15ηs		30ηs	