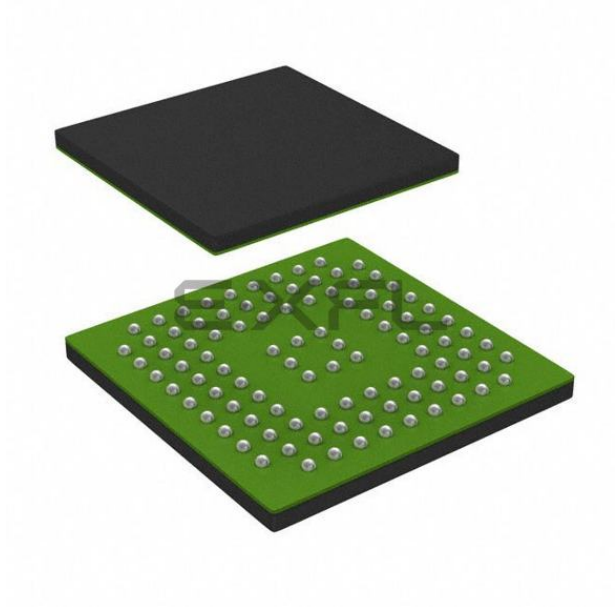

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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3226i-sy-tr

Table of Contents

1.0 GENERAL DESCRIPTION

The SCH3227/SCH3226/SCH3224/SCH3222 Product Family is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. The Product Family also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

1.1 Scope and Definitions

For the purposes of this document, the term “SCH322x Family” refers only to the parts numbered SCH3227, SCH3226, SCH3224 and SCH3222. Similarly-numbered parts may also exist, but they are outside the scope of this document.

1.2 Important New Usage Considerations

The SCH322x Family is the next generation of the SCH311x family components. They mainly differ in the number of pins brought out of the package. In some cases (SCH3227, SCH3226) a new pin called STRAPOPT is brought out, allowing a hard-wired selection between the legacy SCH3114 vs. SCH3116 features of 8 of the pins. This selection also affects the Device ID register, which will display the legacy SCH3114 or SCH3116 code. Other SCH322x members, which do not have a STRAPOPT pin, are hard-wired internally to identify themselves as the legacy SCH3116.

CAUTION: This device contains circuits and registers affecting pin functions which must not be used when they are not brought out of the package. These pins are pulled to known states internally. Any features, especially Logical Devices and GPIOs, that are not listed in this document for a particular family member must not be activated, accessed, or in any way changed from its default reset state. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system. See Table 2-1 SCH3227, Table 2-2 SCH3226, Table 2-3 SCH3224, or Table 2-4 SCH3222, for the pin features that are brought out.

1.3 Feature Sets

See Table 1-1 on page 5 for features available per family member.

The Product Family is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard.

The Product Family supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, hardware IRQ and DMA Channel of each Logical Device may be reprogrammed through the internal configuration registers. There are up to 480 I/O address location options (960 for the Parallel Port), a Serialized IRQ interface, and a choice of three Legacy DMA channel assignments.

Super I/O functionality includes an 8042 based keyboard and mouse controller, one IrDA 1.0 infrared port and multiple serial ports. Some family members (Table 1-1) also provide an IEEE 1284 EPP/ECP compatible parallel port.

The serial ports are fully functional NS16550 compatible UARTs that support data rates up to 1.5 Mbps. There are both 8-pin Serial Ports and 4-pin Serial Ports. The reduced-pin serial ports have selectable input and output controls. The Serial Ports contain programmable direction control, which will automatically drive nRTS when the Output Buffer is loaded, then drive nRTS when the Output Buffer is empty.

Hardware Monitoring capability has programmable, automatic fan control. Three fan tachometer inputs and three pulse width modulator (PWM) fan control outputs are available.

Hardware Monitoring capability also includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans in response. There are four analog inputs for monitoring external voltages of +5V, +2.5V, +12V and Vccp (core processor voltage), as well as internal monitoring of the device’s internal VCC, VTR, and VBAT power supplies. Hardware Monitoring includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring local ambient temperature. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and fan speed conditions. Hardware Monitoring features are accessible via the LPC bus, and the same interrupt event reported on the nHWM_INT pin also creates PME wakeup events. A separate THERMTRIP output is available, which generates a pulse output on a programmed over-temperature condition. This can be used to generate a reset or shutdown indication to the system.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, a programmable Clock output, and reset generation. The reset generation includes a watchdog timer which can be used to generate a reset pulse. The width of this pulse is selectable via an external strapping option.

System related functionality, which offers flexibility to the system designer, includes General Purpose I/O control functions, and control of two LED's.

TABLE 2-3: SCH3224 SUMMARY (CONTINUED)

Ball#	Function[a]
C7	SLCT
E7	PE
L8	BUSY
K8	nACK
J8	nERROR
G11	nALF
K9	nSTROBE
L10	nRI1
J9	nDCD1
K10	RXD1
K11	TXD1 / SIOXNOROUT
J10	nDSR1
J11	nRTS1 / SYSOPT0
H9	nCTS1
H10	nDTR1 / SYSOPT1
H11	GP50 / nRI2
L9	VTR
L7	VSS
G9	GP51 / nDCD2
G10	GP52 / RXD2(IRRX2)
F11	GP53 / TXD2(IRTX2)
F10	GP54 / nDSR2
E11	GP55 / nRTS2 / RESGEN
D11	GP56 / nCTS2
F9	GP57 / nDTR2
D10	RXD5
B11	TXD5
E9	nSCOUT5
D9	nSCIN5
C11	GP42 / nIO_PME
E10	VTR
B10	GP61 / nLED2 / CLKO
C9	GP60 / nLED1 / WDT
C1	CLKI32
B9	nRSMRST
A10	VSS
C8	PWRGD_OUT
A9	PWRGD_PS
B8	nFPRST / GP30
F7	VTR
C6	VSS
B7	nTHERMTRIP
A8	nHWM_INT
A7	PWM3

3.0 BLOCK DIAGRAM

FIGURE 3-1: SCH322X BLOCK DIAGRAM

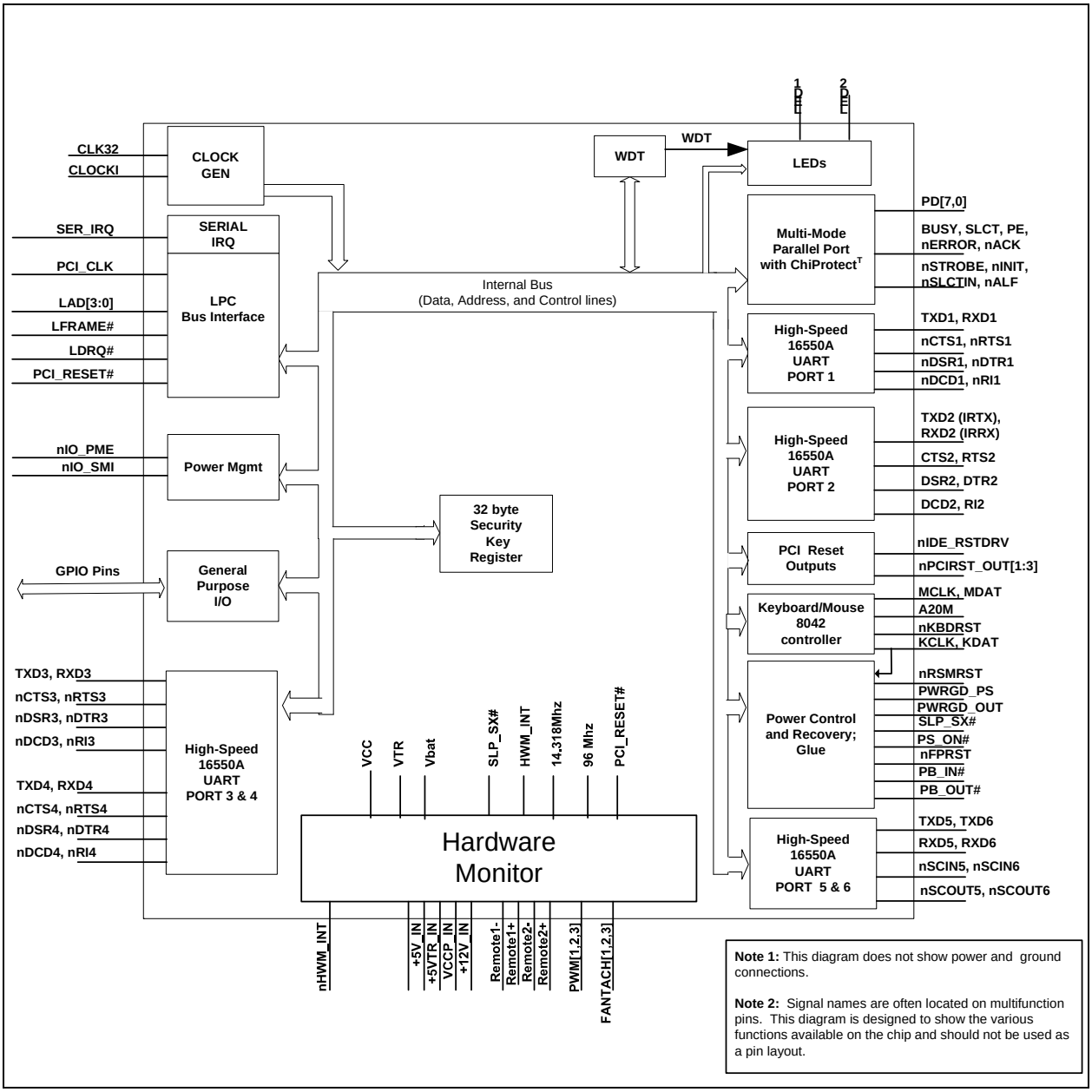


TABLE 7-6: EXTENDED CONTROL REGISTER (A)

R/W	Mode
000:	Standard Parallel Port Mode. In this mode the FIFO is reset and common drain drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register L3-CRF0. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

TABLE 7-7: EXTENDED CONTROL REGISTER (B)

IRQ Selected	Config REG B Bits 5:3
15	110
14	101
11	100
10	011
9	010
7	001
5	111
All others	000

TABLE 7-8: EXTENDED CONTROL REGISTER (C)

IRQ Selected	Config REG B Bits 5:3
3	011
2	010
1	001
All others	000

7.2.7 OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Case 1: Keyboard and/or Mouse Powered by VTR

The KBD and/or MOUSE status bits will be set upon a VTR POR if the keyboard and/or mouse are powered by VTR.

In this case, a nIO_PME will not be generated, since the keyboard and mouse PME enable bits are reset to zero on a VTR POR. The BIOS software needs to clear these PME status bits after power-up.

In this case, an nIO_PME will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are Bvat powered. Therefore, if the keyboard and mouse are powered by VTR, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VTR is removed (i.e., S4 or S5) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME and/or wake events from the power states S3 or below.

Case 2: Keyboard and/or Mouse Powered by VCC

The KBD and/or MOUSE status bits will be set upon a VCC POR if the keyboard and/or mouse are powered by VCC. In this case, a nIO_PME and a nIO_PME will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are VTRor Vbat powered. Therefore, if the keyboard and mouse are powered by VCC, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VCC is removed (i.e., S3) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME and/or wake events from the S0 and/or S1 states. The BIOS software needs to clear these PME status bits after power-up.

18.3.2 POWER SUPPLY TIMING DIAGRAMS

The following diagrams show the relative timing for the I/O pins associated with the Power Control logic. These are conceptual diagrams to show the flow of events.

FIGURE 18-3: POWER SUPPLY DURING NORMAL OPERATION

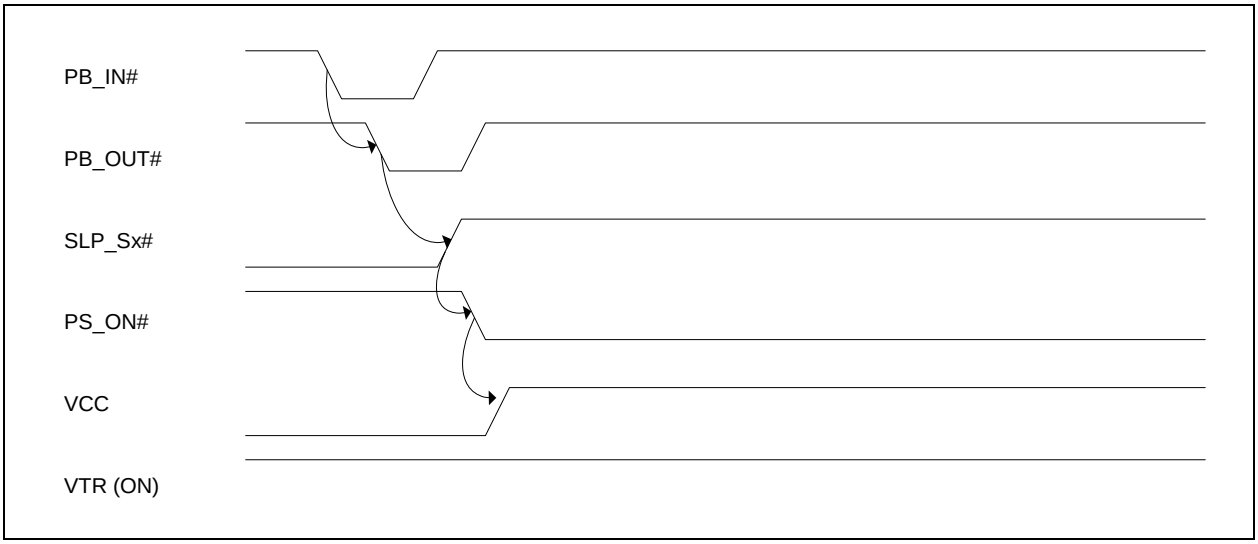
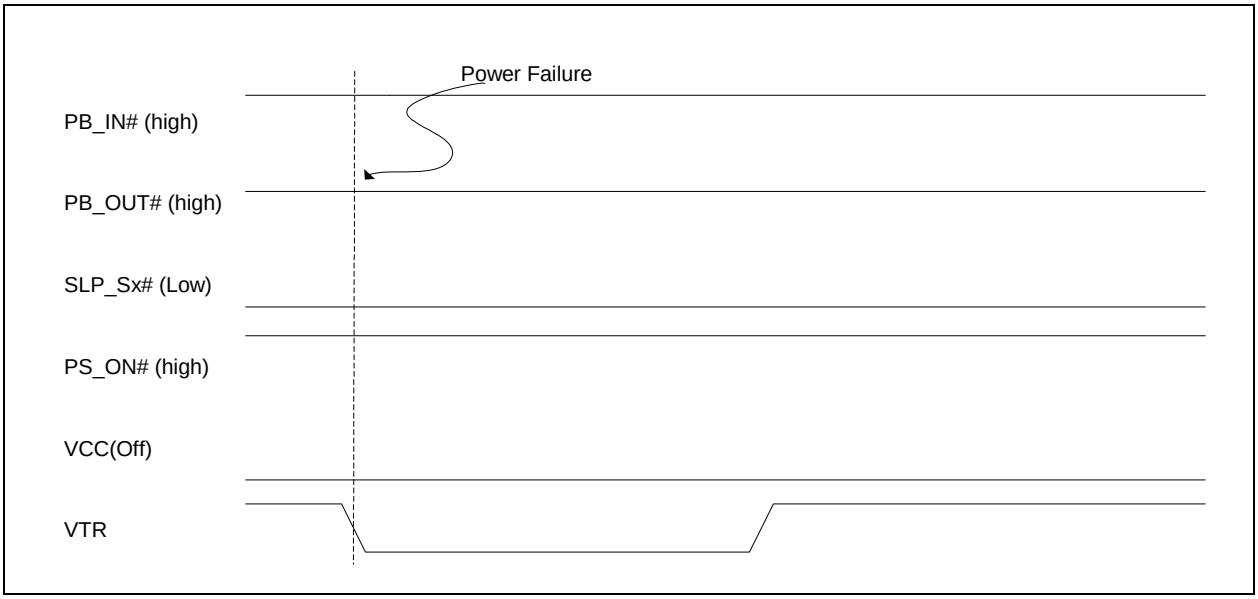


FIGURE 18-4: POWER SUPPLY AFTER POWER FAILURE (RETURN TO OFF)



The state machine used to snoop the incoming data from the keyboard is synchronized by the clock high and low time. If the KCLK signal remains high or low for a nominal 125usec during the transmission of a byte, a timeout event is generated causing the snooping and scan code decoding logic to be reset, such that it will look for the first byte of the make or break scan code.

18.5.1.2 Description Of SCAN 1 and SCAN 2

SCAN 1:

Many standard keyboards (PC/XT, MFII, etc.) generate scan 1 make and break codes per key press. These codes may be generated as a single byte or multi-byte sequences. If a single byte is generated, the make code, which is used to indicate when a key is pressed, is a value between 0h and 7Fh. The break code, which is used to indicate when a key is released, is equal to the make code plus 80h (i.e. 80h ≤ Break Code ≤ FFh). If a multi-byte sequence is sent it will send E0h before the make or break.

Example of Single Byte Scan 1: Make Code = 37h, Break Code=B7h

Example of Multi-byte Scan 1: Make Code = E0h 37h, Break Code = E0h B7h.

SCAN 2:

The scan 2 make and break codes used in AT and PS/2 keyboards, which are defined by the PC 8042 Keyboard Controller, use the same scan code when a key is pressed and when the key is released. A reserved release code, 0xF0, is sent by the keyboard immediately before the key specific portion of the scan code to indicate when that the key is released.

Example of Single Byte Scan 2: Make Code = 37h, Break Code=F0h 37h

Example of Multi-byte Scan 2: Make Code = E0h 37h, Break Code = E0h F0h 37h.

18.5.2 SYSTEM FOR DECODING SCAN CODE MAKE BYTES RECEIVED FROM THE KEYBOARD

Bit [3:2] of the SPEKEY Scan Code register is used to determine if the hardware is required to detect a single byte make code or a multi-byte make code. Table 18-4 summarizes how single byte and multi-byte scan codes are decoded.

FIGURE 18-6: SAMPLE SINGLE-BYTE MAKE CODE

Keyboard Scan Code - Make Byte 1
37h

FIGURE 18-7: SAMPLE MULTI-BYTE MAKE CODE

MSB	LSB
Keyboard Scan Code - Make Byte 1	Keyboard Scan Code - Make Byte 2
E0h	37h

Note: In multi-byte scan codes the most significant byte (MSB) will be received first.

20.0 BATTERY BACKED SECURITY KEY REGISTER

Located at the Secondary Base I/O Address of Logical Device A is a 32 byte CMOS memory register dedicated to security key storage. This security key register is battery powered and has the option to be read protected, write protected, and lockable. The Secondary Base I/O Address is programmable at offsets 0x62 and 0x63. See Table 20-1, "Security Key Register Summary" is a complete list of the Security Key registers.

TABLE 20-1: SECURITY KEY REGISTER SUMMARY

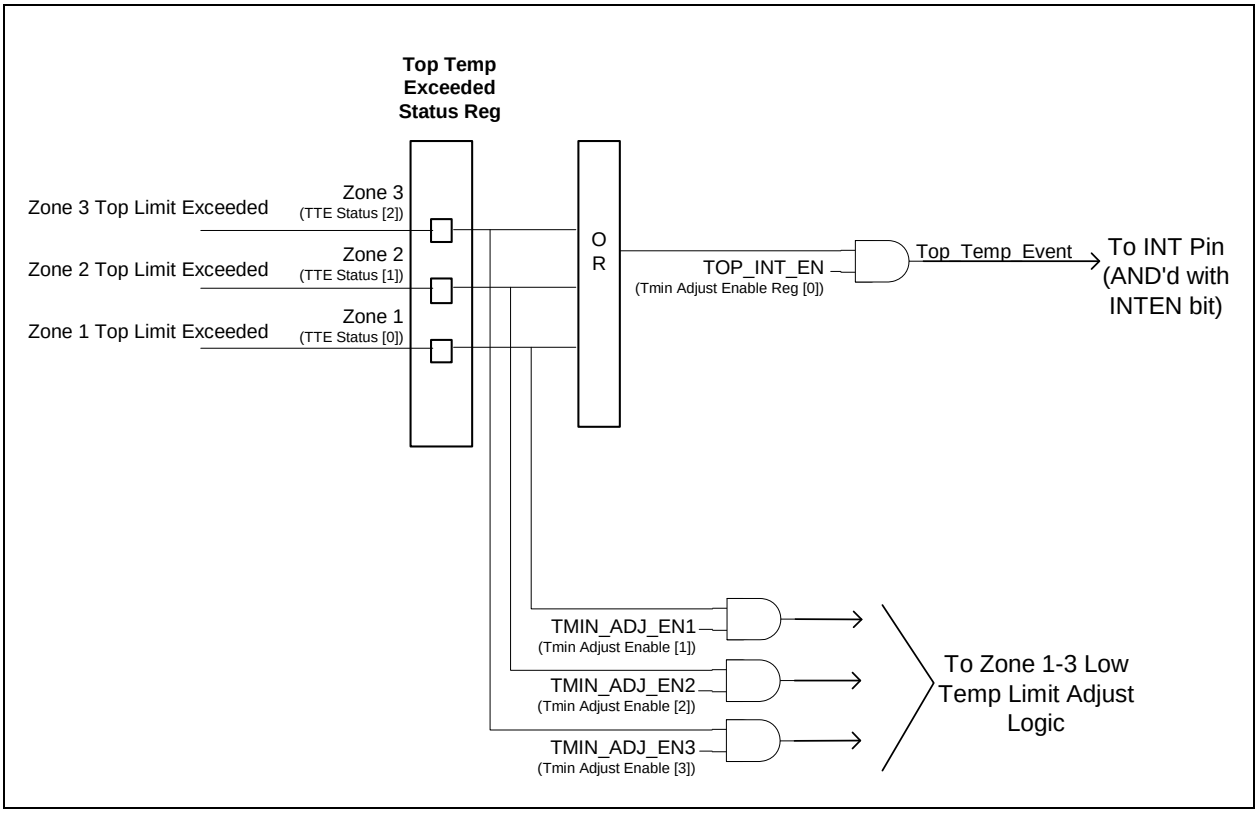
Register Offset (HEX)	VBAT POR	Register
00	0x00	Security Key Byte 0
01	0x00	Security Key Byte 1
02	0x00	Security Key Byte 2
03	0x00	Security Key Byte 3
04	0x00	Security Key Byte 4
05	0x00	Security Key Byte 5
06	0x00	Security Key Byte 6
07	0x00	Security Key Byte 7
08	0x00	Security Key Byte 8
09	0x00	Security Key Byte 9
0A	0x00	Security Key Byte 10
0B	0x00	Security Key Byte 11
0C	0x00	Security Key Byte 12
0D	0x00	Security Key Byte 13
0E	0x00	Security Key Byte 14
0F	0x00	Security Key Byte 15
10	0x00	Security Key Byte 16
11	0x00	Security Key Byte 17
12	0x00	Security Key Byte 18
13	0x00	Security Key Byte 19
14	0x00	Security Key Byte 20
15	0x00	Security Key Byte 21
16	0x00	Security Key Byte 22
17	0x00	Security Key Byte 23
18	0x00	Security Key Byte 24
19	0x00	Security Key Byte 25
1A	0x00	Security Key Byte 26
1B	0x00	Security Key Byte 27
1C	0x00	Security Key Byte 28
1D	0x00	Security Key Byte 29
1E	0x00	Security Key Byte 30
1F	0x00	Security Key Byte 31

Access to the Security Key register block is controlled by bits [2:1] of the Security Key Control (SKC) Register located in the Configuration Register block, Logical Device A, at offset 0xF2. The following table summarizes the function of these bits.

21.13.5.1.1 Interrupt Generation

The following figure illustrates the operation of the interrupt mapping for the AMTA feature in relation to the status bits and enable bits.

FIGURE 21-14: AMTA INTERRUPT MAPPING



21.14 nTHERMTRIP

The nTHERMTRIP output pin can be configured to assert when any of the temperature sensors (remote diodes 1-2, internal) is above its associated temperature limit.

The Thermtrip Enable register at offset CEh selects which reading(s) will cause the nTHERMTRIP signal to be active, when the selected temperature(s) exceed in the associated limit registers (C4h for Remote Diode 1, C5h for Remote diode 2, and C9h for Ambient temp) their pre-programmed limit.

An internal version of this output will also be used by the RESGEN block to generate a system reset pulse. More details can be found in Section 16.0, "Reset Generation," on page 101.

21.14.1 NTHERMTRIP OPERATION

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated nTHERMTRIP temperature limit (THERMTRIP Temp Limit Zone[3:1]). The Thermtrip temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Limit Zone[3:1] registers represent the upper temperature limit for asserting nTHERMTRIP for each zone. These registers are defined as follows: If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit Zone[3:1], the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERM Output Enable register).

Each zone may be individually enabled to assert the nTHERMTRIP pin (as an output).

The zone must exceed the limits set in the associated THERMTRIP Temp Limit Zone [3:1] register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

22.2.4 REGISTERS 28-2DH: FAN TACHOMETER READING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
28h	R	FANTACH1 LSB	7	6	5	4	3	2	1	0	FFh
29h	R	FANTACH1 MSB	15	14	13	12	11	10	9	8	FFh
2Ah	R	FANTACH2 LSB	7	6	5	4	3	2	1	0	FFh
2Bh	R	FANTACH2 MSB	15	14	13	12	11	10	9	8	FFh
2Ch	R	FANTACH3 LSB	7	6	5	4	3	2	1	0	FFh
2Dh	R	FANTACH3 MSB	15	14	13	12	11	10	9	8	FFh

This register is reset to its default value when PWRGD_PS is asserted.

The Fan Tachometer Reading registers contain the number of 11.111µs periods (90KHz) between full fan revolutions. Fans produce two tachometer pulses per full revolution. These registers are updated at least once every second.

This value is represented for each fan in a 16 bit, unsigned number.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, including when the start bit=0.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

These registers are read only – a write to these registers has no effect.

22.2.5 REGISTERS 30-32H: CURRENT PWM DUTY

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
30h	R/W (Note 22-12)	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
31h	R/W (Note 22-12)	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
32h	R/W (Note 22-12)	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A

Note 22-12 These registers are only writable when the associated fan is in manual mode. These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Current PWM Duty registers store the duty cycle that the chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start Register Start bit is set, this register and the PWM signals are updated based on the algorithm described in the Auto Fan Control Operating Mode section and the Ramp Rate Control logic, unless the associated fan is in manual mode – see below.

Note: When the device is configured for Manual Mode, the Ramp Rate Control logic should be disabled.

When read, the Current PWM Duty registers return the current PWM duty cycle for the respective PWM signal.

These registers are read only – a write to these registers has no effect.

Note: If the current PWM duty cycle registers are written while the part is not in manual mode or when the start bit is zero, the data will be stored in internal registers that will only be active and observable when the start bit is set and the fan is configured for manual mode. While the part is not in manual mode and the start bit is zero, the current PWM duty cycle registers will read back FFh.

This register contains the following bits:

Bit[0] Reserved

Bit[1] Monitoring Mode Select

0= Continuous Monitor Mode (default)

1= Cycle Monitor Mode

Bit[2] Interrupt (nHWM_INT Pin) Enable

0= Disables nHWM_INT pin output function (default)

1= Enables nHWM_INT pin output function

Bit[3] MCHP Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.Bit [4] MCHP Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated (TABLE 22). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

TABLE 22-15: AVG[2:0] BIT DECODER

SFTR[7:5]			Averages Per Reading		
AVG2	**AVG1**	**AVG0**	**REM Diode 1**	**REM Diode 2**	**Internal Diode**
0	0	0	128	128	8
0	0	1	16	16	1
0	1	X	16	16	16
1	X	X	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

22.2.26 REGISTER 7EH: INTERRUPT ENABLE 1 REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Eh	R/W	Interrupt Enable 1 (Voltages)	VCC	12V	5V	VTR	VCCP	2.5V	VBAT	VOLT	ECh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register is used to enable individual voltage error events to set the corresponding status bits in the interrupt status registers. This register also contains the group voltage enable bit (Bit[0] VOLT), which is used to enable voltage events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] Group interrupt Voltage Enable (VOLT)

0=Out-of-limit voltages do not affect the state of the nHWM_INT pin (default)

1=Enable out-of-limit voltages to make the nHWM_INT pin active low

Bit[1] VBAT Error Enable

Bit[2] 2.5V Error Enable

Bit[3] Vccp Error Enable

22.2.28 REGISTER 80H: INTERRUPT ENABLE 2 REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
80h	R/W	Interrupt Enable 2 (Fan Tachs)	RES	RES	RES	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	FAN-TACH	1Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual fan tach error events to set the corresponding status bits in the interrupt status registers. This register also contains the group fan tach enable bit (Bit[0] TACH), which is used to enable fan tach events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] FANTACH (Group TACH Enable)

0= Out-of-limit tachometer readings do not affect the state of the nHWM_INT pin (default)

1= Enable out-of-limit tachometer readings to make the nHWM_INT pin active low

Bit[1] Fantach 1 Event Enable

Bit[2] Fantach 2 Event Enable

Bit[3] Fantach 3 Event Enable

Bit[4] Reserved

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual fan tach error event bits are defined as follows:

0= disable

1= enable.

22.2.29 REGISTER 81H: TACH_PWM ASSOCIATION REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
81h	R/W	TACH_PWM Association	RES	RES	T3H	T3L	T2H	T2L	T1H	T1L	24h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to associate a PWM with a tachometer input. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers.

The fan tachometer will not cause a bit to be set in the interrupt status register:

a) if the current value in Current PWM Duty registers is 00h or
b) if the fan is disabled via the Fan Configuration Register.

Note: A bit will never be set in the interrupt status for a fan if its tachometer minimum is set to FFFFh.

See bit definition below.

Bits[1:0] Tach1. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[3:2] Tach2. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[5:4] Tach3. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[7:6] Reserved

TABLE 23-13: KYBD. LOGICAL DEVICE 7 [LOGICAL DEVICE NUMBER = 0X07]

Name	REG Index	Definition
KRST_GA20 Default = 0x00 on VCC POR, VTR POR and PCI RESET Bits[6:5] reset on VTR POR only	0xF0 R/W	KRESET and GateA20 Select Bit[7] Polarity Select for P12 = 0 P12 active low (default) = 1 P12 active high Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect MDAT signal to mouse wakeup (PME) logic. 1= block mouse clock and data signals into 8042 0= do not block mouse clock and data signals into 8042 Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect KDAT signal to keyboard wakeup (PME) logic. 1= block keyboard clock and data signals into 8042 0= do not block keyboard clock and data signals into 8042 Bit[4] MLATCH = 0 MINT is the 8042 MINT ANDed with Latched MINT (default) = 1 MINT is the latched 8042 MINT Bit[3] KLATCH = 0 KINT is the 8042 KINT ANDed with Latched KINT (default) = 1 KINT is the latched 8042 KINT Bit[2] Port 92 Select = 0 Port 92 Disabled = 1 Port 92 Enabled Bit[1] Reserved (read/write bit) Bit[0] Reserved (read/write bit)

TABLE 24-1: SCH322X RUNTIME REGISTER SUMMARY (CONTINUED)

Register Offset (HEX)	SCH3222 Register	SCH3224 Register	SCH3226, SCH3227 Register
1C	MSC_STS	MSC_STS	MSC_STS
1D	RESGEN	RESGEN	RESGEN
1E	Reserved	Reserved	Reserved
1F	Reserved	Reserved	Reserved
20	UART1 FIFO Control Shadow	UART1 FIFO Control Shadow	UART1 FIFO Control Shadow
21	UART2 FIFO Control Shadow	UART2 FIFO Control Shadow	UART2 FIFO Control Shadow
22	UART3 FIFO Control Shadow	Reserved - Indeterminate	UART3 FIFO Control Shadow
23	GP10	GP10 (Note 24-6)	GP10 (Note 24-6)
24	GP11	GP11 (Note 24-6)	GP11 (Note 24-6)
25	GP12	GP12 (Note 24-6)	GP12 (Note 24-6)
26	GP13	GP13 (Note 24-6)	GP13 (Note 24-6)
27	GP14	GP14 (Note 24-6)	GP14 (Note 24-6)
28	UART4 FIFO Control Shadow	Reserved - Indeterminate	UART4 FIFO Control Shadow
29	GP15	GP15 (Note 24-6)	GP15 (Note 24-6)
2A	GP16	GP16 (Note 24-6)	GP16 (Note 24-6)
2B	GP17	GP17 (Note 24-6)	GP17 (Note 24-6)
2C	GP21	GP21	GP21
2D	GP22	GP22	GP22
2E	UART5 FIFO Control Shadow	UART5 FIFO Control Shadow	If STRAPOPT=1: UART5 FIFO Control Shadow If STRAPOPT=0: Reserved
2F	UART6 FIFO Control Shadow	UART6 FIFO Control Shadow	If STRAPOPT=1: UART6 FIFO Control Shadow If STRAPOPT=0: Reserved
30	SP5 Option	SP5 Option	If STRAPOPT=1: SP5 Option If STRAPOPT=0: Reserved
31	SP6 Option	SP6 Option	If STRAPOPT=1: SP6 Option If STRAPOPT=0: Reserved
32	GP27	GP27	GP27
33	GP30	GP30	GP30
34	GP31	GP31(Note 24-6)	GP31(Note 24-6)
35	GP32	GP32	GP32
36	GP33	GP33	GP33
37	GP34	GP34 (Note 24-6)	GP34 (Note 24-6)
38	Reserved	Reserved	Reserved
39	GP36	GP36	GP36
3A	GP37	GP37	GP37
3B	GP40	GP40	GP40
3C	CLK_OUT Register	CLK_OUT Register	CLK_OUT Register
3D	GP42	GP42	GP42
3E	Reserved – reads return 0	Reserved – reads return 0	Reserved – reads return 0
3F	GP50	GP50	GP50

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP61 Default = 0x01 on VTR POR	48 (R/W)	General Purpose I/O bit 6.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=CLKO - Programmable clock output as described in 10=Either Edge Triggered Interrupt Input 5 (Note 24-20) 01=LED2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
PWR_REC Power Recovery Register Default = 0xxxxx11b on VTR POR Default =x00000xxb on a Vbat POR Default = 0xxxxxxxb on a VCC POR and PCI Reset Note: x indicates that the bit is not affected by this reset condition. (SCH3227 or SCH3226, and STRAPOPT=0)	49 R/W when bit[7] =0 (default), except for bit[4] Bit[4] is a Read-Only bit. Read-Only when bit[7]=1	A/C Power Control/Recovery Register Bit[0] Power Button Enable 0=disabled 1=enabled (default) Bit[1] Keyboard Power Button Enable 0=disabled 1=enabled (default) Bit[2] Power Failure Recovery Enable 0=disabled (default) 1=enabled Bit[3] PS_ON# sampling enable 0=Sampling is disabled (Mode 1) 1=Sampling is enabled (Mode 2) When sampling is enabled the PS_ON# pin is sampled every 0.5 seconds and stored in an 8-bit shift register for up to a maximum of 4 seconds. Bit[4] Previous State Bit (This read-only bit is powered by Vbat) (NOTE: THIS BIT IS NOT RESET ON A VTR POR) This bit contains the state of the PS_ON# pin when VTR power is removed from the device. 0=off (PS_ON# signal was high) 1=on (PS_ON# signal was low) Bit[6:5] APF (After Power Failure) (These bits are powered by Vbat) (NOTE: THIS BIT IS NOT RESET ON A VTR POR) When VTR transitions from the OFF state to the ON state, the power recovery logic will look at the APF bits to determine if the power supply should be off or on. If the logic determines that the Power Supply should be place in the ON state it will generate a pulse on the PB_OUT# pin. The auto recovery logic does not directly control the PS_ON# pin. The PS_ON# pin is controlled by the SLP_Sx# pin. 00=Power Supply Off 01=Power Supply On 10=Power Supply set to Previous State 11=Power Supply Off Bit[7] Register Recovery R/W Control This bit is used to control write access to the Power Recovery Register at offset 49h. 0=Read/Write 1=Read-OnlyA/C Power Control/Recovery Register

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP2 Default = 0x00 on VTR POR	4C (R/W)	General Purpose I/O Data Register 2 Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] GP27
GP3 Default = 0x00 on VTR POR	4D (R/W)	General Purpose I\O Data Register 3 Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] Reserved Bit[6] GP36 Bit[7] GP37
GP4 Default = 0xF0 on VTR POR	4E (R/W)	General Purpose I/O Data Register 4 Bit[0] GP40 Bit[1] Reserved Bit[2] GP42 Bit[3] Reserved Bit[4] GP44 Bit[5] GP45 Bit[6] GP46 Bit[7] GP47
GP5 Default = 0x00 on VTR POR	4F (R/W)	General Purpose I/O Data Register 5 Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57
GP6 Default = 0x00 on VTR POR	50 (R/W)	General Purpose I/O Data Register 6 Bit[0] GP60 Bit[1] GP61 Bit[2] GP62 Bit[3] GP63 Bit[4] GP64 Bit[5] GP65 Bit[6] GP66 Bit[7] GP67
N/A	51 (R)	Bits[7:0] Reserved – reads return 0

FIGURE 27-7: I/O WRITE

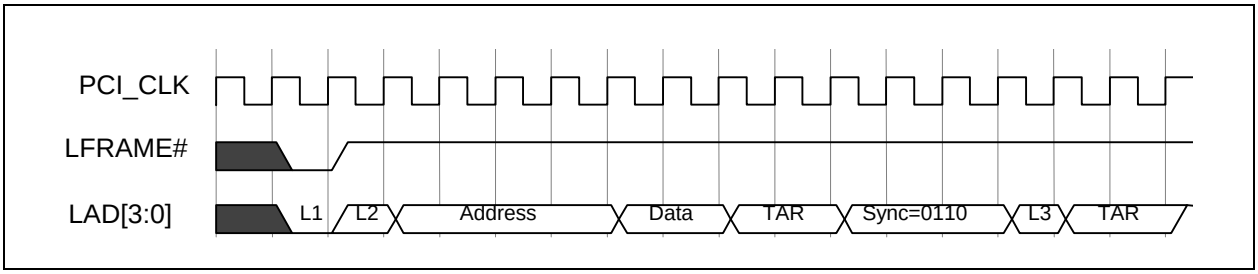
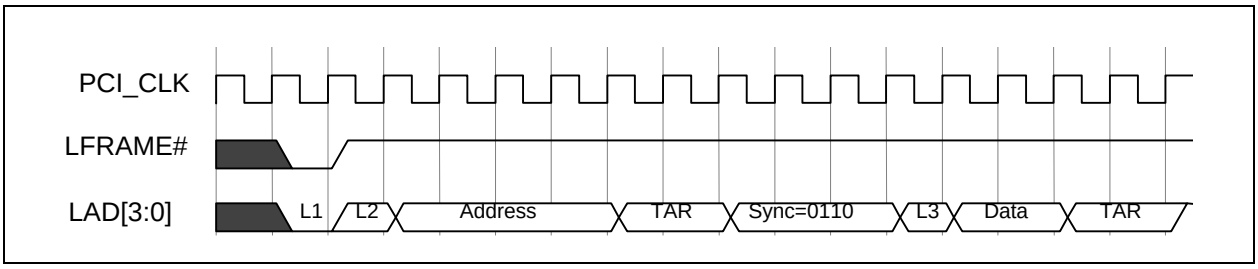


FIGURE 27-8: I/O READ



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 27-9: DMA REQUEST ASSERTION THROUGH LDRQ#

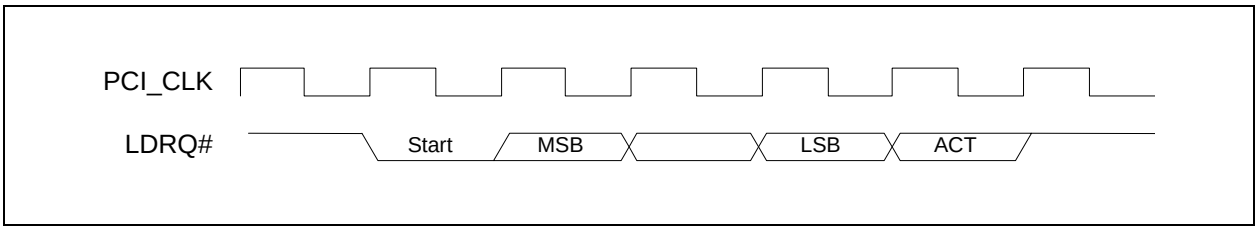
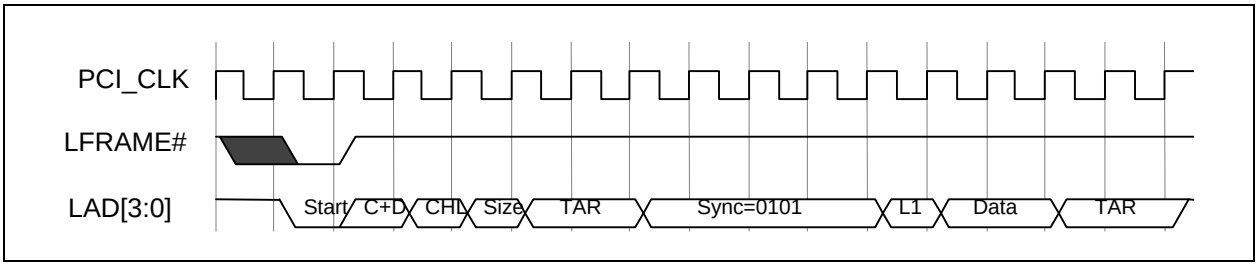
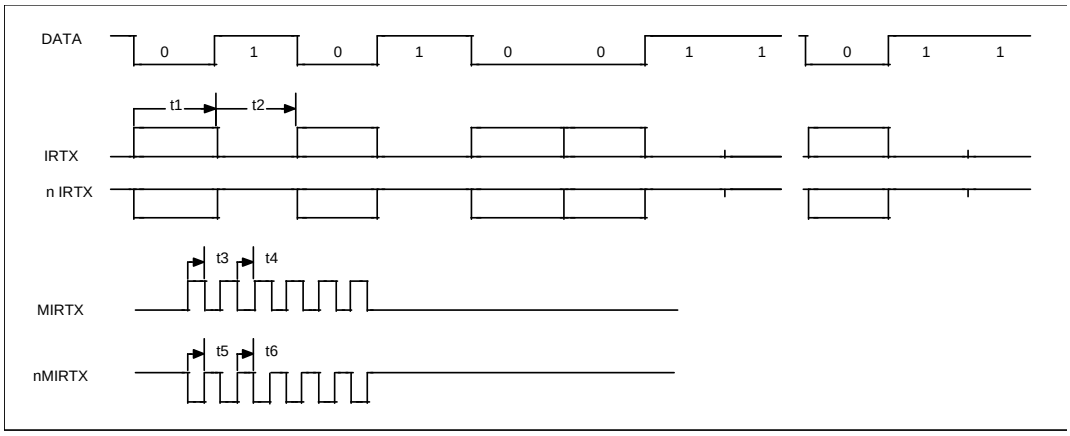


FIGURE 27-10: DMA WRITE (FIRST BYTE)



Note: L1=Sync of 0000

FIGURE 27-22: AMPLITUDE SHIFT-KEYED IR TRANSMIT TIMING



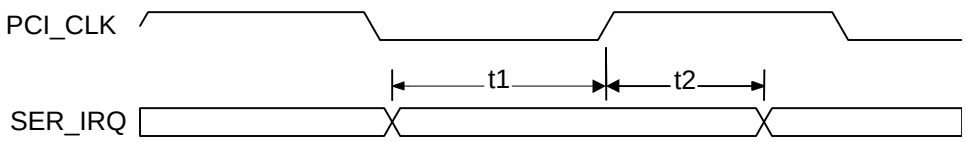
	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µ s
t2	Off Bit Time				µ s
t3	Modulated Output "On"	0.8	1	1.2	µ s
t4	Modulated Output "Off"	0.8	1	1.2	µ s
t5	Modulated Output "On"	0.8	1	1.2	µ s
t6	Modulated Output "Off"	0.8	1	1.2	µ s

Notes:

1. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0
   MIRTX, nMIRTX are the modulated outputs

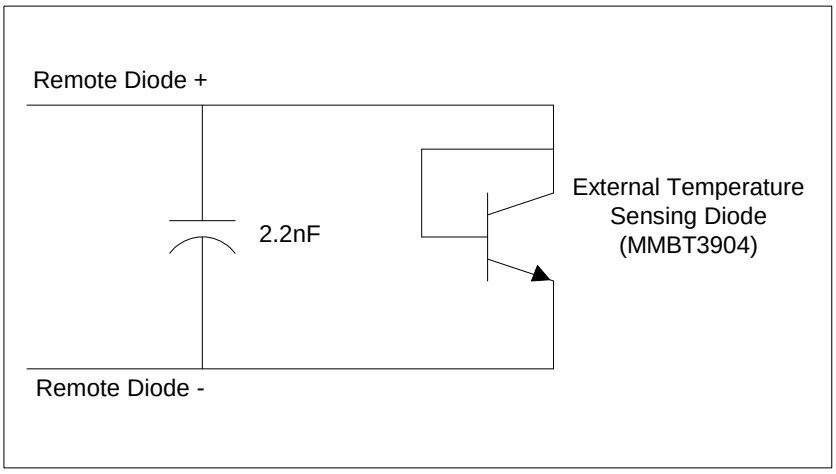
27.6 Serial IRQ Timing

FIGURE 27-23: SETUP AND HOLD TIME



Name	Description	MIN	TYP	MAX	Units
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

FIGURE B-4: REMOTE DIODE (APPLY TO REMOTE2 LINES)



Note 1: 2.2nF cap is optional and should be placed close to the SCH322x f used.

2: The voltage at PWM3 must be at least 2.0V to avoid triggering Address Enable.

3: The Remote Diode + and Remote Diode - tracks should be kept close together, in parallel with grounded guard tracks on each side. Using wide tracks will help to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended. See Figure B-5, "Suggested Minimum Track Width and Spacing".

FIGURE B-5: SUGGESTED MINIMUM TRACK WIDTH AND SPACING