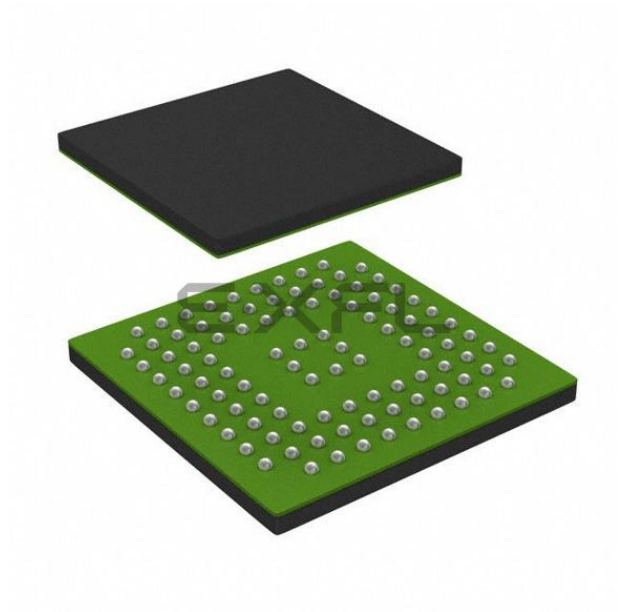

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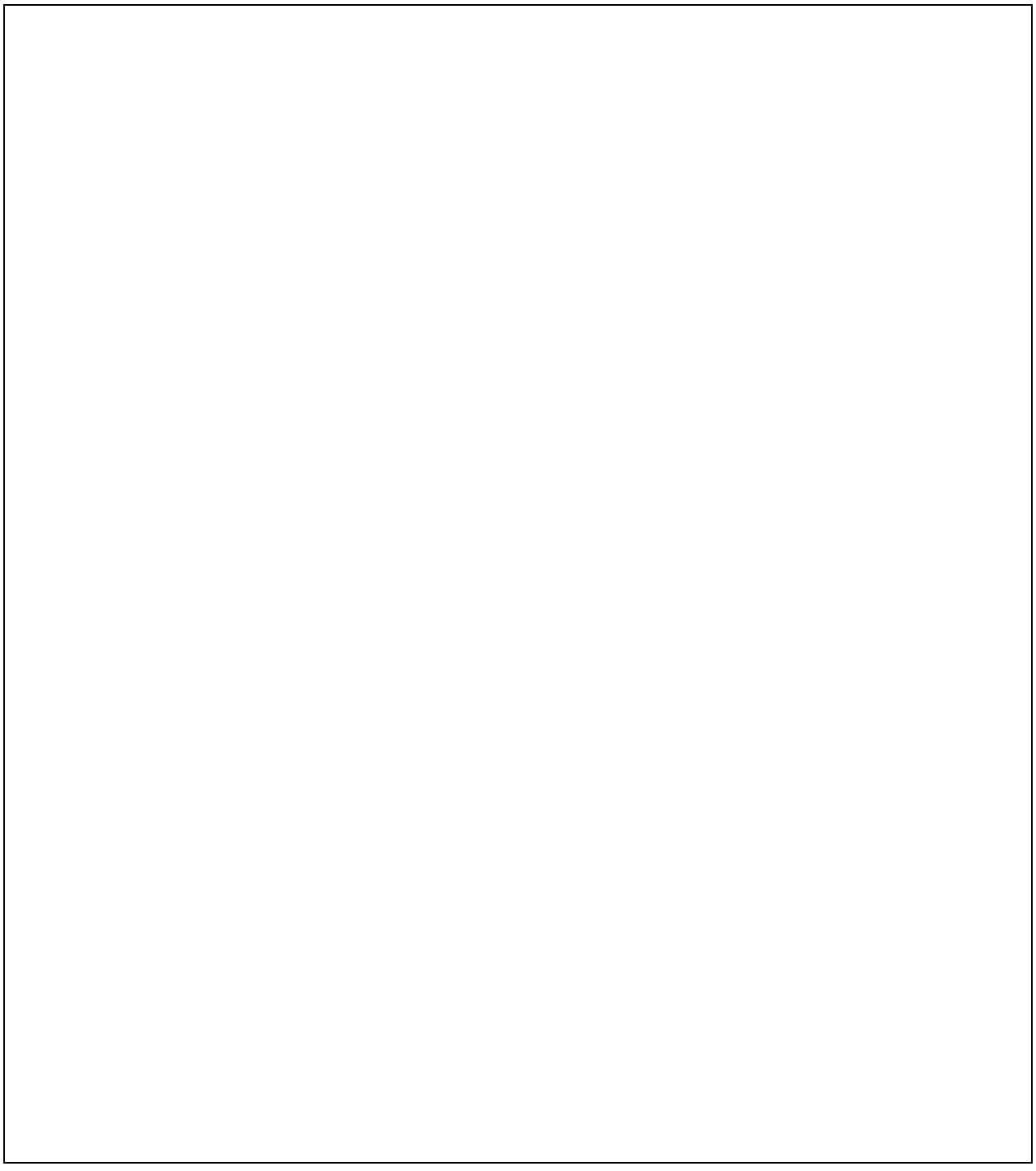
Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-WFBGA
Supplier Device Package	100-WFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3226i-sy

Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
K13	STRAPOPT (=VTR[a])	STRAPOPT (=VSS[a])
M4	RESERVED=VTR[b]	RESERVED=VTR[b]
C3	+12V_IN	+12V_IN
D3	+5V_IN	+5V_IN
E6	GP40	GP40
E3	VTR	VTR
E5	RESERVED=VSS[c]	RESERVED=VSS[c]
F8	TEST=VSS[c]	TEST=VSS[c]
F7	RESERVED=VSS[c]	RESERVED=VSS[c]
F3	VSS	VSS
F6	RESERVED=VSS[c]	RESERVED=VSS[c]
F5	RESERVED=VSS[c]	RESERVED=VSS[c]
G8	RESERVED=VSS[c]	RESERVED=VSS[c]
G6	RESERVED=VSS[c]	RESERVED=VSS[c]
H8	RESERVED=VSS[c]	RESERVED=VSS[c]
G5	RESERVED=VSS[c]	RESERVED=VSS[c]
H7	RESERVED=VSS[c]	RESERVED=VSS[c]
H6	RESERVED=VSS[c]	RESERVED=VSS[c]
H5	RESERVED=VSS[c]	RESERVED=VSS[c]
D2	CLOCKI	CLOCKI
E2	LAD0	LAD0
D1	LAD1	LAD1
E1	LAD2	LAD2
F2	LAD3	LAD3
F1	LFRAME#	LFRAME#
G2	LDRQ#	LDRQ#
H1	PCI_RESET#	PCI_RESET#
G1	PCI_CLK	PCI_CLK
H2	SER_IRQ	SER_IRQ
H3	VSS	VSS
J3	VCC	VCC
J1	GP44 / TXD6	nIDE_RSTDRV / GP44
J2	GP45 / RXD6	nPCIRST1 / GP45
K3	GP46 / nSCIN6	nPCIRST2 / GP46
L3	GP47 / nSCOUT6	nPCIRST3 / GP47
K1	AVSS	AVSS
L1	VBAT	VBAT
K2	GP27 / nIO_SMI / P17	GP27 / nIO_SMI / P17
L2	KDAT / GP21	KDAT / GP21
M1	KCLK / GP22	KCLK / GP22
M2	MDAT / GP32	MDAT / GP32
N1	MCLK / GP33	MCLK / GP33
M3	GP36 / nKBDRST	GP36 / nKBDRST

FIGURE 2-4: SCH3222 PIN DIAGRAM



5.0 LPC INTERFACE

5.1 LPC Interface Signal Definition

The signals implemented for the LPC bus interface are described in the tables below. LPC bus signals use PCI 33MHz electrical signal characteristics.

5.1.1 LPC REQUIRED SIGNALS

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset. Same functionality as RST_DRV but active low 3.3V.
PCI_CLK	Input	PCI Clock.

5.1.2 LPC OPTIONAL SIGNALS

Signal Name	Type	Description	Comment
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.	Implemented
SER_IRQ	I/O	Serial IRQ.	Implemented
CLKRUN#	OD	Clock Run	Not Implemented
nIO_PME	OD	Same as the PME# or Power Mgt Event signal. Allows the SCH3227/SCH3226/SCH3224/SCH3222 to request wakeup in S3 and below.	Implemented
LPCPD#	I	Power down - Indicates that the device should prepare for LPC I/F shutdown	Not Implemented
LSMI#	OD	Only need for SMI# generation on I/O instruction for retry.	Not Implemented

5.2 Supported LPC Cycles

Table 5-1 summarizes the cycle types are supported by the SCH3227/SCH3226/SCH3224/SCH3222. All other cycle types are ignored.

TABLE 5-1: SUPPORTED LPC CYCLES

Cycle Type	Transfer Size	Comment
I/O Write	1 Byte	Supported
I/O Read	1 Byte	Supported
Memory Write	1 Byte	Not Supported
Memory Read	1 Byte	Not Supported
DMA Write	1 Byte	Supported
DMA Write	2 Byte	Supported
DMA Write	4 Byte	Not Supported
DMA Read	1 Byte	Supported
DMA Read	2 Byte	Supported
DMA Read	4 Byte	Not Supported
Bus Master Memory Write	1 Byte	Not Supported
Bus Master Memory Write	2 Byte	Not Supported
Bus Master Memory Write	4 Byte	Not Supported
Bus Master Memory Read	1 Byte	Not Supported
Bus Master Memory Read	2 Byte	Not Supported
Bus Master Memory Read	4 Byte	Not Supported
Bus Master I/O Write	1 Byte	Not Supported

7.1.7 EPP DATA PORT 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.1.8 EPP DATA PORT 3

ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

7.1.9 EPP 1.9 OPERATION

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

7.1.10 SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

7.1.11 EPP 1.9 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

- If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
- If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host initiates an I/O write cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
6.
   a) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b) The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.
7. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
8. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

7.2 Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel Interlocked handshake, for fast reliable transfer Optional single byte RLE compression for improved throughput (64:1) Channel addressing for low-cost peripherals Maintains link and data layer separation Permits the use of active output drivers permits the use of adaptive signal timing Peer-to-peer capability.

7.2.1 VOCABULARY

The following terms are used in this document:

assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.

forward: Host to Peripheral communication.

reverse: Peripheral to Host communication

Pword: A port word; equal in size to the width of the LPC interface. For this implementation, PWord is always 8 bits.

1 A high level.

0 A low level.

These terms may be considered synonymous:

PeriphClk, nAck

HostAck, nAutoFd

PeriphAck, Busy

nPeriphRequest, nFault

nReverseRequest, nInit

nAckReverse, PError

Xflag, Select

ECPMode, nSelectln

HostClk, nStrobe

Reference Document: *IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard*, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	D6	D5	D4	D3	D2	D1	D0	Note
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			
ecr	MODE			nErrIntrEn	dmaEn	serviceI ntr	full	empty	

Note 1: These registers are available in all modes.

2: All FIFOs use one common 16 byte FIFO.

3: The ECP Parallel Port Config Reg B reflects the IRQ and DMA channel selected by the Configuration Registers.

In the SCH3227/SCH3226/SCH3224/SCH3222 the nIO_PME pin can be programmed to be an open drain, active low, driver. The SCH3227/SCH3226/SCH3224/SCH3222 nIO_PME pin are fully isolated from other external devices that might pull the signal low; i.e., the nIO_PME pin are capable of being driven high externally by another active device or pull-up even when the SCH3227/SCH3226/SCH3224/SCH3222 VCC is grounded, providing VTR power is active. The IO_PME pin driver sinks 6mA at 0.55V max (see section 4.2.1.1 DC Specifications in the "PCI Local Bus Specification, Revision 2.2, December 18, 1998).

13.4 Wake on Specific Key Code

The SCH3227/SCH3226/SCH3224/SCH3222 Wake on Specific Key Code feature is enabled for the assertion of the nIO_PME signal in SX power states by the SPEKEY bit in the PME_STS6 register. This bit defaults to enabled and is Vbat powered.

At Vbat POR the Wake on Specific Key Code feature is disabled. During the first VTR POR and VCC POR the Wake on Specific Key Code feature remains disabled. Software selects the precise Specific Key Code event (configuration) to wake the system and then enables the feature via the SPEKEY bit in the PME_STS6 register. The system then may go the sleep and/or have a power failure. After returning to or remaining in S5 sleep, the system will fully awake by a Wake on Specific Key Code The Specific Key Code configuration and the enable for the nIO_PME are retained via Vbat POR backed registers.

The SCH3227/SCH3226/SCH3224/SCH3222 Wake on Specific Key Code feature is enabled for assertion of the nIO_PME signal when in S3 power state or below by the SPEKEY bit in the PME_EN6 register. This bit defaults to disabled and is VTR powered.

13.5 Wake on Specific Mouse Click

The SPESME SELECT field in the Mouse_Specific_ Wake Register selects which mouse event is routed to the PME_STS6 if enabled by PME_EN6. The KB_MSE_SWAP bit in the Mouse_Specific_ Wake Register can swap the Mouse port and Keyboard interfaces internally.

The Lock bit in the Mouse_Specific_ Wake Register provides a means of changing access to read only to prevent tampering with the Wake on Mouse settings. The other bits in the Mouse_Specific_ Wake Register are VBAT powered and reset on VBAT POR; therefore, the mouse event settings are maintained through a power failure. The lock bit also controls access to the DBLCLICK Register.

The DBLCLICK register contains a numeric value that determines the time interval used to check for a double mouse click. The value is the time interval between mouse clicks. For example, if DBLCLICK is set to 0.5 seconds, you have one half second to click twice for a double-click.

The larger the value in the DBLCLICK Register, the longer you can wait between the first and second click for the SCH3227/SCH3226/SCH3224/SCH3222 to interpret the two clicks as a double-click mouse wake event. If the DBLCLICK value is set to a very small value, even quick double clicks may be interpreted as two single clicks.

The DBLCLICK register has a six bit weighted sum value from 0 to 0x3Fh which provides a double click interval between 0.0859375 and 5.5 seconds. Each incremental digit has a weight of 0.0859375 seconds.

The DBLCLICK Register is VBAT powered and reset on VBAT POR; therefore, the double click setting is maintained through a power failure. The default setting provides a 1.03125 second time interval.

DBLCLICK Writing to the DBLCLICK register shall reset the Mouse Wake-up internal logic and initialize the Mouse Wake-up state machines.The SPEMSE_EN bit in of the CLOCKI32 configuration register at 0xF0 in Logical Device A is used to control the “Wake on Specific Mouse Click” feature. This bit is used to turn the logic for this feature on and off. It will disable the 32KHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:

0= "Wake on Specific Mouse Click" logic is on (default)

1= "Wake on Specific Mouse Click" logic is off

The generation of a PME for this event is controlled by the PME enable bits (SPEMSE_EN bit in the PME_EN6 register and in the SMI_EN2 register) when the logic for feature is turned on. See Section 13.5, "Wake on Specific Mouse Click," on page 96.

APPLICATION NOTE: The Wake on Specific Mouse Click feature requires use of the M_ISO bit in the KRST_GA20 register. See Application Note 8.8 titled “Keyboard and Mouse Wake-up Functionality”.

18.0 POWER CONTROL FEATURES

The SCH322x family devices are able to turn on the power supply when the power button located on the PC chassis is pressed, when the power button located on the keyboard is pressed, or when recovering from a power failure. The signals used to support these features are:

- PB_IN#
- PB_OUT#
- SLP_Sx#
- PS_ON#

Table 18-1 and Figure 18-1 describe the interface and connectivity of the following Power Control Features:

1. Front Panel Reset with Input Debounce, Power Supply Gate, and Powergood Output Signal Generation
2. AC Recovery Circuit
3. Keyboard Wake on Mouse.
4. SLP_Sx# PME wakeup

TABLE 18-1: POWER CONTROL INTERFACE

Name	Direction	Description
PB_IN#	Input	Power Button Input
PB_OUT#	Output	Power Good Output
PS_ON#	Output	Power Supply On output
SLP_SX#	Input	From south bridge
PWRGD_PS	Input	Power Good Input from Power Supply
nFPRST	Input	Reset Input from Front Panel
PWRGD_OUT	Output	Power Good Output – Open Drain
nIO_PME	Output	Power Management Event Output signal allows this device to request wakeup.

clear the status bit. Setting or clearing the START bit when the individual enable bit is one has no effect on the status bits.

Note 1: The individual enable bits for D2, AMB, and D1 are located in the Interrupt Enable 3 (Temp) register at offset 82h.

2: Clearing the group Temp enable bit or the global INTEN enable bit has no effect on the status bits.

Bit	Name	R/W	Default	Description
0	2.5V_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the Vccp input voltage is less than or equal to the limit set in the Vccp Low Limit register or greater than the limit set in the Vccp High Limit register.
2	VCC_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the VCC input voltage is less than or equal to the limit set in the VCC Low Limit register or greater than the limit set in the VCC High Limit register.
3	5V_Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Remote Diode 1 Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ is less than or equal to the limit set in the Remote Diode 1 Low Temp register or greater than the limit set in Remote Diode 1 High Temp register.
5	Internal Sensor Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal Low Temp register or greater than the limit set in the Internal High Temp register.
6	Remote Diode 2 Limit Error	R/WC	0	The SCH322x automatically sets this bit to 1 when the temperature input measured by the Remote2- and Remote2+ is less than or equal to the limit set in the Remote Diode 2 Low Temp register or greater than the limit set in the Remote Diode 1 High Temp register.
7	INT2 Event Active	R/WC	0	The device automatically sets this bit to 1 when a status bit is set in the Interrupt Status Register 2.

22.2.11 REGISTER 42H: INTERRUPT STATUS REGISTER 2

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
42h	R/WC	Interrupt Status Register 2	ERR2	ERR1	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	RES	12V	00h

Note 1: This register is reset to its default value when the PWRGD_PS signal transitions high.

2: This is a read/write-to-clear register. The status bits are cleared on a write of one if the event causing the interrupt is no longer active. Writing a zero to these bits has no effect.

The Interrupt Status Register 2 bits is automatically set by the device whenever a tach reading value is above the minimum value set in the tachometer minimum registers or when a remote diode fault occurs. When a remote diode fault occurs (if the start bit is set) 80h will be loaded into the associated temperature reading register, which causes the associated diode limit error bit to be set (see Register 41h: Interrupt Status Register 1 on page 167) in addition to the diode fault bit (ERRx). These individual status bits remain set until the bit is written to one by software or until the individual enable bit is cleared, even if the event no longer persists.

- Clearing the status bits by a write of ‘1’
  - The FANTACHx status bits are cleared (set to 0) automatically by the SCH322x after they are written to one by software, if the FANTACHx reading register no longer violates the programmed FANTACH Limit. (See Registers 28-2Dh: Fan Tachometer Reading on page 164 and Registers 54-59h: Fan Tachometer Low Limit on page 171)

This register holds a set bit until the event is cleared by software or until the individual enable bit is cleared. Once set, the Interrupt Status Register 3 bits remain set until the individual enable bits is cleared, even if the voltage or tachometer reading no longer violate the limits set in the limit registers. Note that clearing the group Temp, Fan, or Volt enable bits or the global INTEN enable bit has no effect on the status bits.

Note: The individual enable bits for VTR and Vbat are located in the Interrupt Enable 1 register at offset 7Eh.

This register is read only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	VTR_Error	R	0	The device automatically sets this bit to 1 when the VTR input voltage is less than or equal to the limit set in the VTR Low Limit register or greater than the limit set in the VTR High Limit register.
1	Vbat_Error	R	0	The device automatically sets this bit to 1 when the Vbat input voltage is less than or equal to the limit set in the Vbat Low Limit register or greater than the limit set in the Vbat High Limit register.
2-7	Reserved	R	0	Reserved

22.2.32 REGISTERS 84H-88H: A/D CONVERTER LSBS REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
84h	R	A/D Converter LSbs Reg 5	VTR.3	VTR.2	VTR.1	VTR.0	VBT.3	VBT.2	VBT.1	VBT.0	N/A
85h	R	A/D Converter LSbs Reg 1	RD2.3	RD2.2	RD2.1	RD2.0	RD1.3	RD1.2	RD1.1	RD1.0	N/A
86h	R	A/D Converter LSbs Reg 2	V12.3	V12.2	V12.1	V12.0	AM.3	AM.2	AM.1	AM.0	N/A
87h	R	A/D Converter LSbs Reg 3	V50.3	V50.2	V50.1	V50.0	V25.3	V25.2	V25.1	V25.0	N/A
88h	R	A/D Converter LSbs Reg 4	VCC.3	VCC.2	VCC.1	VCC.0	VCP.3	VCP.2	VCP.1	VCP.0	N/A

There is a 10-bit Analog to Digital Converter (ADC) located in the hardware monitoring block that converts the measured voltages into 10-bit reading values. Depending on the averaging scheme enabled (i.e., 16x averaging, 32x averaging, etc.), the hardware monitor may take multiple readings and average them to create 12-bit reading values. The 8 MSb's of the reading values are placed in the Reading Registers. When the upper 8-bits located in the reading registers are read the 4 LSb's are latched into their respective bits in the A/D Converter LSbs Register. This give 12-bits of resolution with a minimum value of $1/16^{th}$ per unit measured. (i.e., Temperature Range: -127.9375 ºC < Temp < 127.9375 ºC and Voltage Range: 0 < Voltage < 256.9375). See the DC Characteristics for the accuracy of the reading values.

The eight most significant bits of the 12-bit averaged readings are stored in Reading registers and compared with Limit registers. The Interrupt Status Register bits are asserted if the corresponding measured value(s) on the inputs violate their programmed limits.

22.2.33 REGISTERS 89H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
89h	R	MCHP Test Register	7	6	5	4	3	2	1	0	N/A

This is a read-only MCHP test register. Writing to this register has no effect on the hardware.

22.2.34 REGISTERS 8AH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

22.2.35 REGISTERS 8BH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Bh	R/W	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

TABLE 24-1: SCH322X RUNTIME REGISTER SUMMARY (CONTINUED)

Register Offset (HEX)	SCH3222 Register	SCH3224 Register	SCH3226, SCH3227 Register
1C	MSC_STS	MSC_STS	MSC_STS
1D	RESGEN	RESGEN	RESGEN
1E	Reserved	Reserved	Reserved
1F	Reserved	Reserved	Reserved
20	UART1 FIFO Control Shadow	UART1 FIFO Control Shadow	UART1 FIFO Control Shadow
21	UART2 FIFO Control Shadow	UART2 FIFO Control Shadow	UART2 FIFO Control Shadow
22	UART3 FIFO Control Shadow	Reserved - Indeterminate	UART3 FIFO Control Shadow
23	GP10	GP10 (Note 24-6)	GP10 (Note 24-6)
24	GP11	GP11 (Note 24-6)	GP11 (Note 24-6)
25	GP12	GP12 (Note 24-6)	GP12 (Note 24-6)
26	GP13	GP13 (Note 24-6)	GP13 (Note 24-6)
27	GP14	GP14 (Note 24-6)	GP14 (Note 24-6)
28	UART4 FIFO Control Shadow	Reserved - Indeterminate	UART4 FIFO Control Shadow
29	GP15	GP15 (Note 24-6)	GP15 (Note 24-6)
2A	GP16	GP16 (Note 24-6)	GP16 (Note 24-6)
2B	GP17	GP17 (Note 24-6)	GP17 (Note 24-6)
2C	GP21	GP21	GP21
2D	GP22	GP22	GP22
2E	UART5 FIFO Control Shadow	UART5 FIFO Control Shadow	If STRAPOPT=1: UART5 FIFO Control Shadow If STRAPOPT=0: Reserved
2F	UART6 FIFO Control Shadow	UART6 FIFO Control Shadow	If STRAPOPT=1: UART6 FIFO Control Shadow If STRAPOPT=0: Reserved
30	SP5 Option	SP5 Option	If STRAPOPT=1: SP5 Option If STRAPOPT=0: Reserved
31	SP6 Option	SP6 Option	If STRAPOPT=1: SP6 Option If STRAPOPT=0: Reserved
32	GP27	GP27	GP27
33	GP30	GP30	GP30
34	GP31	GP31(Note 24-6)	GP31(Note 24-6)
35	GP32	GP32	GP32
36	GP33	GP33	GP33
37	GP34	GP34 (Note 24-6)	GP34 (Note 24-6)
38	Reserved	Reserved	Reserved
39	GP36	GP36	GP36
3A	GP37	GP37	GP37
3B	GP40	GP40	GP40
3C	CLK_OUT Register	CLK_OUT Register	CLK_OUT Register
3D	GP42	GP42	GP42
3E	Reserved – reads return 0	Reserved – reads return 0	Reserved – reads return 0
3F	GP50	GP50	GP50

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
SMI_EN3 Default = 0x00 on VTR POR	1A (R/W)	SMI Enable Register 3 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] GP54 Bit[4] GP55 Bit[5] GP56 Bit[6] GP57 Bit[7] GP60
SMI_EN4 Default = 0x00 on VTR POR (SCH3224)	1B (R/W)	SMI Enable Register 4 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] RESERVED Bit[1] RESERVED Bit[2] GP32 Bit[3] GP33 Bit[4] U5INT Bit[5] GP42 Bit[6] U5INT Bit[7] GP61
SMI_EN4 Default = 0x00 on VTR POR (All except SCH3224)	1B (R/W)	SMI Enable Register 4 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] U3INT Bit[1] U4INT Bit[2] GP32 Bit[3] GP33 Bit[4] U5INT (RESERVED if SCH3227/SCH3226 and STRAPOPT=0) Bit[5] GP42 Bit[6] U6INT (RESERVED if SCH3227/SCH3226 and STRAPOPT=0) Bit[7] GP61
MSC_STS Default = 0x00 on VTR POR	1C (R/W)	Miscellaneous Status Register Bits[5:0] can be cleared by writing a 1 to their position (writing a 0 has no effect). Bit[0] Either Edge Triggered Interrupt Input 0 Status. This bit is set when an edge occurs on the GP21 pin. Bit[1] Either Edge Triggered Interrupt Input 1 Status. This bit is set when an edge occurs on the GP22 pin. Bit[2] Reserved Bit[3] Reserved Bit[4] Either Edge Triggered Interrupt Input 4 Status. This bit is set when an edge occurs on the GP60 pin. Bit[5] Either Edge Triggered Interrupt Input 5 Status. This bit is set when an edge occurs on the GP61 pin. Bit[7:6] Reserved. This bit always returns zero.
RESGEN VTR POR default = 00h	1Dh (R/W)	Reset Generator Bit[0] WDT2_EN: Enable Watchdog timer Generation / Select 0= WDT Enabled - Source for PWRGD_OUT (Default) 1= WDT Disabled - Not source for PWRGD_OUT Bit[1] ThermTrip Source Select 0 = Thermtrip not source for PWRGD_OUT ((Default) 1 = Thermtrip source for PWRGD_OUT Bit[2] WDT2_CTL: WDT input bit Bit[7:3] Reserved

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
GP21 Default =0x8C on VTR POR	2C (R/W)	General Purpose I/O bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KDAT (Default) 10=Either Edge Triggered Interrupt Input 0 (Note 24-20) 01=Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull (Default) **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KDAT function, bit[0] should always be programmed to '0'. The KDAT function will not operate properly when bit[0] is set.
GP22 Default =0x8C on VTR POR	2D (R/W)	General Purpose I/O bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KCLK (Default) 10=Either Edge Triggered Interrupt Input 1 (Note 24-20) 01= Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull **APPLICATION NOTE:** When Bits[3:2] are programmed to '11' to select the KCLK function, bit[0] should always be programmed to '0'. The KCLK function will not operate properly when bit[0] is set.
UART5 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2E (R)	Bits[7:0] RESERVED
UART5 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2E (R)	UART FIFO Control Shadow 5 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
UART6 FIFO Control Shadow (SCH3227 or SCH3226, and STRAPOPT=0)	2F (R)	Bits[7:0] RESERVED
UART6 FIFO Control Shadow (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	2F (R)	Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PWR_REC Power Recovery Register Default = 0xxxxx11b on VTR POR Default =x00000xxb on a Vbat POR Default = 0xxxxxxxb on a VCC POR and PCI Reset Note: x indicates that the bit is not affected by this reset condition. (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	49	Bits[7:0] RESERVED Do not write to this register.
PS_ON Register default = 0x00 on a Vbat POR default = value latched on Power Failure on a VTR POR (SCH3227 or SCH3226, and STRAPOPT=0)	4A (R)	PS_ON Shift Register This 8-bit register is used to read the PS_ON sample values loaded in the shift register in A/C Power Recovery Control - Mode 2. Bit[0] = PS_ON# sampled 0 - 0.5sec before power failure Bit[1] = PS_ON# sampled 0.5 - 1.0sec before power failure Bit[2] = PS_ON# sampled 1.0 - 1.5sec before power failure Bit[3] = PS_ON# sampled 1.5 - 2.0sec before power failure Bit[4] = PS_ON# sampled 2.0 - 2.5sec before power failure Bit[5] = PS_ON# sampled 2.5 - 3.0sec before power failure Bit[6] = PS_ON# sampled 3.0 - 3.5sec before power failure Bit[7] = PS_ON# sampled 3.5 - 4.0sec before power failure Bit definition 0=off (PS_ON# signal was high) 1=on (PS_ON# signal was low) **Note:** This register is powered by Vbat
PS_ON Register default = 0x00 on a Vbat POR default = value latched on Power Failure on a VTR POR (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	4A (R)	Bits[7:0] RESERVED **Note:** This register is powered by Vbat
GP1 Default = 0x00 on VTR POR	4B (R/W)	General Purpose I/O Data Register 1 Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17

HARDWARE MONITORING BLOCK (T_A = 0°C – +70°C, HVTR = +3.3 V ± 10%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Comments**
H_{VTR} Supply Current Active Mode	I_{HTR}			2	µA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V.

HARDWARE MONITORING BLOCK (T_A = -40°C – +85°C, HVTR = +3.3 V ± 10%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Temperature-to-Digital Converter Characteristics						
Internal Temperature Accuracy		-3	±0.25	+3	°C	0°C <= T_A <= 85°C
		-2		+3	°C	40°C <= T_A <= 85°C
External Diode Sensor Accuracy					°C	Resolution
		-5	±0.25	+5	°C	-40°C <= T_S <= 125°C
		-3		+3	°C	40°C <= T_S <= 100°C
					°C	Resolution
Analog-to-Digital Converter Characteristics						
Total Unadjusted Error	TUE			±2	%	Note 26-5
Differential Non-Linearity	DNL		±1		LSB	
Power Supply Sensitivity	PSS		±2		%/V	
Total Monitoring Cycle Time (Cycle Mode, Default Averaging)	$t_{C(Cycle)}$		1.25	1.4	sec	Note 26-6
Conversion Time (Continuous Mode, Default Averaging)	$t_{C(Cts)}$	225	247	275	msec	Note 26-7
Input Resistance			140	200	kΩ	
ADC Resolution						10 bits Note 26-10
Input Buffer (I) (FANTACH1)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
Input Buffer (I) (FANTACH2-FANTACH3)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		5.5	V	
I_VID Type Buffer (GP62* to GP67*)						(Note 26-11)
Low Input Level	V_{ILI}			0.4	V	
High Input Level	V_{IHI}	0.8		5.5	V	

HARDWARE MONITORING BLOCK (T_A = -40°C – +85°C, HVTR = +3.3 V ± 10%)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Comments**
IOD Type Buffer (PWM1, PWM2, PWM3/ADDRESS ENABLE, nHWM_INT						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		5.5	V	
Hysteresis	V_{HYS}		500		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = +4.0 mA (Note 26-9)
Leakage Current (ALL - Digital)						(Note 26-8)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Digital Input Capacitance	C_{IN}			10	pF	
H_{VTR} Supply Current Active Mode	I_{HTR}			2	µA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V.

Note 1: Voltages are measured from the local ground potential, unless otherwise specified.

2: Typicals are at TA=25°C and represent most likely parametric norm.

3: The maximum allowable power dissipation at any temperature is PD = (TJmax - TA) / QJA.

4: Timing specifications are tested at the TTL logic levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 26-1 All leakage currents are measured with all pins in high impedance.

Note 26-2 These values are estimated. They will be updated after Characterization. Contact Microchip for the latest values.

Note 26-3 The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

Note 26-4 Max I_{TRI} with V_{CC} = 3.3V (nominal) is 10mA
Max I_{TRI} with V_{CC} = 0V (nominal) is 250uA

Note 26-5 TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

Note 26-6 Total Monitoring Cycle Time for cycle mode includes a one second delay plus all temperature conversions and all analog input voltage conversions.

Note 26-7 Only the nominal default case is shown in this section.

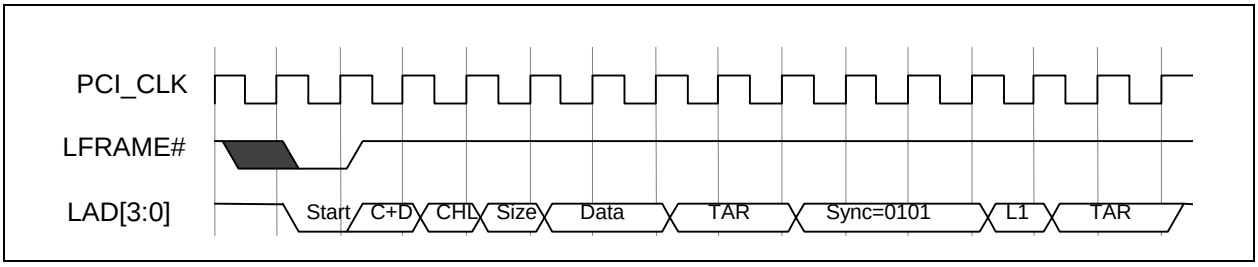
Note 26-8 All leakage currents are measured with all pins in high impedance.

Note 26-9 The low output level for PWM pins is actually +8.0mA.

Note 26-10 The h/w monitor analog block implements a 10-bit ADC. The output of this ADC goes to an average block, which can be configured to accumulate the averaged value of the analog inputs. The amount of averaging is programmable. The output of the averaging block produce a 12-bit temperature or voltage reading value. The 8 MSbits go to the reading register and the 4 LSbits to the A/D LSb register.

Note 26-11 Other platform components may use VID inputs and may require tighter limits.

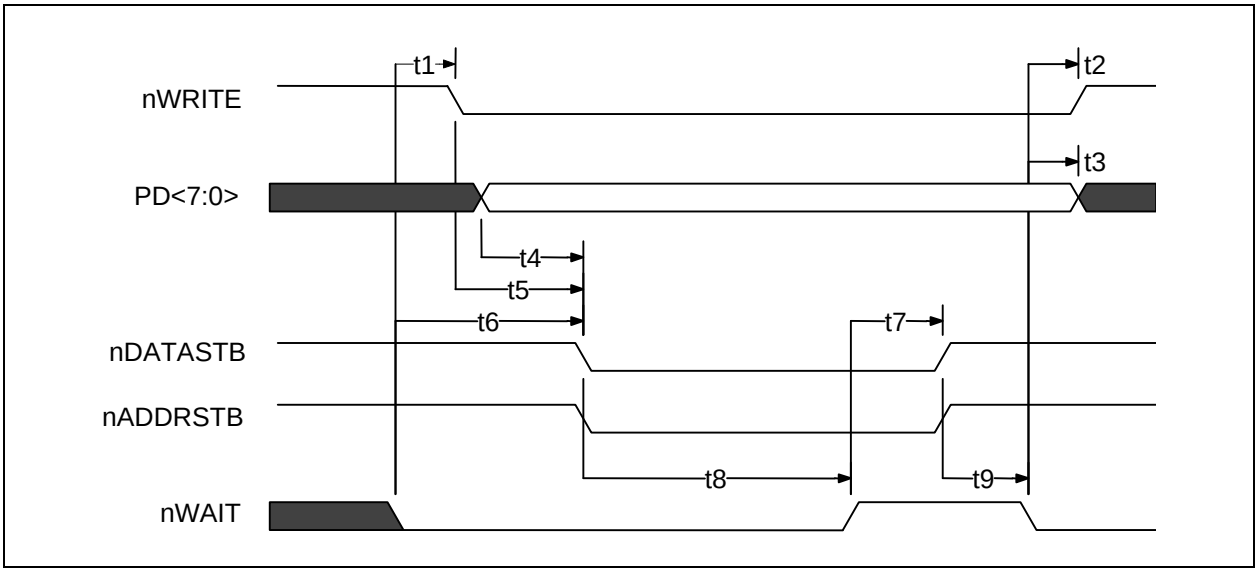
FIGURE 27-11: DMA READ (FIRST BYTE)



Note: L1=Sync of 0000

27.4 Parallel Port Timing

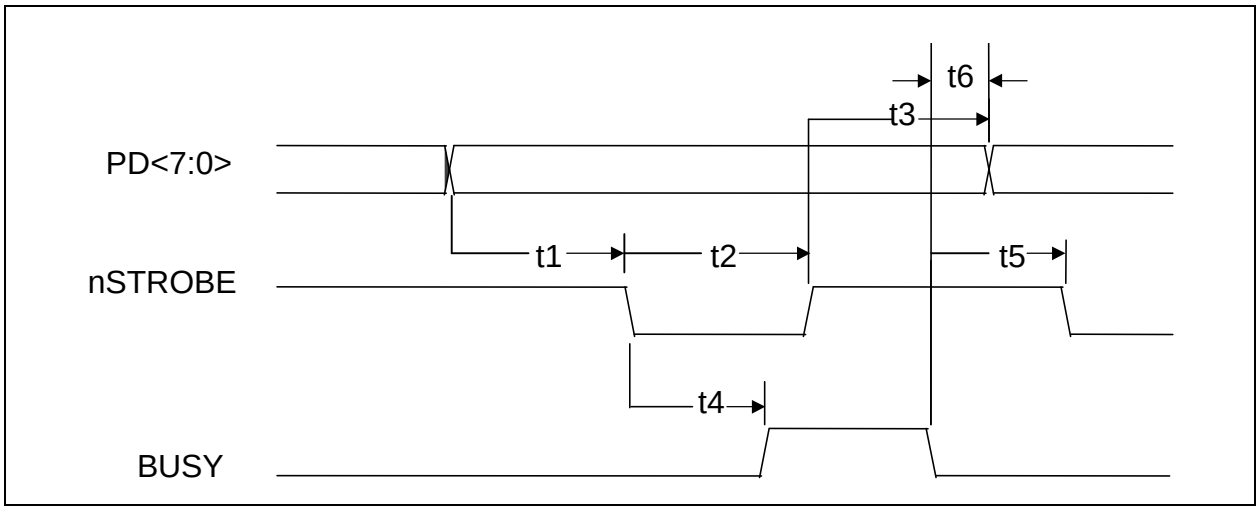
FIGURE 27-12: EPP 1.9 DATA OR ADDRESS WRITE CYCLE



Name	Description	MIN	TYP	MAX	Units
t1	nWAIT Asserted to nWRITE Asserted (See Note 27-2)	60		185	ns
t2	nWAIT Asserted to nWRITE Change (See Note 27-2)	60		185	ns
t3	nWAIT Asserted to PDATA Invalid (See Note 27-2)	0			ns
t4	PDATA Valid to Command Asserted	10			ns
t5	nWRITE to Command Asserted	5		35	ns
t6	nWAIT Asserted to Command Asserted (See Note 27-2)	60		210	ns
t7	nWAIT Deasserted to Command Deasserted (See Note 27-2)	60		190	ns
t8	Command Asserted to nWAIT Deasserted	0		10	µs
t9	Command Deasserted to nWAIT Asserted	0			ns

Note 27-2 nWAIT must be filtered to compensate for ringing on the parallel bus cable. nWAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

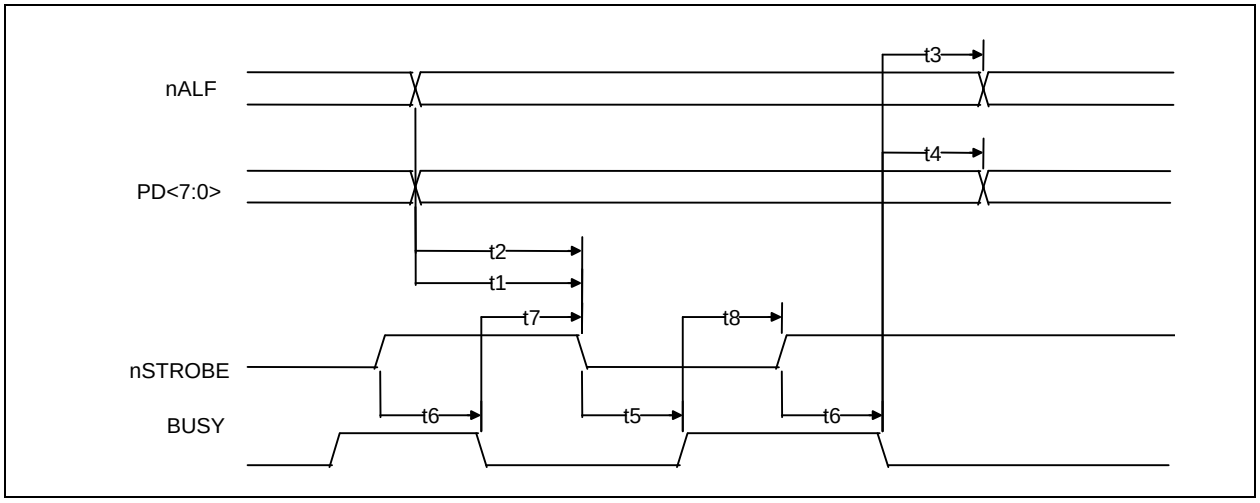
FIGURE 27-16: PARALLEL PORT FIFO TIMING



Name	Description	MIN	TYP	MAX	Units
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (See Note 27-3)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (See Note 27-3)	80			ns

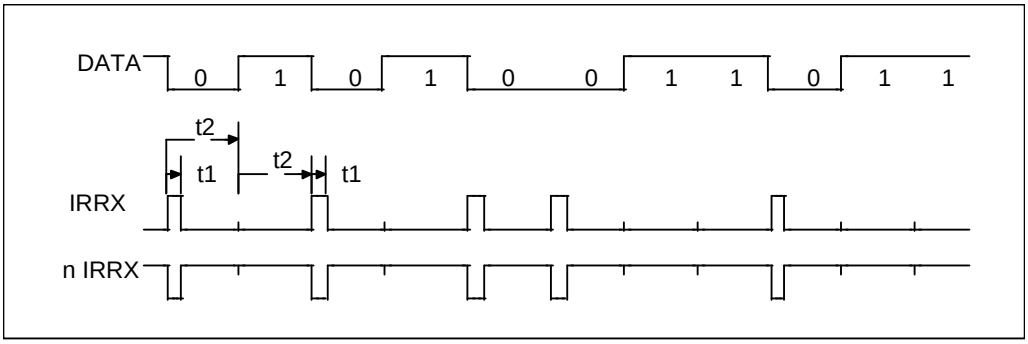
Note 27-3 The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

FIGURE 27-17: ECP PARALLEL PORT FORWARD TIMING



27.5 IR Timing

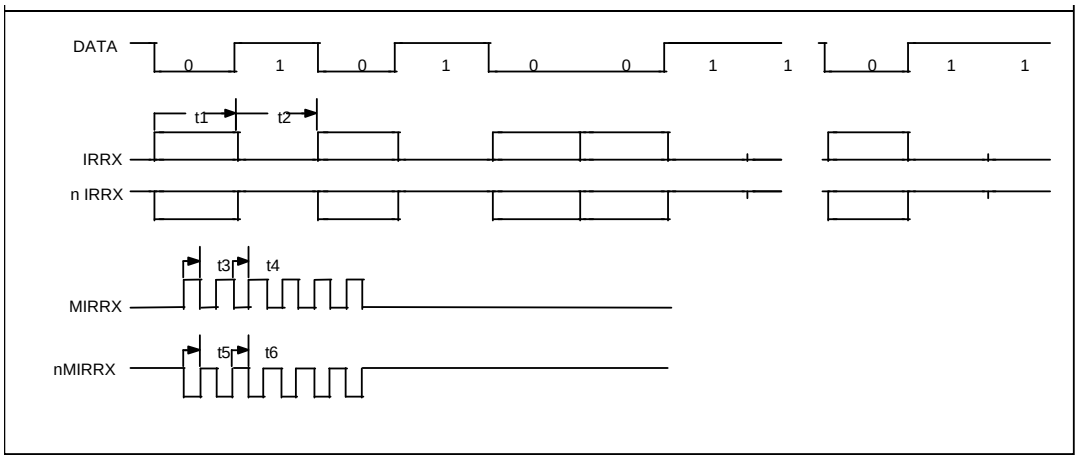
FIGURE 27-19: IRDA RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

FIGURE 27-21: AMPLITUDE SHIFT-KEYED IR RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

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