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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3227-sz-tr

TABLE 2-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
D12	GP11 / TXD3	GP11 / TXD3
E11	GP14 / nDSR3	GP14 / nDSR3
C13	GP17 / nRTS3	GP17 / nRTS3
B13	GP16 / nCTS3	GP16 / nCTS3
C12	GP42 / nIO_PME	GP42 / nIO_PME
D11	VTR	VTR
A13	GP15 / nDTR3	GP15 / nDTR3
B12	GP61 / nLED2 / CLKO	GP61 / nLED2 / CLKO
C11	GP60 / nLED1 / WDT	GP60 / nLED1 / WDT
A12	GP13 / nRI3	GP13 / nRI3
B11	GP12 / nDCD3	GP12 / nDCD3
A11	GP31 / nRI4	GP31 / nRI4
C10	GP63 / nDCD4	GP63 / nDCD4
B10	CLKI32	CLKI32
A10	nRSMRST	nRSMRST
B9	VSS	VSS
C9	GP64 / RXD4	GP64 / RXD4
A9	GP65 / TXD4	GP65 / TXD4
A8	GP66 / nDSR4	GP66 / nDSR4
B8	GP67 / nRTS4	GP67 / nRTS4
C8	GP62 / nCTS4	GP62 / nCTS4
A7	GP34 / nDTR4	GP34 / nDTR4
B7	PWRGD_OUT	PWRGD_OUT
A6	PWRGD_PS	PWRGD_PS
C7	nFPRST / GP30	nFPRST / GP30
E8	VTR	VTR
E7	VSS	VSS
B6	nTHERMTRIP	nTHERMTRIP
A5	nHWM_INT	nHWM_INT
C6	PWM3	PWM3
B5	PWM2	PWM2
A4	PWM1	PWM1
B4	FANTACH3	FANTACH3
C5	FANTACH2	FANTACH2
C4	FANTACH1	FANTACH1
A3	HVSS	HVSS
B3	HVTR	HVTR
A2	REMOTE2-	REMOTE2-
A1	REMOTE2+	REMOTE2+
B1	REMOTE1-	REMOTE1-
C1	REMOTE1+	REMOTE1+
C2	VCCP_IN	VCCP_IN

Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

TABLE 2-2: SCH3226 SUMMARIES BY STRAP OPTION

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
L8	STRAPOPT (=VTR[a])	STRAPOPT (=VSS[a])
C2	+12V_IN	+12V_IN
C1	+5V_IN	+5V_IN
C3	GP40 / DRVDEN0(out)	GP40 / DRVDEN0(out)
D3	VTR	VTR
G5	TEST=VSS[b]	TEST=VSS[b]
D2	VSS	VSS
E3	CLOCKI	CLOCKI
F3	LAD0	LAD0
E2	LAD1	LAD1
D1	LAD2	LAD2
F2	LAD3	LAD3
E1	LFRAME#	LFRAME#
G3	LDRQ#	LDRQ#
F1	PCI_RESET#	PCI_RESET#
G1	PCI_CLK	PCI_CLK
G2	SER_IRQ	SER_IRQ
H1	VSS	VSS
H2	VCC	VCC
H3	GP44 / TXD6	nIDE_RSTDRV / GP44
J2	GP45 / RXD6	nPCIRST1 / GP45
K2	GP46 / nSCIN6	nPCIRST2 / GP46
J3	GP47 / nSCOUT6	nPCIRST3 / GP47
J1	AVSS	AVSS
K1	VBAT	VBAT
K3	GP27 / nIO_SMI / P17	GP27 / nIO_SMI / P17
J4	KDAT / GP21	KDAT / GP21
L2	KCLK / GP22	KCLK / GP22
L3	MDAT / GP32	MDAT / GP32
K4	MCLK / GP33	MCLK / GP33
L4	GP36 / nKBDRST	GP36 / nKBDRST
L5	GP37 / A20M	GP37 / A20M
G7	VSS	VSS
G6	VTR	VTR
K7	nRI1	nRI1
L6	nDCD1	nDCD1
K8	RXD1	RXD1
J8	TXD1 / SIOXNOROUT	TXD1 / SIOXNOROUT
K6	nDSR1	nDSR1
K5	nRTS1 / SYSOPT0	nRTS1 / SYSOPT0
J7	nCTS1	nCTS1
J6	nDTR1 / SYSOPT1	nDTR1 / SYSOPT1
J5	GP50 / nRI2	GP50 / nRI2

TABLE 13-2: PME EVENTS (CONTINUED)

Events	PME	Comment
UART-6		
by IRQ	Y (from group SMI)	
by nRI6 pin	Y	
Hardware Monitor	nHWM_INT	
Watch Dog Timer	Y	
GPIO, total 15 pins	Y	
Low-Battery	Y	Detect on VCC POR only not a S3 wakeup either

The PME function is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in configuration registers 0x60 and 0x61 in Logical.

There are four types of registers which control PME events:

1. PME Wake Status register (PME_STS1, PME_STS3, PME_STS5, PME_STS6.) provides the status of individual wake events.
2. PME Wake Enable (PME_EN1, PME_EN3, PME_EN5, PME_EN6) provides the enable for individual wake events.
3. PME Pin Enable Register (PME_EN,) provides an enable for the PME output pins.
4. PME Pin Status Register (PME_STS) provides the status for the PME output pins.

See Section 24.0, "Runtime Register," on page 213 for detailed register description.

The following describes the behavior to the PME status bits for each event:

Each wake source has a bit in a PME Wake Status register which indicates that a wake source has occurred. The PME Wake Status bits are “sticky“(unless otherwise stated in bit description in Section 24.0): once a status bit is set by the wake-up event, the bit will remains set until cleared by writing a ‘1’ to the bit.

Each PME Wake Status register has a corresponding PME Wake Enable Register.

If the corresponding bit in both in a PME Wake Status register and the PME Wake Enable Register are set then the PME Pin Status Register bit is set. If both corresponding PME Pin Status and the PME Pin Enable Register bit are set then the IO_PME pinIO_PME pin will asserted.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the polarity bit of the GPIO control register. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding PME status bits. Status bits are cleared on a write of '1'.

The PME Wake registers also include status and enable bits for the HW Monitor Block.

See Section 10.11, "Keyboard and Mouse PME Generation," on page 84 for information about using the keyboard and mouse signals to generate a PME.

13.2 Enabling SMI Events onto the PME Pin

There is a bit in the PME Status Register 3 to show the status of the internal “group” SMI signal in the PME logic (if bit 5 of the SMI_EN2 register is set). This bit, DEVINT_STS, is at bit 3 of the PME_STS3 register. When this bit is clear, the group SMI output is inactive. When bit is set, the group SMI output is active.The corresponding Wake-up enable bit is DEVINT_EN, is at bit 3 of the PME_EN3 register.

Bit 5 of the SMI_EN2 register must also be set. This bit is cleared on a write of '1'.

13.3 PME Function Pin Control

The GP42/nIO_PME pin, when selected for the nIO_PME function, can be programmed to be active high or active low via the polarity bit in the GP42 register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the GP42 register. The nIO_PME pin function defaults to active low, open-drain output; however the GP42/nIO_PME pin defaults to the GP42 function.

In the SCH3227/SCH3226/SCH3224/SCH3222 the nIO_PME pin can be programmed to be an open drain, active low, driver. The SCH3227/SCH3226/SCH3224/SCH3222 nIO_PME pin are fully isolated from other external devices that might pull the signal low; i.e., the nIO_PME pin are capable of being driven high externally by another active device or pull-up even when the SCH3227/SCH3226/SCH3224/SCH3222 VCC is grounded, providing VTR power is active. The IO_PME pin driver sinks 6mA at 0.55V max (see section 4.2.1.1 DC Specifications in the "PCI Local Bus Specification, Revision 2.2, December 18, 1998).

13.4 Wake on Specific Key Code

The SCH3227/SCH3226/SCH3224/SCH3222 Wake on Specific Key Code feature is enabled for the assertion of the nIO_PME signal in SX power states by the SPEKEY bit in the PME_STS6 register. This bit defaults to enabled and is Vbat powered.

At Vbat POR the Wake on Specific Key Code feature is disabled. During the first VTR POR and VCC POR the Wake on Specific Key Code feature remains disabled. Software selects the precise Specific Key Code event (configuration) to wake the system and then enables the feature via the SPEKEY bit in the PME_STS6 register. The system then may go the sleep and/or have a power failure. After returning to or remaining in S5 sleep, the system will fully awake by a Wake on Specific Key Code The Specific Key Code configuration and the enable for the nIO_PME are retained via Vbat POR backed registers.

The SCH3227/SCH3226/SCH3224/SCH3222 Wake on Specific Key Code feature is enabled for assertion of the nIO_PME signal when in S3 power state or below by the SPEKEY bit in the PME_EN6 register. This bit defaults to disabled and is VTR powered.

13.5 Wake on Specific Mouse Click

The SPESME SELECT field in the Mouse_Specific_ Wake Register selects which mouse event is routed to the PME_STS6 if enabled by PME_EN6. The KB_MSE_SWAP bit in the Mouse_Specific_ Wake Register can swap the Mouse port and Keyboard interfaces internally.

The Lock bit in the Mouse_Specific_ Wake Register provides a means of changing access to read only to prevent tampering with the Wake on Mouse settings. The other bits in the Mouse_Specific_ Wake Register are VBAT powered and reset on VBAT POR; therefore, the mouse event settings are maintained through a power failure. The lock bit also controls access to the DBLCLICK Register.

The DBLCLICK register contains a numeric value that determines the time interval used to check for a double mouse click. The value is the time interval between mouse clicks. For example, if DBLCLICK is set to 0.5 seconds, you have one half second to click twice for a double-click.

The larger the value in the DBLCLICK Register, the longer you can wait between the first and second click for the SCH3227/SCH3226/SCH3224/SCH3222 to interpret the two clicks as a double-click mouse wake event. If the DBLCLICK value is set to a very small value, even quick double clicks may be interpreted as two single clicks.

The DBLCLICK register has a six bit weighted sum value from 0 to 0x3Fh which provides a double click interval between 0.0859375 and 5.5 seconds. Each incremental digit has a weight of 0.0859375 seconds.

The DBLCLICK Register is VBAT powered and reset on VBAT POR; therefore, the double click setting is maintained through a power failure. The default setting provides a 1.03125 second time interval.

DBLCLICK Writing to the DBLCLICK register shall reset the Mouse Wake-up internal logic and initialize the Mouse Wake-up state machines.The SPEMSE_EN bit in of the CLOCKI32 configuration register at 0xF0 in Logical Device A is used to control the “Wake on Specific Mouse Click” feature. This bit is used to turn the logic for this feature on and off. It will disable the 32KHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:

0= "Wake on Specific Mouse Click" logic is on (default)

1= "Wake on Specific Mouse Click" logic is off

The generation of a PME for this event is controlled by the PME enable bits (SPEMSE_EN bit in the PME_EN6 register and in the SMI_EN2 register) when the logic for feature is turned on. See Section 13.5, "Wake on Specific Mouse Click," on page 96.

APPLICATION NOTE: The Wake on Specific Mouse Click feature requires use of the M_ISO bit in the KRST_GA20 register. See Application Note 8.8 titled “Keyboard and Mouse Wake-up Functionality”.

The state machine used to snoop the incoming data from the keyboard is synchronized by the clock high and low time. If the KCLK signal remains high or low for a nominal 125usec during the transmission of a byte, a timeout event is generated causing the snooping and scan code decoding logic to be reset, such that it will look for the first byte of the make or break scan code.

18.5.1.2 Description Of SCAN 1 and SCAN 2

SCAN 1:

Many standard keyboards (PC/XT, MFII, etc.) generate scan 1 make and break codes per key press. These codes may be generated as a single byte or multi-byte sequences. If a single byte is generated, the make code, which is used to indicate when a key is pressed, is a value between 0h and 7Fh. The break code, which is used to indicate when a key is released, is equal to the make code plus 80h (i.e. 80h ≤ Break Code ≤ FFh). If a multi-byte sequence is sent it will send E0h before the make or break.

Example of Single Byte Scan 1: Make Code = 37h, Break Code=B7h

Example of Multi-byte Scan 1: Make Code = E0h 37h, Break Code = E0h B7h.

SCAN 2:

The scan 2 make and break codes used in AT and PS/2 keyboards, which are defined by the PC 8042 Keyboard Controller, use the same scan code when a key is pressed and when the key is released. A reserved release code, 0xF0, is sent by the keyboard immediately before the key specific portion of the scan code to indicate when that the key is released.

Example of Single Byte Scan 2: Make Code = 37h, Break Code=F0h 37h

Example of Multi-byte Scan 2: Make Code = E0h 37h, Break Code = E0h F0h 37h.

18.5.2 SYSTEM FOR DECODING SCAN CODE MAKE BYTES RECEIVED FROM THE KEYBOARD

Bit [3:2] of the SPEKEY Scan Code register is used to determine if the hardware is required to detect a single byte make code or a multi-byte make code. Table 18-4 summarizes how single byte and multi-byte scan codes are decoded.

FIGURE 18-6: SAMPLE SINGLE-BYTE MAKE CODE

Keyboard Scan Code - Make Byte 1
37h

FIGURE 18-7: SAMPLE MULTI-BYTE MAKE CODE

MSB	LSB
Keyboard Scan Code - Make Byte 1	Keyboard Scan Code - Make Byte 2
E0h	37h

Note: In multi-byte scan codes the most significant byte (MSB) will be received first.

TABLE 18-5: DECODING KEYBOARD SCAN CODE FOR BREAK CODE (CONTINUED)

SPEKEY Scan Code		Scan Code	Number of Bytes in Break Code	Description
Bit[3]	Bit[2]			
1	1	Scan 2	3 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 3 located in the Runtime Register block at offset 63h. If this byte is a valid scan code and it matches the value (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.

Note: To de-assert wake on specific key status event (KB_PB_STS) on any valid break key the register containing the LSB of the break code should be programmed to 00h. If a Keyboard Scan Code – Break Byte register is programmed to 00h then any valid scan code will be a match. The value 00h is treated as a Don't Care.

18.6 Wake on Specific Mouse Event

The device can generate SX wake events (where SX is the sleep state input) based on detection of specific Mouse button clicks on a Mouse connected to the Mouse port interface (MDAT and MCLK pins). The following specific Mouse events can be used for wake-up events:

1. Any button click (left/right/middle) or any movement
2. Any one click of left/right/middle button
3. one click of left button
4. one click of right button
5. two times click of left button
6. two times click of right button

In addition to the Idle detection logic there is Start Bit Time-out logic which detects any time MCLK stays high for more that 115-145us.

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated (Table 21-1). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

TABLE 21-1: AVG[2:0] BIT DECODER

SFTR[7:5]			Measurements per Reading			Nominal Total Conversion Cycle Time (MSEC)
AVG2	AVG1	AVG0	Remote Diode 1	Remote Diode 2	Ambient	
0	0	0	128	128	8	587.4
0	0	1	16	16	1	73.4
0	1	X	16	16	16	150.8
1	X	X	32	32	32	301.5

Note: The default for the AVG[2:0] bits is ‘010’b.

21.7.1 CONTINUOUS MONITORING MODE

In the continuous monitoring mode, the sampling and conversion process is performed continuously for each temperature reading after the Start bit is set high. The time for each temperature reading is shown above for each measurement option.

The continuous monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the START bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown below (see Table 21-2). Sampling of all values occurs in a nominal 150.8 ms (default - see Table 21-2).

TABLE 21-2: ADC CONVERSION SEQUENCE

Sampling Order	Register
1	Remote Diode Temp Reading 1
2	Ambient Temperature reading
3	Remote Diode Temp Reading 2

When the continuous monitoring function is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 150.8 ms (default - see Table 21-2). Each measured value is compared to values stored in the Limit registers. When the measured value violates the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly.

The results of the sampling and conversions can be found in the Reading Registers and are available at any time.

21.7.2 CYCLE MONITORING MODE

In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.151 seconds (1.3 sec max - default averaging enabled). The sampling and conversion of each temperature reading is performed once every monitoring cycle. This is a power saving mode.

The cycle monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown above.

When the cycle monitoring function is started, it cycles through each measurement in sequence, and it produces a converted temperature reading for each input. The state machine waits approximately one second before repeating this process. Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

The nHWM_INT pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding diode error bit to be set. This will cause the nHWM_INT pin to become active if enabled.

The nHWM_INT pin can be enabled to indicate fan errors. Bit[0] of the Interrupt Enable 2 (Fan Tachs) register (80h) is used to enable this option. This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The nHWM_INT pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the nHWM_INT pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to '1' again.

The nHWM_INT pin may only become active while the monitor block is operational.

21.9.2 INTERRUPT AS A PME EVENT

The hardware monitoring interrupt signal is routed to the SIO PME block. For a description of these bits see the section defining PME events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

The THERM PME status bit is located in the PME_STS1 Runtime Register at offset 04h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM PME status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the PME_EN1 register at offset 0Ah.

21.9.3 INTERRUPT AS AN SMI EVENT

The hardware monitoring interrupt signal is routed to the SIO SMI block. For a description of these bits see the section defining SMI events. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

The THERM SMI status bit is located in the SMI_STS5 Runtime Register at offset 14h located in the SIO block.

When a temperature or fan tachometer event causes a status bit to be set, the THERM SMI status bits will be set as long as the corresponding group enable bit is set.

The enable bit is located in the SMI_EN5 register at offset 1Ah.

The SMI is enabled onto the SERIRQ (IRQ2) via bit 6 of the SMI_EN2 register at 17h.

21.9.4 INTERRUPT EVENT ON SERIAL IRQ

The hardware monitoring interrupt signal is routed to the Serial IRQ logic. This signal is unaffected by the nHWM_INT pin enable (INT_EN) bit (See FIGURE 21-3: Interrupt Control on page 128.)

This operation is configured via the Interrupt Select register (0x70) in Logical Device A. This register allows the selection of any serial IRQ frame to be used for the HWM nHWM_INT interrupt (SERIRQ9 slot will be used). See Interrupt Event on Serial IRQ on page 130.

21.10 Low Power Mode

bit The hardware monitor has two modes of operation: Monitoring and Sleep. When the START bit, located in Bit[0] of the Ready/Lock/Start register (0x40), is set to zero the hardware monitor is in Sleep Mode. When this bit is set to one the hardware monitor is fully functional and monitors the analog inputs to this device.
bit Sleep mode is a low power mode in which bias currents are on and the internal oscillator is on, but the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

Note 1: In Sleep Mode the PWM Pins are held high forcing the PWM pins to 100% duty cycle (256/256).

2: The START a bit cannot be modified when the LOCK bit is set.

21.13.3 PWM FAN SPEED CONTROL

The following description applies to PWM1, PWM2, and PWM3.

Note: The PWM output pins are held low when VCC=0. The PWM pins will be forced to “spinup” when PWRGD_PS goes active. See “Spin Up” on page 137.

The PWM pin reflects a duty cycle that is determined based on 256 PWM duty cycle intervals. The minimum duty cycle is “off”, when the pin is low, or “full on” when the pin is high for 255 intervals and low for 1 interval. The INVERT bit (bit 4 of the PWMx Configuration registers at 80h-82h) can be used to invert the PWM output, however, the default operation (following a VCC POR) of the part is based on the PWM pin active high to turn the fans “on”. When the INVERT bit is set, as long as power is not removed from the part, the inversion of the pin will apply thereafter.

When describing the operation of the PWMs, the terms “Full on” and “100% duty cycle” means that the PWM output will be high for 255 clocks and low for 1 clock (INVERT bit = 0). The exception to this is during fan spin-up when the PWM pin will be forced high for the duration of the spin-up time.

The SCH322x can control each of the PWM outputs in one of two modes:

- Manual Fan Control Operating Mode: software controls the speed of the fans by directly programming the PWM duty cycle.
- Auto Fan Control Mode: the device automatically adjusts the duty cycle of the PWM outputs based on temperature, according to programmed parameters.

These modes are described in sections that follow.

21.13.3.1 Manual Fan Control Operating Mode (Test Mode)

When operating in Manual Fan Control Operating Mode, software controls the speed of the fans by directly programming the PWM duty cycle. The operation of the fans can be monitored based on reading the temperature and tachometer reading registers and/or by polling the interrupt status registers. The SCH322x offers the option of generating an interrupt indicated by the nHWM_INT signal.

To control the PWM outputs in manual mode:

- To set the mode to operate in manual mode, write ‘111’ to bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWMx Configuration.
- The speed of the fan is controlled by the duty cycle set for that PWM output. The duty cycle must be programmed in Registers 30h-32h: Current PWM Duty

To monitor the fans:

Fans equipped with Tachometer outputs can be monitored via the FANTACHx input pins. See Section 21.14.2, "Fan Speed Monitoring," on page 150.

If an out-of-limit condition occurs, the corresponding status bit will be set in the Interrupt Status registers. Setting this status bit will generate an interrupt signal on the nHWM_INT pin (if enabled). Software must handle the interrupt condition and modify the operation of the device accordingly. Software can evaluate the operation of the Fan Control device through the Temperature and Fan Tachometer Reading registers.

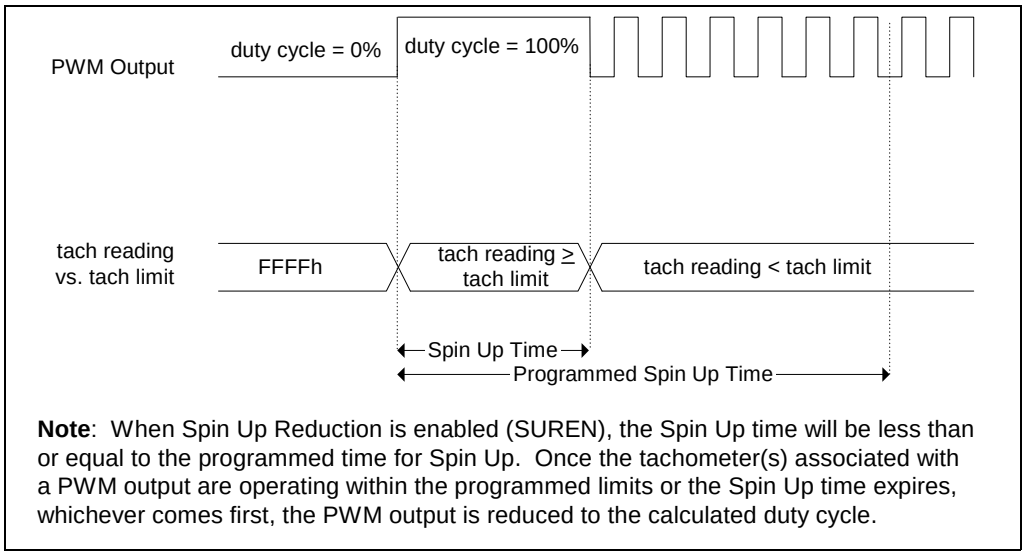
When in manual mode, the current PWM duty cycle registers can be written to adjust the speed of the fans, when the start bit is set. These registers are not writable when the lock bit is set.

Note: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

21.13.3.2 Auto Fan Control Operating Mode

The SCH322x implements automatic fan control. In Auto Fan Mode, this device automatically adjusts the PWM duty cycle of the PWM outputs, according to the flow chart on the following page (see FIGURE 21-4: Automatic Fan Control Flow Diagram on page 135).

FIGURE 21-6: SPIN UP REDUCTION ENABLED



Note: When Spin Up Reduction is enabled (SUREN), the Spin Up time will be less than or equal to the programmed time for Spin Up. Once the tachometer(s) associated with a PWM output are operating within the programmed limits or the Spin Up time expires, whichever comes first, the PWM output is reduced to the calculated duty cycle.

This feature defaults to enabled; it can be disabled by clearing bit 4 of the Configuration register (7Fh). If disabled, the all fans go to 100% duty cycle for the duration of their associated spin up time. Note that the Tachometer x minimum registers must be programmed to a value less than FFFFh in order for the spin up reduction to work properly.

Note 1: The tachometer reading register always gives the actual reading of the tachometer input.

2: No interrupt bits are set during spin-up.

21.13.3.4 Hottest Option

If the “Hottest” option is chosen (101 or 110), then the fan is controlled by the limits and parameters associated with the zone that requires the highest PWM duty cycle value, as calculated by the auto fan algorithm.

21.13.3.5 Ramp Rate Control Logic

The Ramp Rate Control Logic, if enabled, limits the amount of change in the PWM duty cycle over a specified period of time. This period of time is programmable in the Ramp Rate Control registers located at offsets 62h and 63h.

21.13.3.5.1 Ramp Rate Control Disabled: (default)

The Auto Fan Control logic determines the duty cycle for a particular temperature. If PWM Ramp Rate Control is disabled, the PWM output will be set to this calculated duty cycle.

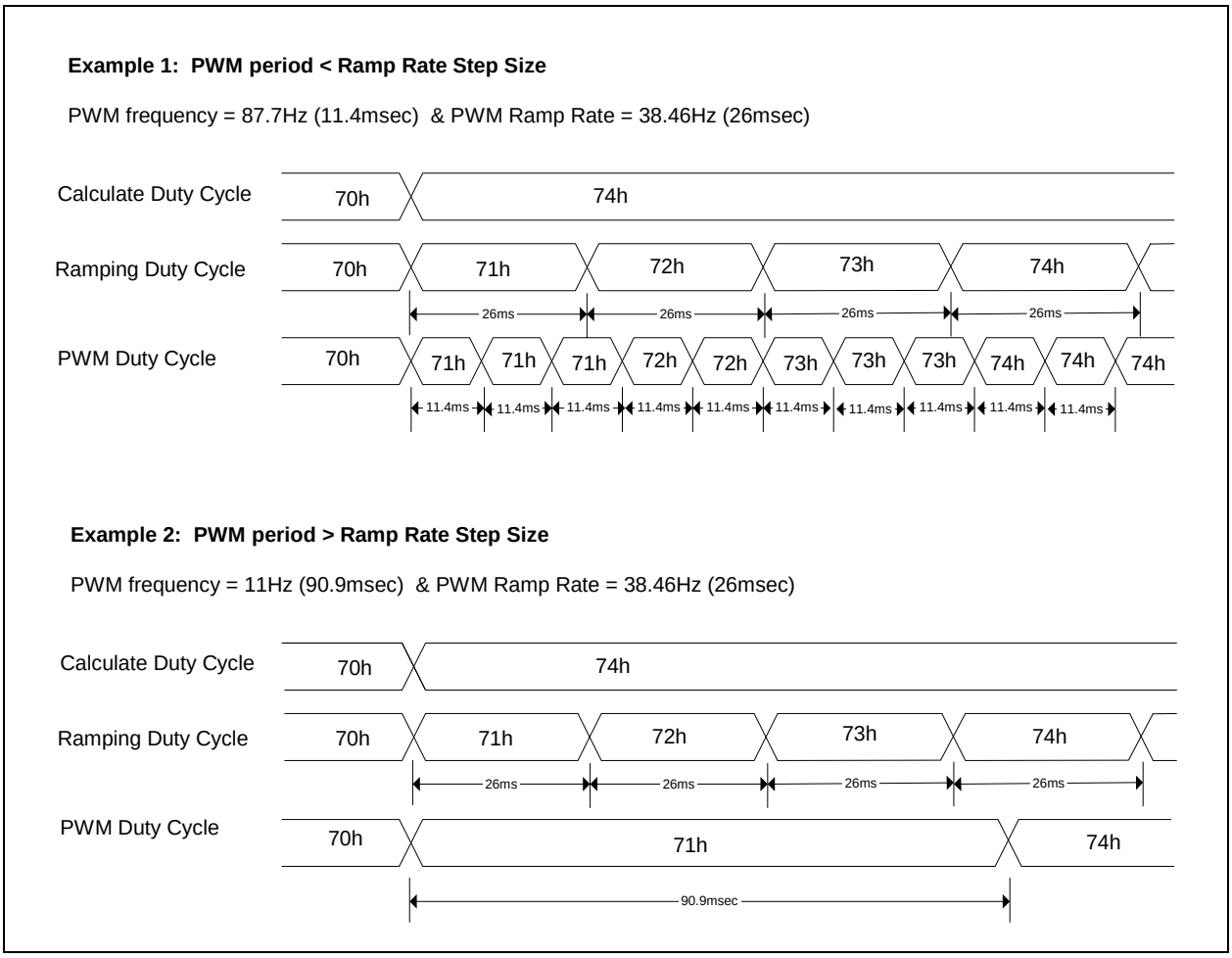
21.13.3.5.2 Ramp Rate Control Enabled:

If PWM Ramp Rate Control is enabled, the PWM duty cycle will Ramp up or down to the new duty cycle computed by the auto fan control logic at the programmed Ramp Rate. The PWM Ramp Rate Control logic compares the current duty cycle computed by the auto fan logic with the previous ramp rate duty cycle. If the current duty cycle is greater than the previous ramp rate duty cycle the ramp rate duty cycle is incremented by ‘1’ at the programmed ramp rate until it is greater than or equal to the current calculated duty cycle. If the current duty cycle is less than the previous ramp rate duty cycle, the ramp rate duty cycle is decremented by ‘1’ until it is less than or equal to the current duty cycle. If the current PWM duty cycle is equal to the calculated duty cycle the PWM output will remain unchanged.

Internally, the PWM Ramp Rate Control Logic will increment/decrement the internal PWM Duty cycle by ‘1’ at a rate determined by the Ramp Rate Control Register (see Table 21-4). The actual duty cycle output is changed once per the period of the PWM output, which is determined by the frequency of the PWM output. (See FIGURE 21-7: Illustration of PWM Ramp Rate Control on page 140.)

- If the period of the PWM output is less than the step size created by the PWM Ramp Rate, the PWM output will hold the duty cycle constant until the Ramp Rate logic increments/decrements the duty cycle by ‘1’ again. For example, if the PWM frequency is 87.7Hz (1/87.7Hz = 11.4msec) and the PWM Step time is 206msec, the PWM

FIGURE 21-7: ILLUSTRATION OF PWM RAMP RATE CONTROL



Note 1: The PWM Duty Cycle latches the Ramping Duty Cycle on the rising edge of the PWM output.

2: The calculated duty cycle, ramping duty cycle, and the PWM output duty cycle are asynchronous to each other, but are all synchronized to the internal 90kHz clock source.

It should be noted that the actual duty cycle on the pin is created by the PWM Ramp Rate Control block and latched on the rising edge of the PWM output. Therefore, the current PWM duty cycle may lag the PWM Calculated Duty Cycle.

21.13.4 OPERATION OF PWM PIN FOLLOWING A POWER CYCLE

This device has special features to control the level and operation of the PWM pin following a Power Cycle. These features are PWM Clamping and Forced Spinup.

21.13.4.1 PWM Clamp

The PWM pin has the option to be held low for 0 seconds or 2 seconds following a VCC POR. This feature is selectable by a Vbat powered register bit in the SIO Runtime Register block.

Bit[7] of the DBLCLICK register at offset 5Bh is used to select the 0 or 2 second option.

This bit is defined as follows:

- BIT[3] ZERO_SPINUP
  - 1 = zero delay for spin up
  - 0 = delay spinup by 2 seconds (default)

21.15 High Frequency PWM Options

Note: If a fan with a tachometer output is driven by the high frequency PWM option, the tachometer must be monitored in Mode 1 only.

21.15.1 PWM FREQUENCIES SUPPORTED

The SCH322x supports low frequency and high frequency PWMs. The low frequency options are 11.0Hz, 14.6Hz, 21.9Hz, 29.3Hz, 35.2Hz, 44.0Hz, 58.6Hz and 87.7Hz. The high frequency options are 15kHz, 20kHz, 25kHz and 30kHz. All PWM frequencies are derived from the 14.318MHz clock input.

The frequency of the PWM output is determined by the Frequency Select bits[3:0]. The default PWM frequency is 25kHz.

22.2.3 REGISTERS 25-27H: TEMPERATURE READING

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
25h	R	Remote Diode 1 (Zone 1) Temp Reading	7	6	5	4	3	2	1	0	N/A
26h	R	Internal Diode (Zone 2) Temp Reading	7	6	5	4	3	2	1	0	N/A
27h	R	Remote Diode 2 (Zone 3) Temp Reading	7	6	5	4	3	2	1	0	N/A

The Temperature Reading registers reflect the current temperatures of the internal and remote diodes. Remote Diode 1 Temp Reading register reports the temperature measured by the Remote1- and Remote1+ pins, Remote Diode 2 Temp Reading register reports the temperature measured by the Remote2- and Remote2+ pins, and the Internal Diode Temp Reading register reports the temperature measured by the internal (ambient) temperature sensor. Current temperatures are represented as 12 bit, 2's complement, signed numbers in Celsius. The 8MSbs are accessible in the temperature reading registers. Table 22-3 shows the conversion for the 8-bit reading value shown in these registers. The extended precision bits for these readings are accessible in the A/D Converter LSBs Register (85h-86h). The Temperature Reading register will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly (this corresponds to the diode fault interrupt status bits). The Temperature Reading registers will be updated automatically by the SCH322x Chip with a minimum frequency of 4Hz.

Note: These registers are read only – a write to these registers has no effect.

Each of the temperature reading registers are mapped to a zone. Each PWM may be programmed to operate in the auto fan control operating mode by associating a PWM with one or more zones. The following is a list of the zone associations.

- Zone 1 is controlled by Remote Diode 1 Temp Reading
- Zone 2 is controlled by Internal Temp Reading (Ambient Temperature Sensor)
- Zone 3 is controlled by Remote Diode 2 Temp Reading

Note: To read a 12-bit reading value, software must read in the order of MSB then LSB. If several readings are being read at the same time, software can read all the MSB registers then the corresponding LSB registers. For example: Read RD1 Reading, RD2 Reading, then A/D Converter LSbs Reg1, which contains the LSbs for RD1 and RD2.

TABLE 22-3: TEMPERATURE VS. REGISTER READING

Temperature	Reading (DEC)	Reading (HEX)
-127°c	-127	81h
. . .	. . .	. . .
-50°c	-50	CEh
. . .	. . .	. . .
0°c	0	00h
. . .	. . .	. . .
50°c	50	32h
. . .	. . .	. . .
127°c	127	7Fh
(SENSOR ERROR)		80h

Note 22-15 There is a start-up time of up to 301.5ms (default - see Table 21-2, “ADC Conversion Sequence,” on page 126) for monitoring after the start bit is set to ‘1’, during which time the reading registers are not valid. Software can poll the TRDY bit located in the Configuration Register (7Fh) to determine when the voltage and temperature readings are valid.The following summarizes the operation of the part based on the Start bit:

1. If Start bit = '0' then:
   a) Fans are set to Full On.
   b) No temperature or fan tach monitoring is performed. The values in the reading registers will be N/A (Not Applicable), which means these values will not be considered valid readings until the Start bit = '1'. The exception to this is the Tachometer reading registers, which always give the actual reading on the TACH pins.
   c) No Status bits are set.
2. If Start bit = '1'
   a) All fan control and monitoring will be based on the current values in the registers. There is no need to preserve the default values after software has programmed these registers because no monitoring or auto fan control will be done when Start bit = '0'.
   b) Status bits may be set.

Note: Once programmed, the register values will be saved when start bit is reset to ‘0’.

22.2.10 REGISTER 41H: INTERRUPT STATUS REGISTER 1

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
41h	R/WC	Interrupt Status 1	INT2 Note 22 -16	D2	AMB	D1	5V	VCC	Vccp	2.5V	00h

Note 22-16 This is a read-only bit. Writing ‘1’ to this bit has no effect.

Note 1: This register is reset to its default value when the PWRGD_PS signal transitions high.

2: The is a read/write-to-clear register. Bits[6:4] are cleared on a write of one if the temperature event is no longer active. Writing a zero to these bits has no effect.

Bit[7] INT2

This bit indicates that a status bit is set in the Interrupt Status Register 2 Register. Therefore, S/W can poll this register, and only if bit 7 is set does the other registers need to be read. This bit is cleared (set to 0) automatically by the device if there are no bits set in the Interrupt Status Register 2.

Bits[6:0] Individual Status Bits

Bits[6:0] of the Interrupt Status Register 1 are automatically set by the device whenever the measured temperature on Remote Diode 1, Internal Diode, or the Remote Diode 2 Temperature violates the limits set in the corresponding temperature limit registers. These individual status bits remain set until the bit is written to one by software or until the individual enable bit is cleared, even if the temperatures no longer violate the limits set in the limit registers.

- Clearing the status bits by a write of ‘1’
  - The voltage status bits are cleared (set to 0) automatically by the SCH322x after they are written to one by software, if the voltage readings no longer violate the limit set in the limit registers. See Registers 44-4Dh, 9B-9Eh: Voltage Limit Registers on page 169.
  - The temperature status bits are cleared (set to 0) automatically by the SCH322x after they are written to one by software, if the temperature readings no longer violate the limit set in the limit registers. See Registers 4E-53h: Temperature Limit Registers on page 170.
- Clearing the status bits by clearing the individual enable bits.
  - Clearing or setting the individual enable bits does not take effect unless the START bit is 1. No interrupt status events can be generated when START=0 or when the individual enable bit is cleared. If the status bit is one and the START bit is one then clearing the individual enable bit will immediately clear the status bit. If the status bit is one and the START bit is zero then clearing the individual enable bit will have no effect on the status bit until the START bit is set to one. Setting the START bit to one when the individual enable bit is zero will

TABLE 23-9: DMA CHANNEL SELECT

Name	REG Index	Definition
DMA Channel Select Default=0x02 or 0x04 **(See notes)** on VCC POR, VTR POR, PCI RESET and SOFT RESET	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00= Reserved 0x01= DMA1 0x02= DMA2 0x03= DMA3 0x04-0x07= No DMA active

Note 1: A DMA channel is activated by setting the DMA Channel Select register to [0x01-0x03] AND:

2: For the PP logical device in ECP mode by setting dmaEn, bit D3 of the ecr.

3: The DMA channel must be disabled if not used/selected by any Logical Device. Refer to Note A.

4: The default value of the DMA Channel Select register for logical device 3 and 5 is 0x04.

Note 23-9 Logical Device IRQ and DMA Operation. IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel must be disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (Active bit or address not valid).

Serial Ports:

Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic “0”, the serial port interrupt is disabled.

Disabling DMA Enable bit, disables DMA for UART2. Refer to the IrCC specification.

Parallel Port:

SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to “0”, IRQ is disabled.

ECP Mode:

- (DMA) dmaEn from ecr register. See table.
- IRQ - See table.

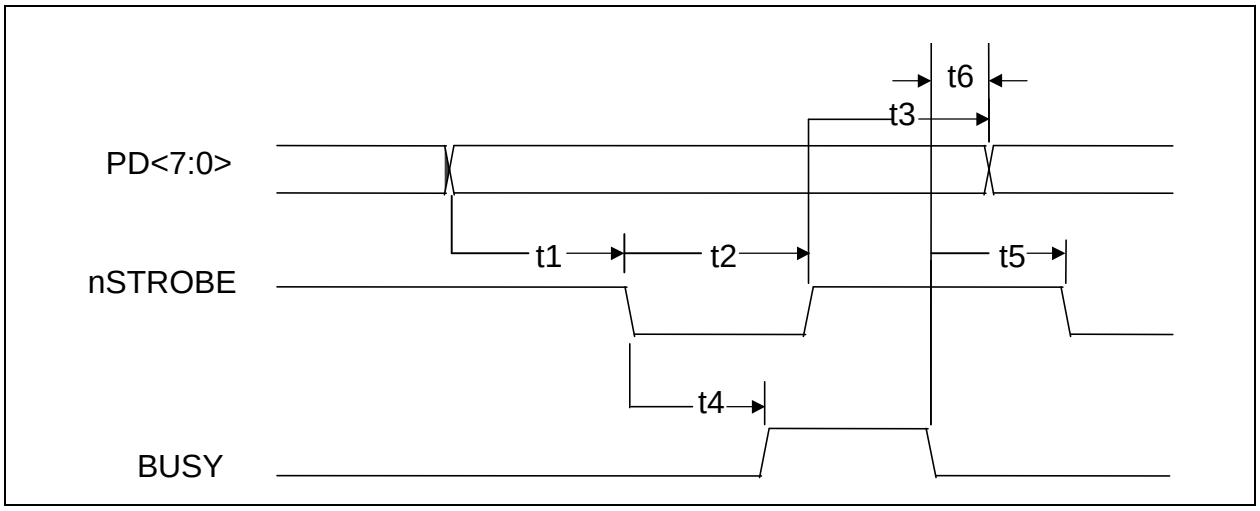
Mode (From ECG Register)		IRQ Controlled By	DMA Controlled By
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

Keyboard Controller: Refer to the 8042 Keyboard Controller Description on page 77 **of this document.**

MCHP Defined Logical Device Configuration Registers

The MCHP Specific Logical Device Configuration Registers reset to their default values only on PCI resets generated by Vcc or VTR POR (as shown) or the PCI_RESET# signal. These registers are not affected by soft resets.

FIGURE 27-16: PARALLEL PORT FIFO TIMING



Name	Description	MIN	TYP	MAX	Units
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (See Note 27-3)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (See Note 27-3)	80			ns

Note 27-3 The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

FIGURE 27-17: ECP PARALLEL PORT FORWARD TIMING

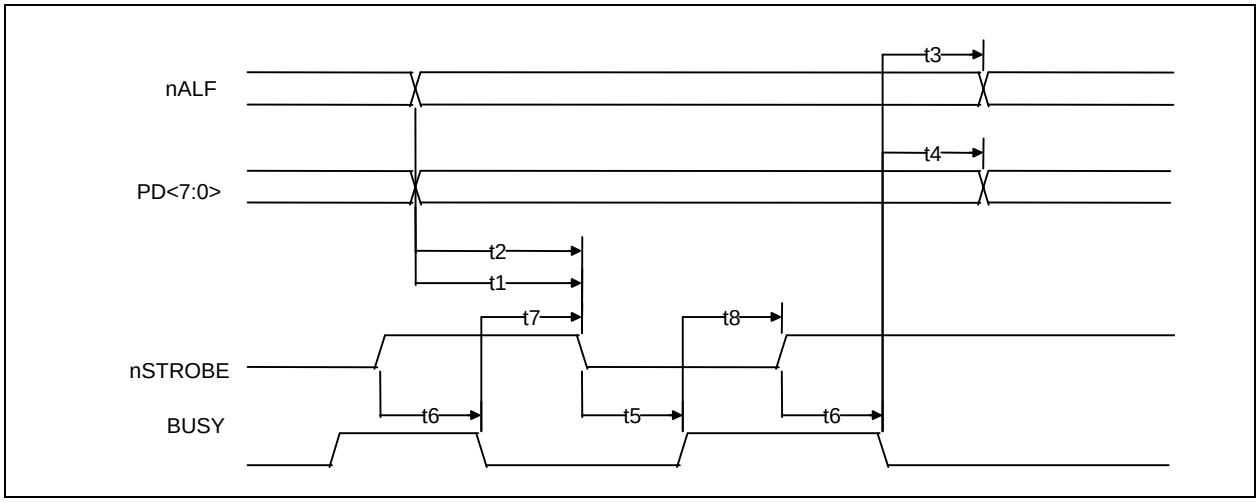
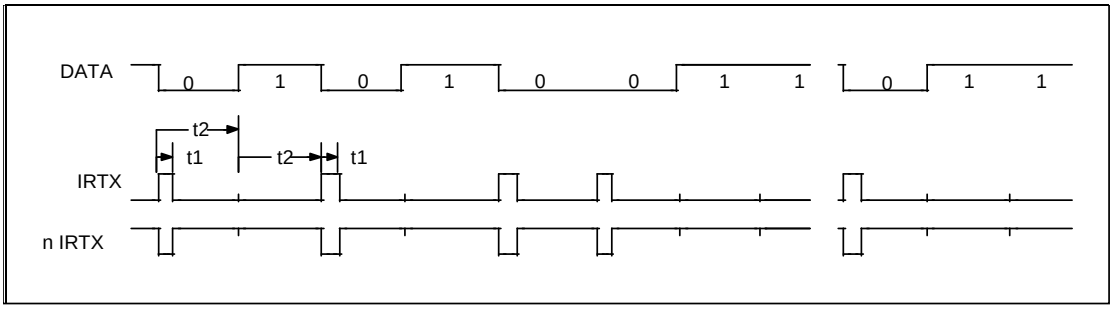


FIGURE 27-20: IRDA TRANSMIT TIMING



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

27.9 Resume Reset Signal Generation

nRSMRST signal is the reset output for the ICH resume well. This signal is used as a power on reset signal for the ICH.

SCH322x detects when VTR voltage raises above VTRIP, provides a delay before generating the rising edge of nRSMRST. See definition of VTRIP on page 275.

This delay, tRESET_DELAY, (t1 on page 275) is nominally 350ms, starts when VTR voltage rises above the VTRIP trip point. If the VTR voltage falls below VTRIP the during tRESET_DELAY then the following glitch protection behavior is implemented:. When the VTR voltage rises above VTRIP, nRSMRST will remain asserted the full tRESET_DELAY after which nRSMRST is deasserted.

On the falling edge there is minimal delay, tRESET_FALL.

Timing and voltage parameters are shown in Figure 27-26 and Table 27-1.

FIGURE 27-26: RESUME RESET SEQUENCE

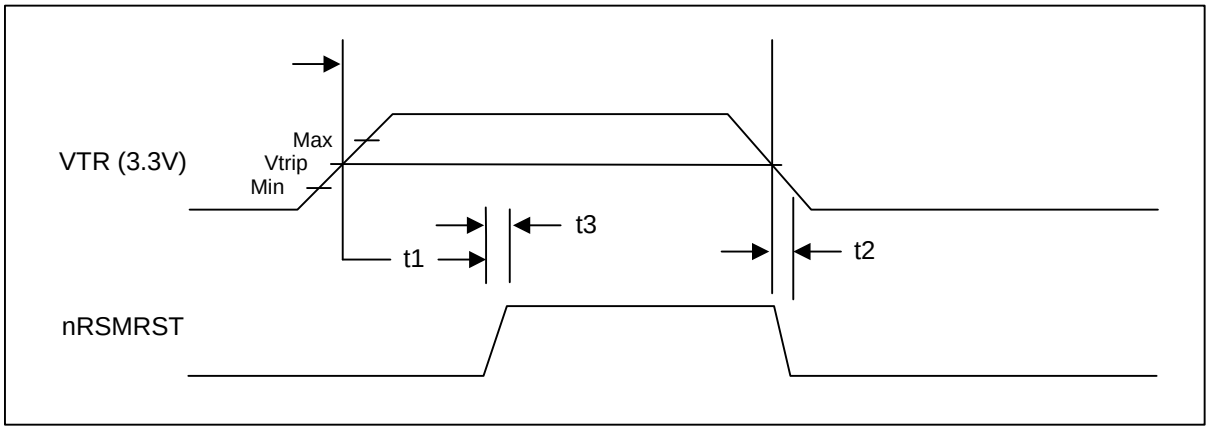


TABLE 27-1: RESUME RESET TIMING

Name	Description	MIN	TYP	MAX	Units	Notes
t1	tRESET_DELAY: VTR active to nRSMRST inactive	140	350	560	msec	
t2	tRESET_FALL: VTR inactive to nRSMRST active (Glitch width allowance)			100	nsec	
t3	tRESET_RISE			100	nsec	
V_{TRIP}	VTR low trip voltage	2.7	2.8	2.9	V	

APPLICATION NOTE: The 5 Volt Standby power supply must power up before or simultaneous with VTR, and must power down simultaneous with or after VTR (from ICH2 data sheet.) SCH322x does not have a 5 Volt Standby power supply input and does not respond to incorrect 5 Volt Standby power - VTR sequencing.

27.12 PWM Outputs

The following section shows the timing for the PWM[1:3] outputs.

FIGURE 27-30: PWMX OUTPUT TIMING

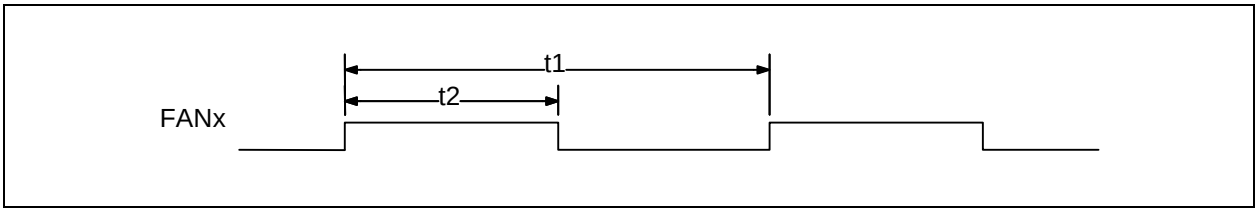


TABLE 27-2: TIMING FOR PWM[1:3] OUTPUTS

Name	Description	MIN	TYP	MAX	Units
t1	PWM Period (Note 1) - low frequency option - high frequency option	 11.4 10.7		 90.9 42.7	 msec usec
t2	PWM High Time (Note 2)	0		99.6	%

Note 1: This value is programmable by the PWM frequency bits located in the FRFx registers.

2: The PWM High Time is based on a percentage of the total PWM period (min=0/256*T_{PWM}, max =255/256*T_{PWM}). During Spin-up the PWM High Time can reach a 100% or Full On. (T_{PWM} = t1).

APPENDIX B: EXAMPLE FAN CIRCUITS

The following figures show examples of circuitry on the board for the PWM outputs, tachometer inputs, and remote diodes. Figure B-1 shows how the part can be used to control four fans by connecting two fans to one PWM output.

Note:

- These examples represent the minimum required components. Some designs may require additional components.
- The SCH3222 device does not support fan control.

FIGURE B-1: FAN DRIVE CIRCUITRY FOR LOW FREQUENCY OPTION (APPLY TO PWM DRIVING TWO FANS)