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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3227-sz

TABLE 2-2: SCH3226 SUMMARIES BY STRAP OPTION (CONTINUED)

Ball#	Function: StrapOPT=1	Function: StrapOPT=0
L9	VTR	VTR
L7	VSS	VSS
K9	GP51 / nDCD2	GP51 / nDCD2
J9	GP52 / RXD2(IRRX2)	GP52 / RXD2(IRRX2)
H9	GP53 / TXD2(IRTX2)	GP53 / TXD2(IRTX2)
G9	GP54 / nDSR2	GP54 / nDSR2
L10	GP55 / nRTS2 / RESGEN	GP55 / nRTS2 / RESGEN
K10	GP56 / nCTS2	GP56 / nCTS2
J10	GP57 / nDTR2	GP57 / nDTR2
H10	RXD5	PB_OUT#
K11	TXD5	PS_ON#
J11	nSCOUT5	PB_IN#
H11	nSCIN5	SLP_SX#
F9	GP10 / RXD3	GP10 / RXD3
G10	GP11 / TXD3	GP11 / TXD3
E9	GP14 / nDSR3	GP14 / nDSR3
F10	GP17 / nRTS3	GP17 / nRTS3
G11	GP16 / nCTS3	GP16 / nCTS3
F11	GP42 / nIO_PME	GP42 / nIO_PME
E10	VTR	VTR
E11	GP15 / nDTR3	GP15 / nDTR3
D9	GP61 / nLED2 / CLKO	GP61 / nLED2 / CLKO
D10	GP60 / nLED1 / WDT	GP60 / nLED1 / WDT
D11	GP13 / nRI3	GP13 / nRI3
C11	GP12 / nDCD3	GP12 / nDCD3
C10	GP31 / nRI4	GP31 / nRI4
C9	GP63 / nDCD4	GP63 / nDCD4
B11	CLKI32	CLKI32
B10	nRSMRST	nRSMRST
A10	VSS	VSS
C8	GP64 / RXD4	GP64 / RXD4
B9	GP65 / TXD4	GP65 / TXD4
A9	GP66 / nDSR4	GP66 / nDSR4
B8	GP67 / nRTS4	GP67 / nRTS4
A8	GP62 / nCTS4	GP62 / nCTS4
C7	GP34 / nDTR4	GP34 / nDTR4
A7	PWRGD_OUT	PWRGD_OUT
B7	PWRGD_PS	PWRGD_PS
E7	nFPRST / GP30	nFPRST / GP30
F7	VTR	VTR
C6	VSS	VSS
B6	nTHERMTRIP	nTHERMTRIP
E6	nHWM_INT	nHWM_INT
A6	PWM3	PWM3

6.1.3 INTERRUPT ENABLE REGISTER (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SCH3227/SCH3226/SCH3224/SCH3222. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic “1”.

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic “1”.

Bit 2

This bit enables the Received Line Status Interrupt when set to logic “1”. The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic “1”. This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic “0”.

6.1.4 FIFO CONTROL REGISTER (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level.

Note:	DMA is not supported. The UART1 and UART2 FCRs are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x21).

Bit 0

Setting this bit to a logic “1” enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic “0” disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic “1” clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic “1” clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the Trigger Level For The Rcvr Fifo Interrupt.

6.1.5 INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 6-2 on page 39). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic “0”, an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic “1”, no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table (Table 6-2).

Bit 3

In non-FIFO mode, this bit is a logic “0”. In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic “0”.

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

TABLE 6-2: INTERRUPT CONTROL

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.

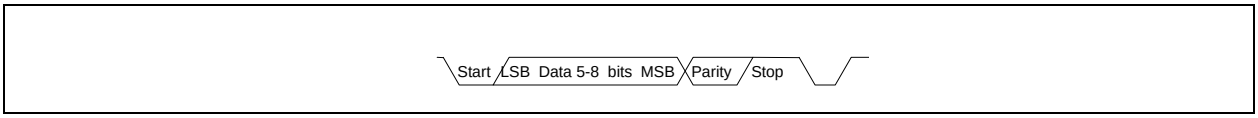
TABLE 6-2: INTERRUPT CONTROL (CONTINUED)

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

6.1.6 LINE CONTROL REGISTER (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

FIGURE 6-1: SERIAL DATA



This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

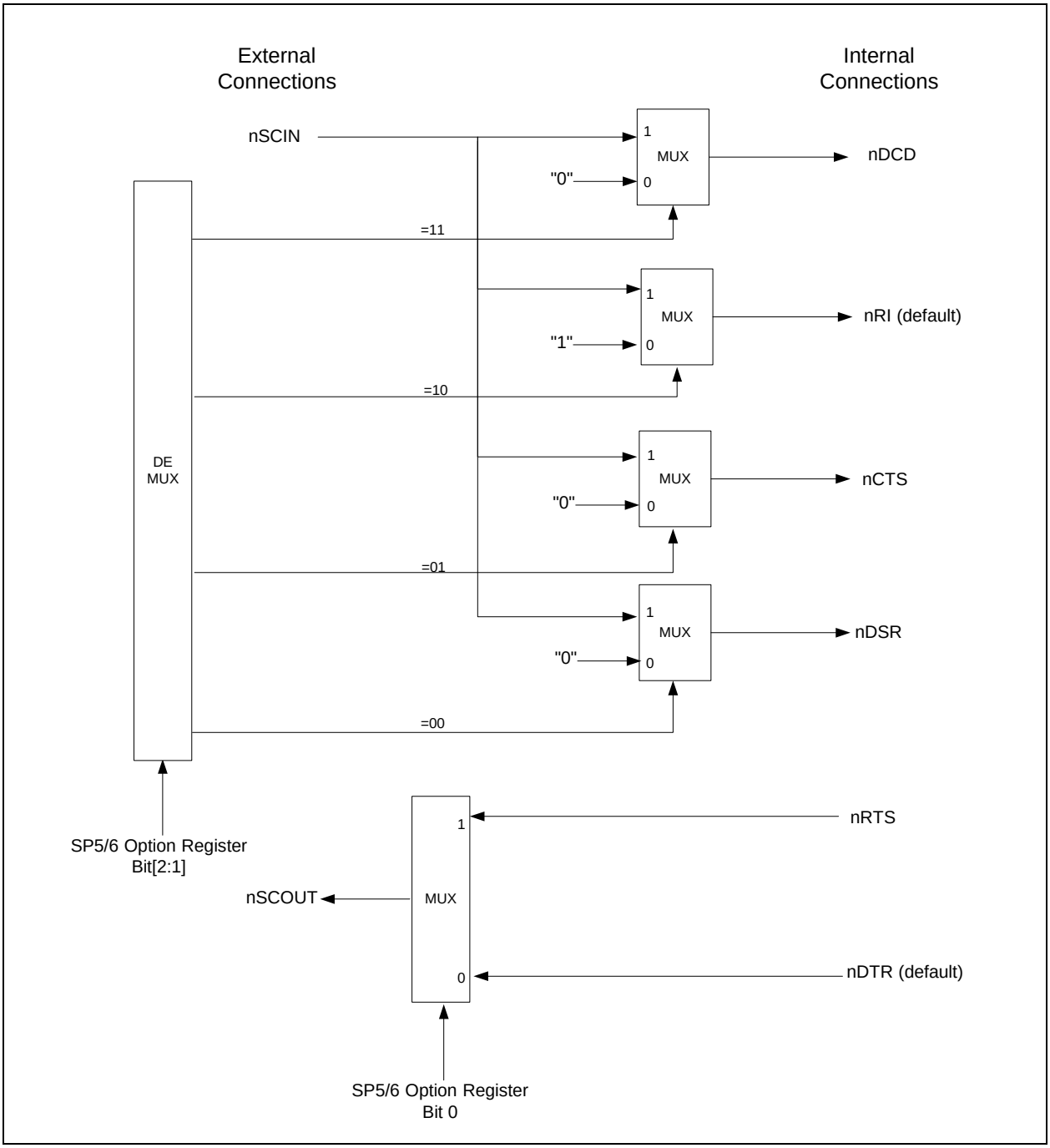
Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

Bit 2	Word Length	Number of Stop Bits
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

FIGURE 6-5: REDUCE PIN SERIAL PORT CONTROL SIGNAL SELECTION



For SP5, the port signals are nRTS5, nDTR5, nSCOUT5 and nSCIN5. The nSCOUT5 signal may be either nRTS5 or nDTR5, selected via an SP5 option bit in a register.

The nSCIN5 signal may be either the nDSR5, nCTS5, nRI5 or nDCD5 signals, as selected via a bit in the SP5 option register.

For SP6, the nSCOUT6 signal may be either nRTS6 or nDTR6, selected via SP6 option bit. The nSCIN6 signal may be either the nDSR6, nCTS6, nRI6 or nDCD6 signals, as selected via a bit in theSP6 option register. The programming for the SP5 and SP6 Option register is given in Section 24.0, "Runtime Register," on page 213.

7.1.16 EPP 1.7 READ

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. The chip inserts wait states into the I/O read cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

- The host sets PDIR bit in the control register to a logic “1”. This deasserts nWRITE and tri-states the PData bus.
- The host initiates an I/O read cycle to the selected EPP register.
- Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
- If nWAIT is asserted, the chip inserts wait states into the I/O read cycle until the peripheral deasserts nWAIT or a time-out occurs.
- The Peripheral drives PData bus valid.
- The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
- The chip drives the final sync and deasserts nDATASTB or nADDRSTRB.
- Peripheral tri-states the PData bus.
- Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

TABLE 7-2: EPP PIN DESCRIPTIONS

EPP Signal	EPP Name	Type	EPP Description
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
nWAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
nDATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
nRESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
nADDRSTB	Address Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.

Note 1: SPP and EPP can use 1 common register.

2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

7.2.20 PROGRAMMED I/O - TRANSFERS FROM THE HOST TO THE FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

10.10 Port 92 Fast GATEA20 and Keyboard Reset

Port 92 Register

This port can only be read or written if Port 92 has been enabled via bit 2 of the KRST_GA20 Register (Logical Device 7, 0xF0) set to 1.

This register is used to support the alternate reset (nALT_RST) and alternate A20 (ALT_A20) functions.

Name	Port 92
Location	92h
Default Value	24h
Attribute	Read/Write
Size	8 bits

Port 92 Register	
Bit	**Function**
7:6	Reserved. Returns 00 when read
5	Reserved. Returns a 1 when read
4	Reserved. Returns a 0 when read
3	Reserved. Returns a 0 when read
2	Reserved. Returns a 1 when read
1	ALT_A20 Signal control. Writing a 0 to this bit causes the ALT_A20 signal to be driven low. Writing a 1 to this bit causes the ALT_A20 signal to be driven high.
0	Alternate System Reset. This read/write bit provides an alternate system reset function. This function provides an alternate means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the Keyboard controller. This bit is set to a 0 by a system reset. Writing a 1 to this bit will cause the nALT_RST signal to pulse active (low) for a minimum of 1 µs after a delay of 500 ns. Before another nALT_RST pulse can be generated, this bit must be written back to a 0.

NGATEA20		
8042 P21	**ALT_A20**	**System NA20M**
0	0	0
0	1	1
1	0	1
1	1	1

Bit 0 of Port 92, which generates the nALT_RST signal, is used to reset the CPU under program control. This signal is AND'ed together externally with the reset signal (nKBDRST) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the keyboard controller. Writing a 1 to bit 0 in the Port 92 Register causes this signal to pulse low for a minimum of 6µs, after a delay of a minimum of 14µs. Before another nALT_RST pulse can be generated, bit 0 must be set to 0 either by a system reset of a write to Port 92. Upon reset, this signal is driven inactive high (bit 0 in the Port 92 Register is set to 0).

If Port 92 is enabled, i.e., bit 2 of KRST_GA20 is set to 1, then a pulse is generated by writing a 1 to bit 0 of the Port 92 Register and this pulse is AND'ed with the pulse generated from the 8042. This pulse is output on pin KRESET and its polarity is controlled by the GPI/O polarity configuration.

11.0 GENERAL PURPOSE I/O (GPIO)

The SCH322x provides a set of flexible Input/Output control functions to the system designer through the independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

CAUTION: This device architecture contains registers, controlling GPIOs that may not be brought out to package pins in some specific family members. See Table 2-1 SCH3227, Table 2-2 SCH3226, Table 2-3 SCH3224, or Table 2-4 SCH3222, for the pins that are brought out. Pins which are not brought out must not be used because they are tied to known states internally. Do not change their configurations from their POR defaults, because doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system.

11.1 GPIO Pins

The following pins include GPIO functionality. These pins are defined in the table below.

TABLE 11-1: GPIO PIN FUNCTIONALITY

GPIO Pin Name (Default Func/ Alternate Funcs)	GPIO PWRWELL	VTR POR	SMI/PME	Note
GP10 GP10 / RXD3	VCC	0x01		11-3
GP11 GP11 / TXD3	VTR	0x01		11-3
GP12 GP12 / nDCD3	VTR	0x01		11-3
GP13 GP13 / nRI3	VTR	0x01	PME	11-3, 11-4
GP14 GP14 / nDSR3	VTR	0x01		11-3
GP15 GP15 / nDTR3	VTR	0x01		11-3
GP16 GP16 / nCTS3	VCC	0x01		11-3
GP17 GP17 / nRTS3	VTR	0x01		11-3
KDAT/GP21	VCC	0x8C	SMI/PME	11-1, 11-3
KCLK/GP22	VCC	0x8C	SMI/PME	11-1, 11-3
GP27/nIO_SMI /P17	VCC	0x01	nIO_SMI/PME	11-1
nFPRST / GP30	VTR	0x05		11-3
GP31 GP31 / nRI4	VTR	0x01	PME	11-3, 11-4 11-5
MDAT/GP32	VCC	0x84	SMI/PME	11-1 11-3
MCLK/GP33	VCC	0x84	SMI/PME	11-1 11-3
GP34 GP34 / nDTR4	VTR	0x01		11-3 11-5
GP36/nKBDRST	VCC	0x01	-	
GP37/A20M	VCC	0x01	-	
GP40/DRVDEN0	VCC	0x01	-	
GP42/nIO_PME	VTR	0x01	SMI	
nIDE_RSTDRV / GP44 GP44 / TXD6	VTR	0x01		11-3

15.0 PROGRAMMABLE CLOCK OUTPUT

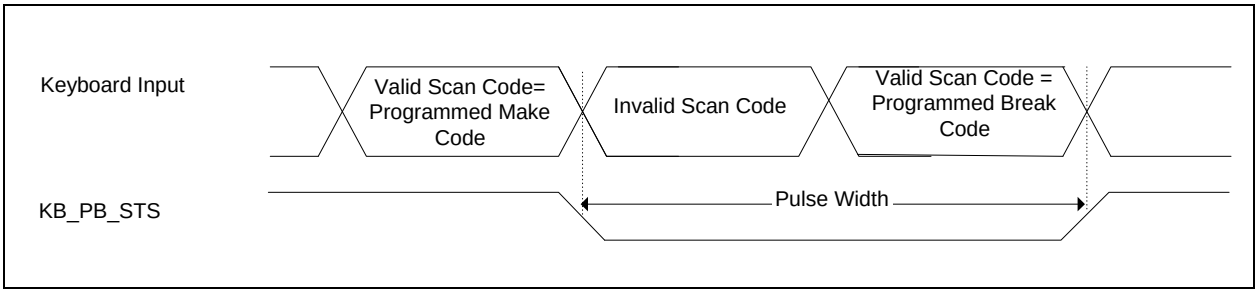
A CLK_OUT pin is available on the SCH322x. This will output a programmable frequency between 0.5 Hz to 16 Hz, and have the following characteristics:

- Must run when Vcc if off - could use 32Khz clock
- Accuracy is not an issue
- CLOCK_OUT register at offset 3Ch in runtime registers with the following programming:
  - Options for 0.25, 0.5, 1, 2, 4, 8, or 16 Hz

APPLICATION NOTE: No attempt has been made to synchronize the clock. As a result, glitches will occur on the clock output when different frequencies are selected.

CLOCK Output Control Register VTR POR = 0x00	3C (R/W)	Bit[0] Enable 1= Output Enabled 0= Disable Clock output Bit[3:1] Frequency Select 000= 0.25 Hz 001= 0.50 Hz 010= 1.00 Hz 011= 2.00 Hz 100= 4.00 Hz 101= 8.00 Hz 110= 16 hz 111 = reserved Bit[7:4] Reserved

FIGURE 18-10: OPTION 3: DE-ASSERT KB_PB_STS WHEN SCAN CODE EQUAL BREAK CODE.



Note: The SPEKEY ScanCode bits are located in the register Keyboard PWRBTN/SPEKEY located at offset 64h.

TABLE 18-5: DECODING KEYBOARD SCAN CODE FOR BREAK CODE

SPEKEY Scan Code		Scan Code	Number of Bytes in Break Code	Description
Bit[3]	Bit[2]			
0	0	Scan 1	1 Byte	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit.
0	1	Scan 1	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.
1	0	Scan 2	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deasset the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.

- The ERRx status bits are cleared (set to 0) automatically by the SCH322x after they are written to one by software, if the Diode Fault condition no longer exists. The remote diode fault bits do not get cleared while the fault condition exists.

• Clearing the status bits by clearing the individual enable bits.

- Clearing or setting the individual enable bits does not take effect unless the START bit is 1. No interrupt status events can be generated when START=0 or when the individual enable bit is cleared. If the status bit is one and the START bit is one then clearing the individual enable bit will immediately clear the status bit. If the status bit is one and the START bit is zero then clearing the individual enable bit will have no effect on the status bit until the START bit is set to one. Setting the START bit to one when the individual enable bit is zero will clear the status bit. Setting or clearing the START bit when the individual enable bit is one has no effect on the status bits.

Note 1: The individual enable bits for FANTACH[1:3] are located in Register 80h: Interrupt Enable 2 Register on page 181. The ERRx bits are enabled by the Remote Diode Limit error bits located in Register 82h: Interrupt Enable 3 Register on page 182

2: Clearing the group FANTACH or Temp enable bits or the global INTEN enable bit has no effect on the status bits.

Bit	Name	R/W	Default	Description
0	+12v_Error	R	0	The SCH322x automatically sets this bit to 1 when the 12V input voltage is less than or equal to the limit set in the 12V Low Limit register or greater than the limit set in the 12V High Limit register.
1	Reserved	R	0	Reserved
2	FANTACH1 Slow/Stalled	R/WC	0	The SCH322x automatically sets this bit to 1 when the FANTACH1 input reading is above the value set in the Tach1 Minimum MSB and LSB registers.
3	FANTACH2 Slow/Stalled	R/WC	0	The SCH322x automatically sets this bit to 1 when the FANTACH2 input reading is above the value set in the Tach2 Minimum MSB and LSB registers.
4	FANTACH3 Slow/Stalled	R/WC	0	The SCH322x automatically sets this bit to 1 when the FANTACH3 input reading is above the value set in the Tach3 Minimum MSB and LSB registers.
5	Reserved	R	0	Reserved
6	Remote Diode 1 Fault	R/WC	0	The SCH322x automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote1+ or Remote1- thermal diode input pins. If the START bit is set and a fault condition exists, the Remote Diode 1 reading register will be forced to 80h.
7	Remote Diode 2 Fault	R/WC	0	The SCH322x automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote2+ or Remote2- thermal diode input pins. If the START bit is set and a fault condition exists, the Remote Diode 2 reading register will be forced to 80h.

22.2.12 REGISTERS 44-4DH, 9B-9EH: VOLTAGE LIMIT REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	Vccp Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	Vccp High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	VCC Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	VCC High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh

Note: If a bit is set in this register, an interrupt can be generated if the TOP_INT_EN bit (register B7h) and, for the nHWM_INT pin to go active, the INT_EN bit (7Ch) is set.

22.2.58 REGISTER BAH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
BAh	R/W	MCHP Reserved	RES	RES	RES	RES	RES	RES	RES	RES	03h

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

22.2.59 REGISTER BBH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
BBh	R	MCHP Reserved	7	6	5	4	3	2	1	0	00h

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

22.2.60 REGISTER 0BDH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
BDh	R	MCHP Reserved	7	6	5	4	3	2	1	0	N/A

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

22.2.61 REGISTER BFH: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
BFh	R/W	MCHP Reserved	RES	RES	RES	RES	RES	RES	RES	RES	00h

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

22.2.62 REGISTER C0H: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C0h	R/W	MCHP Reserved	RES	RES	RES	RES	RES	RES	RES	RES	00h

This is an MCHP Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

22.2.63 REGISTER C1H: MCHP RESERVED REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C1h	R/W	Thermtrip Control	RES	RES	RES	RES	RES	RES	THERM-TRIP_C-TRL	RES	01h

THERMTRIP_CTRL: Bit 1 in the Thermtrip Control register. May be enabled to assert the Thermtrip# pin if programmed limits are exceeded as indicated by the Thermtrip Status register 1=enable, 0=disable (default).

22.2.64 REGISTERS C4-C5, C9H: THERMTRIP TEMPERATURE LIMIT ZONE REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
C4h	R/W	THERMTRIP Temp Limit ZONE 1 (Remote Diode 1)	7	6	5	4	3	2	1	0	7Fh
C9h	R/W	THERMTRIP Temp Limit ZONE 2 (Ambient)	7	6	5	4	3	2	1	0	7Fh
C5h	R/W	THERMTRIP Temp Limit ZONE 3 (Remote Diode 2)	7	6	5	4	3	2	1	0	7Fh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The nTHERMTRIP pin can be configured to assert when one of the temperature zones is above its associated THERMTRIP temperature limit (THERMTRIP Temp Limit ZONES 1-3). The THERMTRIP temperature limit is a separate limit register from the high limit used for setting the interrupt status bits for each zone.

The THERMTRIP Temp Limit ZONE 1-3 registers represent the upper temperature limit for asserting nTHERMTRIP pin for each zone. These registers are defined as follows:

If the monitored temperature for the zone exceeds the value set in the associated THERMTRIP Temp Limit ZONE 1-3 registers, the corresponding bit in the THERMTRIP status register will be set. The nTHERMTRIP pin may or may not be set depending on the state of the associated enable bits (in the THERMTRIP Output Enable register).

Note: The zone must exceed the limits set in the associated THERMTRIP Temp Limit ZONE 1-3 register for two successive monitoring cycles in order for the nTHERMTRIP pin to go active (and for the associated status bit to be set).

22.2.65 REGISTER CAH: THERMTRIP STATUS REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CAh	R/WC	THERMTRIP Status	RES	RES	RES	RES	RES	RD 2	RD 1	AMB	00h
Note:	Each bit in this register is cleared on a write of 1 if the event is not active.										

Note: This register is reset to its default value when the PWRGD_PS signal transitions high.

This register holds a bit set until the bit is written to 1 by software. The contents of this register are cleared (set to 0) automatically by the device after it is written by software, if the nTHERMTRIP pin is no longer active. Once set, the Status bits remain set until written to 1, even if the nTHERMTRIP pin is no longer active.

Bits[2:0] THERMTRIP zone status bits (one bit per zone). A status bit is set to ‘1’ if the associated zone temp exceeds the associated THERMTRIP Temp Limit register value.

22.2.66 REGISTER CBH: THERMTRIP OUTPUT ENABLE REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
CBh	R/W	THERMTRIP Output Enable	RES	RES	RES	RES	RES	RD2	RD1	AMB	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits[2:0] in THERMTRIP Output Enable register, THERMTRIP output enable bits (one bit per zone). Each zone may be individually enabled to assert the nTHERMTRIP pin if the zone temperature reading exceeds the associated THERMTRIP Temp Limit register value. 1=enable, 0=disable (default).

22.2.71 REGISTERS E2H: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

22.2.72 REGISTERS E3H: MCHP TEST REGISTER

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	MCHP Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

22.2.73 REGISTER E9-EEH: MCHP TEST REGISTERS

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
E9h	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EAh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EBh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
ECh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EDh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h
EEh	R/W	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

These are MCHP Test Registers. Writing to these registers may cause unwanted results.

22.2.74 REGISTER FFH: MCHP TEST REGISTER

Register Address	Read/ Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
FFh	R	MCHP Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an MCHP Test register.

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PME_STS6 Default = 0x00 or 0x01 on VTR POR The default will be 0x01 if there is a LOW_BAT event under VBAT power only, 0x00 if the event does not occurs. Bit[0] will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	07 (R/WC)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME pin. Bit[0] LOW_BAT, Cleared by a write of '1'. When the battery is removed and replaced or the if the battery voltage drops below 1.2V under battery power, then the LOW_BAT PME status bit is set on VTR POR. When the battery voltage drops below 2.4 volts under VTR power (VCC=0) or under battery power only, the LOW_BAT PME status bit is set on VCC POR. The corresponding enable bit must be set to generate a PME. The low battery event is not a PME wakeup event. Bit[1] RESERVED. Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_STS (Wake on specific mouse click) Bit[5] SPEKEY_STS (Wake on specific key) Bit[6] PB_STS Bit[7] Reserved The PME Status register is not affected by VCC POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Status Register has no effect.
PME_EN1 Default = 0x00 on VTR POR	08 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_EN bit is "1", the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] Reserved Bit[6] IRINT Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PME_EN3 Default = 0x00 on VTR POR	09 (R/W)	PME Wake Status Register 3 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_EN bit is "1", the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] WDT Bit[1] GP21 Bit[2] GP22 Bit[3] DEVINT_EN (Enable bit for group SMI signal for PME) Bit[4] GP27 Bit[5] GP32 Bit[6] GP33 Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.

25.0 VALID POWER MODES

The following table shows the valid power states for each power supply to the device.

TABLE 25-1: VALID POWER STATES

Power Supply	Power State		
	S0-S2	S3	S4-S5
Vbat	On Off (Note 25-1)	On Off (Note 25-1)	On Off (Note 25-1)
VTR	On	On	On
VCC	On	Off	Off
HVTR	On (HVTR=VTR)	On (HVTR=VTR)	On (HVTR=VTR)

Note 25-1 Although this is not considered normal operating mode, Vbat = Off is a valid power state. When Vbat is off all battery backed system context will be lost.

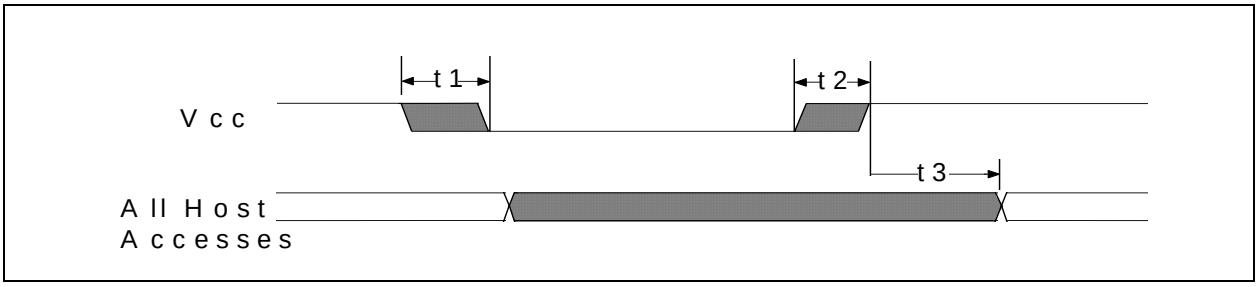
27.0 TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

Name	Capacitance Total (pF)
SER_IRQ	50
LAD [3:0]	50
LDRQ#	50
nDIR	240
nSTEP	240
nDS0	240
PD[0:7]	240
nSTROBE	240
nALF	240
KDAT	240
KCLK	240
MDAT	240
MCLK	240
LED1	50
LED2	50
TXD1	50
TXD2	50
TXD3	50
TXD4	50
TXD5	50
TXD6	50

27.1 Power Up Timing

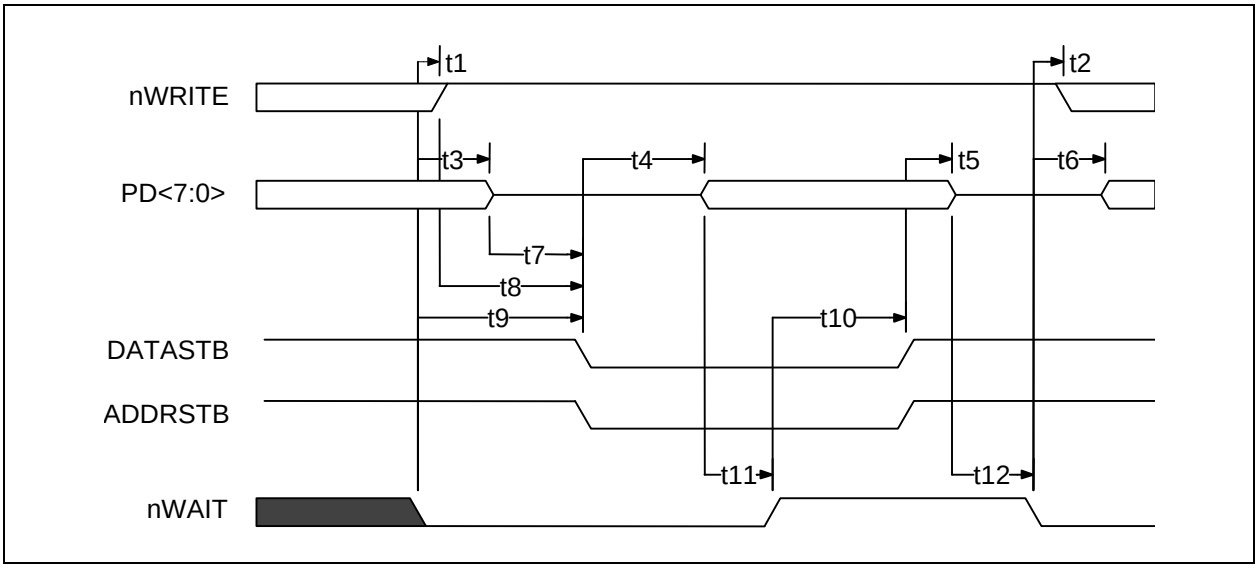
FIGURE 27-1: POWER-UP TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Power-up (See Note 27-1)	125		500	µs

Note 27-1 Internal write-protection period after Vcc passes 2.7 volts on power-up.

FIGURE 27-13: EPP 1.9 DATA OR ADDRESS READ CYCLE

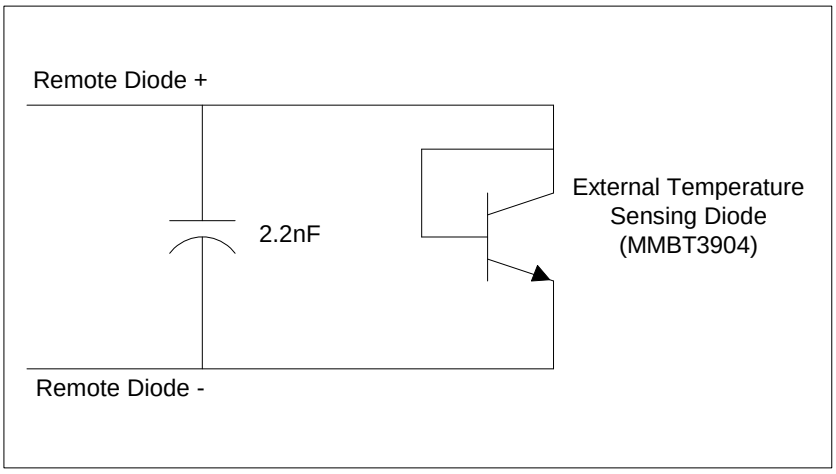


Name	Description	MIN	TYP	MAX	Units
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (Notes 1,2)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (Note 1)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			µs

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.

2: When not executing a write cycle, EPP nWRITE is inactive high.

FIGURE B-4: REMOTE DIODE (APPLY TO REMOTE2 LINES)



Note 1: 2.2nF cap is optional and should be placed close to the SCH322x f used.

2: The voltage at PWM3 must be at least 2.0V to avoid triggering Address Enable.

3: The Remote Diode + and Remote Diode - tracks should be kept close together, in parallel with grounded guard tracks on each side. Using wide tracks will help to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended. See Figure B-5, "Suggested Minimum Track Width and Spacing".

FIGURE B-5: SUGGESTED MINIMUM TRACK WIDTH AND SPACING