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Details	
Product Status	Active
Applications	I/O Controller
Core Processor	8042 Keyboard Controller
Program Memory Type	ROM (2kB)
Controller Series	-
RAM Size	256 x 8
Interface	IrDA, LPC, Parallel, Serial, UART
Number of I/O	40
Voltage - Supply	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-WFBGA
Supplier Device Package	144-WFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sch3227i-sz

TABLE 2-5: SCH322X PIN FUNCTIONS DESCRIPTION (CONTINUED)

Note	Name	Description	VCC Power Plane	VTR-POWER Plane	VCC=0 Operation (Note 2-14)	Buffer Modes (Note 2-1)
2-12	nPCIRST1 / GP45	PCI Reset output 1 GPIO with Schmitt trigger input	nPCIRST1	GP45	NO GATE	(O8/OD8) / (IS/O8/OD8)
2-12	nIDE_RSTDRV / GP44	IDE Reset output GPIO with Schmitt trigger input	nIDE_RSTDRV	GP44	NO GATE	(O4/OD4) / (IS/O4/OD4)
GLUE LOGIC						
	PB_IN#	Power Button In is used to detect a power button event		PB_IN#	NO GATE	I
2-9	SLP_SX#	Sx Sleep State Input Pin.		SLP_SX#	NO GATE	I
	PB_OUT#	Power Button Out		PB_OUT#	NO GATE	O8
	PS_ON#	Power supply On		PS_ON#	NO GATE	O12
MISCELLANEOUS PINS						
	GP42/ nIO_PME	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in either S3 or S5 and below.		GP42/ nIO_PME	NO GATE	(I/O12/OD12) /(O12/OD12)
2-8, 2-9	GP60 /nLED1 /WDT	General Purpose I/O /nLED1 Watchdog Timer Output		GP60 /nLED1 /WDT	NO GATE	(I/O12/OD12) /(O12/OD12) /(O12/OD12)
	nFPRST / GP30	Front Panel Reset / General Purpose IO		nFPRST / GP30	NO GATE	ISPU_400 / (I/O4/OD4)
	PWRGD_PS	Power Good Input from Power Supply		PWRGD_PS	NO GATE	ISPU_400
	PWRGD_OUT	Power Good Output – Open Drain		PWRGD_OUT	NO GATE	OD8
	nRSMRST	Resume Reset Output		nRSMRST	NO GATE	OD24
2-8, 2-9	GP61 /nLED2 / CLKO	General Purpose I/O /nLED2 / Programmable Clock Output		GP61 /nLED2 / CLKO	NO GATE	(I/O12/OD12) / (O12/OD12) / (O12/OD12)
2-9	GP27 /nIO_SMI /P17	General Purpose I/O /System Mgt. Interrupt /8042 P17 I/O	GP27 /nIO_SMI /P17	GP27	/ HI-Z	(I/O12/OD12) /(O12/OD12) /(I/O12/OD12)
HARDWARE MONITORING BLOCK						
	nHWM_INT	Interrupt output for Hardware monitor		nHWM_INT		OD8
2-10	+5V_IN	Analog input for +5V	HVTR			I_{AN}
2-10	+2.5_IN	Analog input for +2.5V	HVTR			I_{AN}
2-10	VCCP_IN	Analog input for +Vccp (processor voltage: 1.5 V nominal).	HVTR			I_{AN}
2-10	+12V_IN	Analog input for +12V	HVTR			I_{AN}

6.0 SERIAL PORT (UART)

The SCH3227/SCH3226/SCH3224/SCH3222 family incorporates up to four full function UARTs and up to two 4 pin UARTS, for a total of 6 available. They are register compatible with the ACE architecture (NS16450, NS16C550A). The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic “1”. OUT2 being a logic “0” disables that UART’s interrupt. The second UART also supports IrDA, HP-SIR and ASK-IR modes of operation.

6.1 Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Section 23.0, "Configuration Registers," on page 194). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The register set of the UARTS are described below.

TABLE 6-1: ADDRESSING THE SERIAL PORT

DLAB*	A2	A1	A0	Register Name
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

Note: *DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

6.1.1 RECEIVE BUFFER REGISTER (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

6.1.2 TRANSMIT BUFFER REGISTER (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

TABLE 6-7: REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL (CONTINUED)

Register Address (Note 6-4)	Register Name	Register Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Note 6-4 DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 6-5 Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 6-6 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 6-7 This bit no longer has a pin associated with it.

Note 6-8 When operating in the XT mode, this register is not available.

Note 6-9 These bits are always zero in the non-FIFO mode.

Note 6-10 Writing a one to this bit has no effect. DMA modes are not supported in this chip.

Note 6-11 The UARTs FCR's are shadowed UART FIFO Control Shadow Registers. See Section 24.0, "Runtime Register" for more details.

TABLE 7-1: PARALLEL PORT CONNECTOR (CONTINUED)

Host Connector	Pin Number	Standard	EPP	ECP
15	81	nERROR	(User Defined)	nFault (1) nPeriphRequest (3)
16	66	nINIT	nRESET	nInit(1) nReverseRqst(3)
17	67	nSLCTIN	nAddrstrb	nSelectIn(1,3)
(1) = Compatible Mode (3) = High Speed Mode				

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the *IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14*, July 14, 1993. This document is available from Microsoft.

7.1 IBM XT/AT Compatible, Bi-Directional and EPP Modes

7.1.1 DATA PORT

ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the internal data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

7.1.2 STATUS PORT

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of a read cycle. The bits of the Status Port are defined as follows:

Bit 0 TMOUT - TIME OUT

This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic O means that no time out error has occurred; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. If the TIMEOUT_SELECT bit (bit 4 of the Parallel Port Mode Register 2, 0xF1 in Logical Device 3 Configuration Registers) is '0', writing a one to this bit clears the TMOUT status bit. Writing a zero to this bit has no effect. If the TIMEOUT_SELECT bit (bit 4 of the Parallel Port Mode Register 2, 0xF1 in Logical Device 3 Configuration Registers) is '1', the TMOUT bit is cleared on the trailing edge of a read of the EPP Status Register.

Bits 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

Bit 3 nERR – nERROR

The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

Bit 4 SLT - Printer Selected Status

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

Bit 5 PE - Paper End

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

Bit 6 nACK - Acknowledge

The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

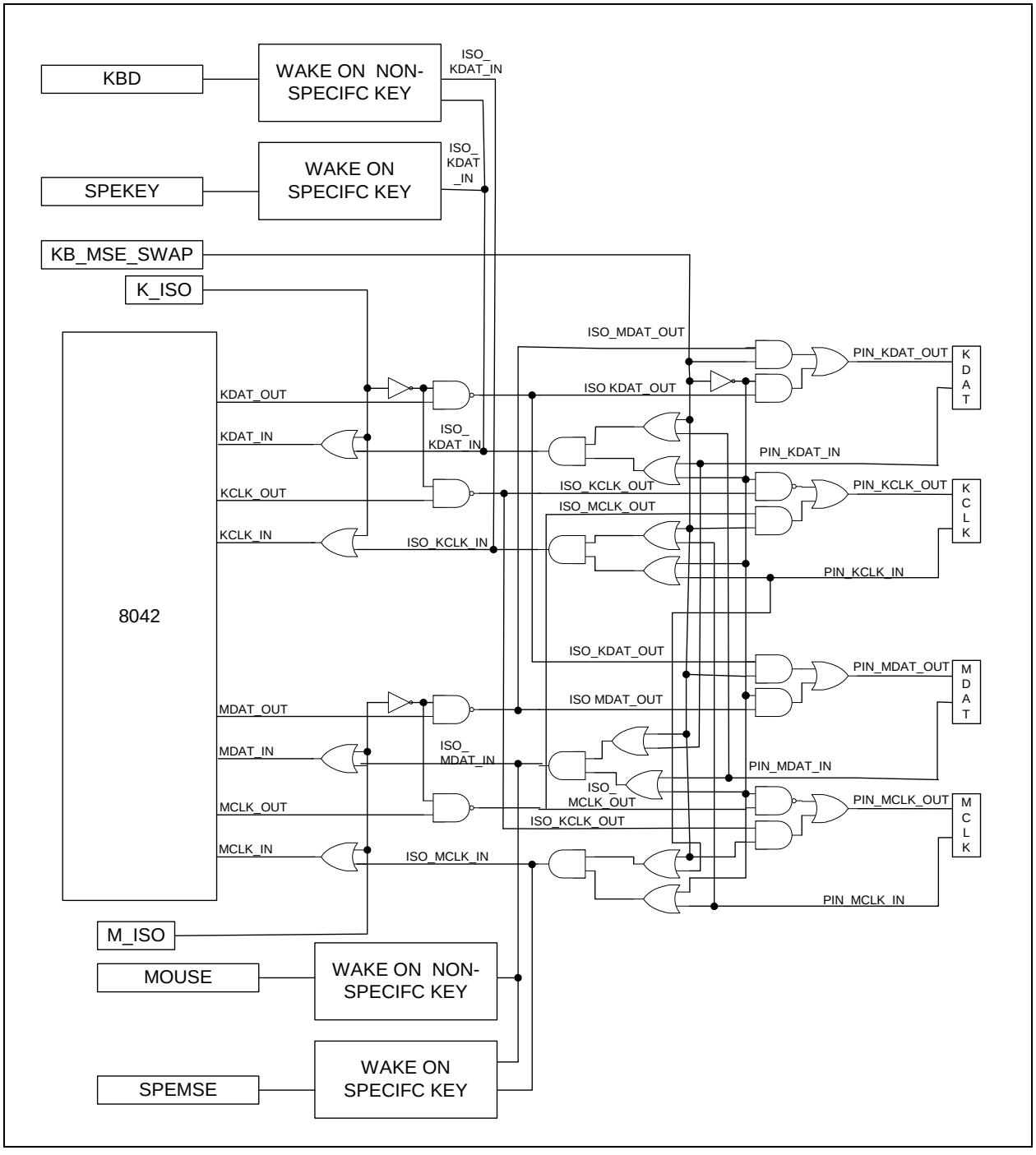
Bit 7 nBUSY - nBUSY

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

The LED pins can drive a LED when the buffer type is configured to be push-pull and the part is powered by either VCC or VTR, since the buffers for these pins are powered by VTR. This means they will source their specified current from VTR even when VCC is present.

The LED control registers are defined in Section 24.0, "Runtime Register," on page 213.

FIGURE 13-1: 8042 ISOLATION AND KEYBOARD AND MOUSE PORT SWAP REPRESENTATION



Note: This figure is for illustration purposes only and not meant to imply specific implementation details.

17.0 BUFFERED PCI OUTPUTS

17.1 Buffered PCI Outputs Interface

The SCH322x family devices provide three software controlled PCIRST# outputs and one buffered IDE Reset.

Table 17-1 describes the interface.

TABLE 17-1: BUFFERED PCI OUTPUTS INTERFACE

Name	Buffer	Power Well	Description
PCI_RESET#	PCI_I	VCC	PCI Reset Input
nIDE_RSTDRV	OD4	VCC	IDE Reset Output
nPCIRST1	O8/OD8	VCC	Buffered PCI Reset Output
nPCIRST2	O8/OD8	VCC	Buffered PCI Reset Output
nPCIRST3	O4/OD4	VCC	Buffered PCI Reset Output

17.1.1 IDE RESET OUTPUT

nIDE_RSTDRV is an open drain buffered copy of PCI_RESET#. This signal requires an external 1KΩ pull-up to VCC or 5V. This pin is an output only pin which floats when VCC=0. The pin function's default state on VTR POR is the nIDE_RST function; however the pin function can be programmed to the a GPO pin function by bit 2 in its GPIO control register.

The nIDE_RSTDRV output has a programmable forced reset. The software control of the programmable forced reset function is located in the GP4 GPIO Data register. When the GP44 bit (bit 4) is set, the nIDE_RSTDRV output follows the PCI_RESET# input; this is the default state on VTR POR. When the GP44 bit is cleared, the nIDE_RSTDRV output stays low.

See GP44 and GP4 for Runtime Register Description (Section 24.0, "Runtime Register," on page 213).

TABLE 17-2: NIDE_RSTDRV TRUTH TABLE

PCI_RESET# (Input)	nIDE_RSTDRV (Output)
0	0
1	Hi-Z

TABLE 17-3: NIDE_RSTDRV TIMING

Name	Description	MIN	TYP	MAX	Units
Tf	nIDE_RSTDRV high to low fall time. Measured form 90% to 10%			15	ns
Tpropf	nIDE_RSTDRV high to low propagation time. Measured from PCI_RESET# to nIDE_RSTDRV.			22	ns
CO	Output Capacitance			25	pF
CL	Load Capacitance			40	pF

17.1.2 NPCIRSTX OUTPUT LOGIC

The nPCIRST1, nPCIRST2, and nPCIRST3 outputs are 3.3V balance buffer push-pull buffered copies of PCI_RESET# input. Each pin function's default state on VTR POR is the nPCIRSTx function; however, the pin function can be programmed to the a GPO pin (output only) function by bit 2 in the corresponding GPIO control register (GP45, GP46, GP47).

Each nPCIRSTx output has a programmable force reset. The software control of the programmable forced reset function is located in the GP4 GPIO Data register. When the corresponding (GP45, GP46 GP47) bit in the GP4 GPIO Data register is set, the nPCIRSTx output follows the PCI_RESET# input; this is the default state on VTR POR. When the corresponding (GP45, GP46, GP47) bit in the GP4 GPIO Data register is cleared, the nPCIRSTx output stays low.

See GP4 for Runtime Register Description.

18.5.1 KEYBOARD DATA FORMAT

Data transmissions from the keyboard consist of an 11-bit serial data stream. A logic 1 is sent at an active high level. The following table shows the functions of the bits.

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

The process to find a match for the scan code stored in the Keyboard Scan Code register meets the timing constraints as defined by the IBM Personal System/2™ Model 50 and 60 Technical Reference, dated April 1987. The timing for the keyboard clock and data signals are shown in Section 27.0, "Timing Diagrams," on page 260. (See Section 27.8, "Keyboard/Mouse Interface Timing," on page 274).

18.5.1.1 Method for Receiving Data is as Follows

The wake on specific key logic snoops the keyboard interface for a particular incoming scan code, which is used to wake the system through a PME event. These scan codes may be comprised of a single byte or multiple bytes. To determine when the first key code is being received, the wake on specific key logic begins sampling the data at the first falling edge of the keyboard clock for the start bit. The data is sampled on each falling edge of the clock. The hardware decodes the byte received and determines if it is valid (i.e., no parity error). Valid scan code bytes received are compared to the programmed scan code as determined by bits [3:2] SPEKEY Scan Code Runtime register located at offset 0x64. If the scan code(s) received matches the value(s) programmed in the Keyboard Scan Code registers then a wake on specific key status event has occurred. The wake on specific key status event is mapped to the PME and Power Button logic.

The snooping logic always checks the incoming data byte for a parity error. The hardware samples the parity bit and checks that the 8 data bits plus the parity bit always have an odd number of 1's (odd parity). If a parity error is detected the state machine used to decode the incoming scan code is reset and begins looking for the first byte in the keyboard scan code sequence.

This process is repeated until a match is found. See Section 18.5.2, "System for Decoding Scan Code Make Bytes Received from the Keyboard," on page 114 and Section 18.5.3, "System for Decoding Scan Code Break Bytes Received from the Keyboard," on page 115.

If the scan code received matches the programmed make code stored in the Keyboard Scan Code registers and no parity error is detected, then it is considered a match. When a match is found and if the stop bit is 1, a PME wake event (KB_PB_STS-See Figure 18-1) will be generated within 100usec of the falling edge of clock 10 of the last byte of the sequence. This wake event may be used to generate the assertion of the nIO_PME signal when in SX power state or below.

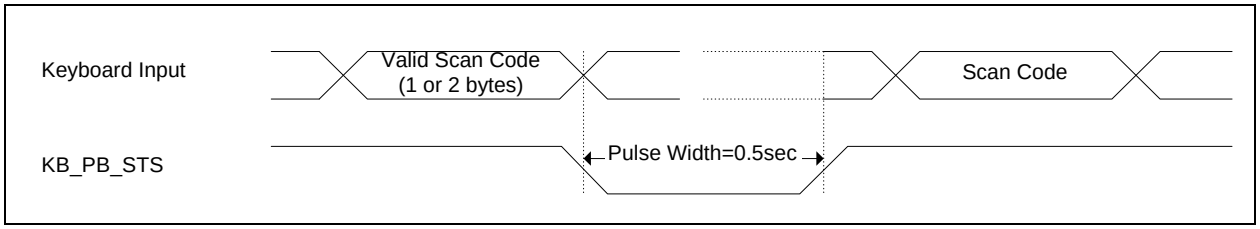
The state machine will reset and repeat the process until it is shut off by setting the SPEKEY_EN bit to '1'.

The SPEKEY_EN bit at bit 1 of the register at 0xF0 in Logical Device A is used to control the "wake-on-specific feature. This bit is used to turn the logic for this feature on and off. It will disable the 32kHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:

0= "Wake on specific key" logic is on (default)

1= "Wake on specific key" logic is off

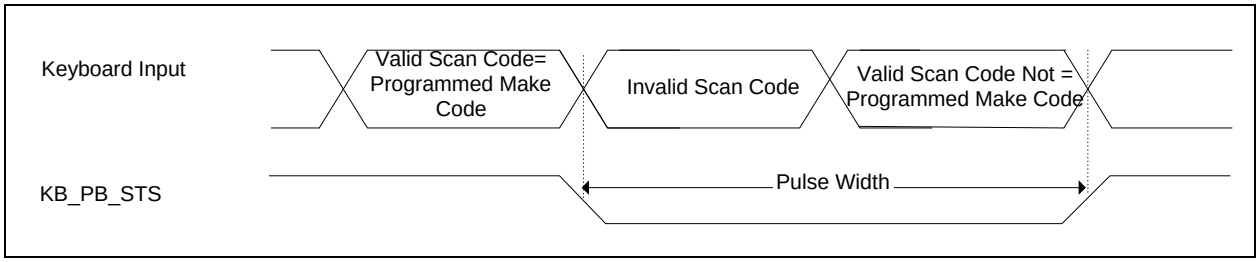
FIGURE 18-8: OPTION 1: KB_PB_STS WAKE EVENT FIXED PULSE WIDTH



Option 2 (01): De-assert KB_PB_STS after Scan Code Not Equal Programmed Make Code

This option may be used by keyboards that emit single byte or multi-byte make codes for each key pressed. When a valid Scan Code is received that matches the value programmed in the Keyboard Scan Code – Make Byte Register(s), the KB_PB_STS wake event signal will be held asserted low until another valid Scan Code is received that is not equal to the programmed make code. Regardless of the state of the SPEKEY bits, no additional wake events will no additional wake events will occur until another valid Scan Code is received that is not equal to the programmed make code.

FIGURE 18-9: Option 2: Assert KB_PB_STS Wake Event Until Scan Code Not Programmed Make Code



Note 1: The Valid Scan Code may be 1 or 2 bytes depending on the SPEKEY ScanCode bits in the Runtime register at offset 64h.

2: A Valid Scan Code for single byte codes means that no parity error exists. A Valid Scan Code for Multi-byte Scan Codes requires that no parity error exists and that the first Byte received matches the value programmed in the Keyboard Scan Code – Make Byte 1 located in the Runtime Register block at offset 5Fh. This value is typically E0h for Scan 1 and Scan 2 type keyboards. (Example: The ACPI power scan 2 make code is E0h, 37h) Section 18.5.1.2, "Description Of SCAN 1 and SCAN 2," on page 114.

Option 3 (10): De-assert KB_PB_STS after Scan Code Equal Break Code

This option may be used with single byte and multi-byte scan 1 and scan 2 type keyboards. The break code can be configured for a specific break code or for any valid break code.

the KB_PB_STS wake event signal will be held asserted low until a valid break code is detected. The break code can be configured for a specific break code or for any valid break code. Regardless of the state of the SPEKEY bits, no additional wake events will occur until another until a valid break code is detected.

Note: Table 18-5 defines how the scan code will be decoded for the Break Code. Once a valid break code is detected, the keyboard power button event will be de-asserted as shown in Figure 18-10.

duty cycle will be held constant for a minimum of 18 periods (206/11.4 = 18.07) until the Ramp Logic increments/decrements the actual PWM duty cycle by '1'.

- If the period of the PWM output is greater than the step size created by the PWM Ramp Rate, the ramp rate logic will force the PWM output to increment/decrement the actual duty cycle in increments larger than 1/255. For example, if the PWM frequency is 11Hz (1/11Hz = 90.9msec) and the PWM Step time is 5msec, the PWM duty cycle output will be incremented 18 or 19 out of 255 (i.e., 90.9/5 = 18.18) until it reaches the calculated duty cycle. Note that the step size may be less if the calculated duty cycle minus the actual duty cycle is less than 18.

Note: The calculated PWM Duty cycle reacts immediately to a change in the temperature reading value. The temperature reading value may be updated once in 105.8msec (default) (see Table 21-2, "ADC Conversion Sequence," on page 126). The internal PWM duty cycle generated by the Ramp Rate control logic gradually ramps up/down to the calculated duty cycle at a rate pre-determined by the value programmed in the PWM Ramp Rate Control bits. The PWM output latches the internal duty cycle generated by the Ramp Rate Control Block every 1/(PWM frequency) seconds to determine the actual duty cycle of the PWM output pin.

PWM Output Transition from OFF to ON

When the calculated PWM Duty cycle generated by the auto fan control logic transitions from the 'OFF' state to the 'ON' state (i.e., Current PWM duty cycle>00h), the internal PWM duty cycle in the Ramp Rate Control Logic is initialized to the calculated duty cycle without any ramp time and the PWMx Current Duty Cycle register is set to this value. The PWM output will latch the current duty cycle value in the Ramp Rate Control block to control the PWM output.

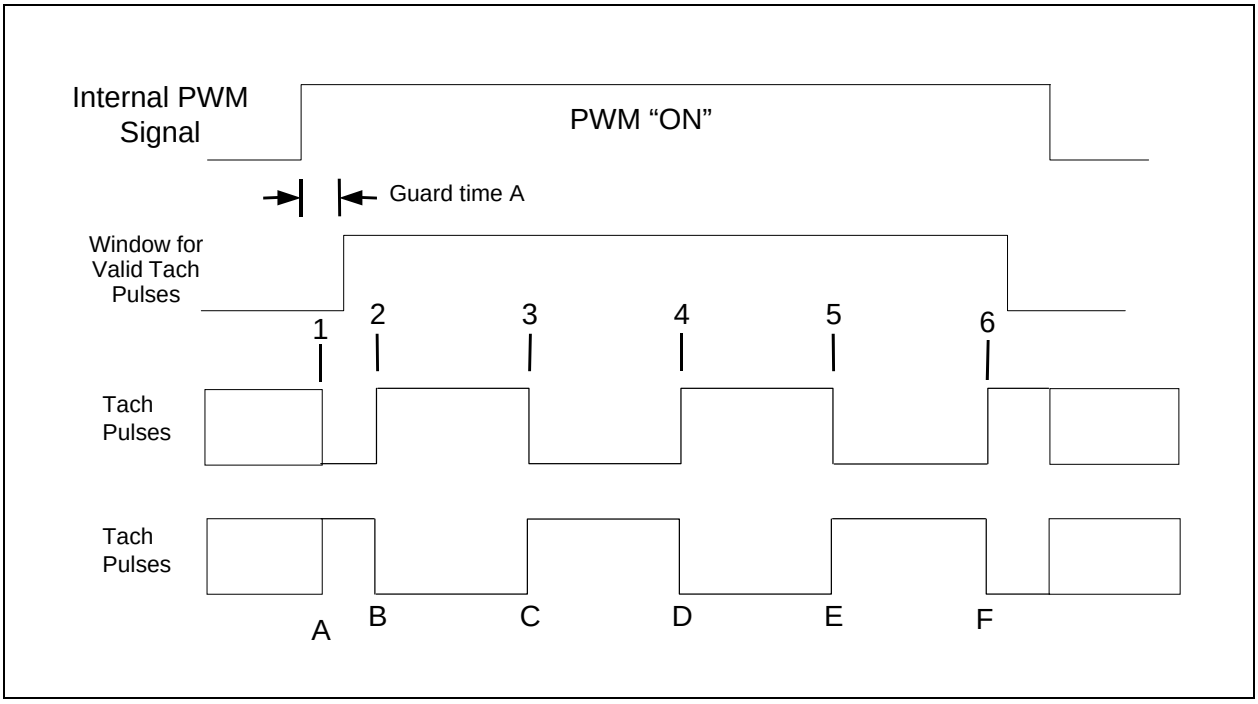
PWM Output Transition from ON to OFF

Each PWM output has a control bit to determine if the PWM output will transition immediately to the OFF state (default) or if it will gradually step down to Off at the programmed Ramp Rate. These control bits (SZEN) are located in the PWMx Options registers at offsets 94h-96h.

TABLE 21-4: PWM RAMP RATE

RRx-[2:0]	PWM Ramp Time (sec) (Time from 33% Duty Cycle to 100% Duty Cycle)	PWM Ramp Time (sec) (Time from 0% Duty Cycle to 100% Duty Cycle)	Time per PWM Step (PWM Step Size = 1/255)	PWM Ramp Rate (Hz)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

FIGURE 21-16: PWM AND TACHOMETER CONCEPT



21.14.2.5.1 Fan Tachometer Options for Mode 2

- 2, 3, 5 or 9 “edges” to calculate the fan speed (Figure 21-16)
- Guard time A is programmable (8-63 clocks) to account for delays in the system (Figure 21-16)
- Suggested PWM frequencies for mode 2 are: 11.0 Hz, 14.6 Hz, 21.9 Hz, 29.3 Hz, 35.2 Hz, 44.0 Hz, 58.6 Hz, 87.7Hz
- Option to ignore first 3 tachometer edges after guard time
- Option to force tach reading register to FFFEh to indicate a slow fan.

21.14.2.6 Fan Tachometer Reading Registers:

The Tachometer Reading registers are 16 bits, unsigned. When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second. The value FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (this could be triggered by a counter overflow). These registers are read only – a write to these registers has no effect.

Note 1: The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional.

2: FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

3: The Tachometer registers are read only – a write to these registers has no effect.

4: Mode 1 should be enabled and the tachometer limit register should be set to FFFFh if a tachometer input is left unconnected.

21.14.2.7 Programming Options for Each Tachometer Input

The features defined in this section are programmable via the TACHx Option registers located at offsets 90h-92h and the PWMx Option registers located at offsets 94h-96h.

21.14.2.7.1 Tach Reading Update Time

In Mode 1, the Fan Tachometer Reading registers are continuously updated. In Mode 2, the fan tachometer registers are updated every 300ms, 500msec, or 1000msec. This option is programmed via bits[1:0] in the PWMx Option register. The PWM associated with a particular TACH(s) determines the TACH update time.

21.14.2.7.2 Programmed Number Of Tach Edges

In modes 1 & 2, the number of edges is programmable for 2, 3, 5 or 9 edges (i.e., ½ tachometer pulse, 1 tachometer pulse, 2 tachometer pulses, 4 tachometer pulses). This option is programmed via bits[2:1] in the TachX Option register.

Note:	The “5 edges” case corresponds to two tachometer pulses, or 1 RPM for most fans. Using the other edge options will require software to scale the values in the reading register to correspond to the count for 1 RPM.

21.14.2.7.3 Guard Time (Mode 2 Only)

The guard time is programmable from 8 to 63 clocks (90kHz). This option is programmed via bits[4:3] in the TachX Option register.

21.14.2.7.4 Ignore first 3 tachometer edges (Mode 2 Only)

Option to ignore first 3 tachometer edges after guard time. This option is programmed for each tachometer via bits[2:0] in the TACHx Option register. Default is do not ignore first 3 tachometer edges after guard time.

21.14.2.8 Summary of Operation for Modes 1 & 2

The following summarizes the detection cases:

- **No edge occurs during the PWM ‘ON’ time:** indicate this condition as a stalled fan
  - The tachometer reading register contains FFFFh.
- **One edge (or less than programmed number of edges) occurs during the PWM ‘ON’ time:** indicate this condition as a slow fan.
  - If the SLOW bit is enabled, the tachometer reading register will be set to FFFEh to indicate that this is a slow fan instead of a seized fan. Note that this operation also pertains to the case where the tachometer counter reaches FFFFh before the programmed number of edges occurs.
  - If the SLOW bit is disabled, the tachometer reading register will be set to FFFFh. In this case, no distinction is made between a slow or seized fan.

Note:	The Slow Interrupt Enable feature (SLOW) is configured in the TACHx Options registers at offsets 90h to 93h.

- The programmed number of edges occurs:
  - Mode 1: If the programmed number of edges occurs before the counter reaches FFFFh latch the tachometer count
  - Mode 2: If the programmed number of edges occurs during the PWM ‘ON’ time: latch the tachometer count (see **Note** below).

Note 1: Whenever the programmed number of edges is detected, the edge detection ends and the state machine is reset. The tachometer reading register is updated with the tachometer count value at this time. See Detection of a Stalled Fan on page 154 for the exception to this behavior.

2: In the case where the programmed number of edges occurs during the “on”, the tachometer value is latched when the last required edge is detected.

TABLE 22-1: REGISTER SUMMARY (CONTINUED)

Reg Addr	Read/ Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock	
9Ch	R/W	VTR Limit Hi		7	6	5	4	3	2	1	0	FFh	No	
9Dh	R/W	VBAT Limit Low										00h	No	
9Eh	R/W	VBAT Limit Hi		7	6	5	4	3	2	1	0	FFh	No	
9Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A0h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A1h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A2h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A3h	R/W	MCHP Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h N/A	Yes	
A4h	R	MCHP Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	02h	No	
A5h	R/WC	Interrupt Status 1 Secondary		INT23	D2	AMB	D1	5V	VCC	Vccp	2.5V	00h Note 22-8	No	
A6h	R/WC	Interrupt Status 2 Secondary		ERR2	ERR1	RES	FAN-TACH3	FAN-TACH2	FAN-TACH1	RES	12V	00h Note 22-8	No	
A7h	RWC	Interrupt Status 3 Secondary	INS3	RES	RES	RES	RES	RES	RES	VBAT	VTR	00h	No	
A8h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
A9h	R/W	MCHP Test Register		7	6	5	4	3	2	1	0	00h	Yes	
AAh	R/W	MCHP Test Register		7	6	5	4	3	2	1	0	00h	Yes	
ABh	R/W	Tach 1-3 Mode		T1M1	T1M0	T2M1	T2M0	T3M1	T3M0	RES	RES	00h	No	
ACh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
ADh	R	MCHP Test Register		7	6	5	4	3	2	1	0	00h	No	
AEh	R/W	Top Temperature Remote Diode 1 (Zone 1)		7	6	5	4	3	2	1	0	2Dh Note 22-8	Yes	
AFh	R/W	Top Temperature Remote Diode 2 (Zone 3)		7	6	5	4	3	2	1	0	2Dh Note 22-8	Yes	
B0h	R	MCHP Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
B1h	R	MCHP Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
B2h	R	MCHP Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
B3h	R/W	Top Temperature Ambient (Zone 2)		7	6	5	4	3	2	1	0	2Dh Note 22-8	Yes	
B4h	R/W	Min Temp Adjust Temp RD1, RD2		R1ATP1	R1ATP0	R2ATP1	R2ATP0	RES	RES	RES	RES	00h	Yes	
B5h	R/W	Min Temp Adjust Temp and Delay Amb		RES	RES	AMATP1	AMATP0	RES	RES	AMAD1	AMAD0	00h	Yes	
B6h	R/W	Min Temp Adjust Delay 1-2		R1AD1	R1AD0	R2AD1	R2AD0	RES	RES	RES	RES	00h	Yes	
B7h	R/W	Tmin Adjust Enable		RES	RES	RES	RES	TMIN_ADJ_EN2	TMIN_ADJ_EN1	TMIN_ADJ_ENA	TOP_INT_EN	00h	Yes	
B8h	R/WC	Top Temp Exceeded Status		RES	RES	RES	RES	RES	STS2	STS1	STSA	00h Note 22-8	No	
B9h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
BAh	R/W	MCHP Reserved		RES	RES	RES	RES	RES	RES	RES	RES	04h	Yes	
BBh	R	MCHP Reserved		7	6	5	4	3	2	1	0	00h	No	
BCh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
BDh	R	MCHP Reserved		7	6	5	4	3	2	1	0	00h	No	
BEh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
BFh	R/W	MCHP Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	Yes	
C0h	R/W	MCHP Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	Yes	
C1h	R/W	Thermtrip Control		RES	RES	RES	RES	RES	RES	RES	THER-MTRIP_CTRL	01h	Yes	
C2h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
C3h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	
C4h	R/W	ThermTrip Temp Limit RD1 (Zone 1)		7	6	5	4	3	2	1	0	7Fh	Yes	
C5h	R/W	ThermTrip Temp Limit RD2 (Zone 3)		7	6	5	4	3	2	1	0	7Fh	Yes	
C6h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No	

Note 1: SOFT RESET: Bit 0 of Configuration Control register set to one.

2: All host accesses are blocked for 500µs after Vcc POR (See FIGURE 27-1: Power-Up Timing on page 260.)

23.1 Configuration Registers

CAUTION: This device contains circuits which must not be used because their pins are not brought out of the package, and are pulled to known states internally. Any features, and especially Logical Devices, that are not listed in this document must not be activated or accessed. Doing so may cause unpredictable behavior and/or excessive currents, and therefore may damage the device and/or the system.

The following table summarizes the logical device allocation for the different varieties of SCH322x devices.

TABLE 23-2: SCH322X LOGICAL DEVICE SUMMARY

Logical Device	SCH3222	SCH3224	SCH3226	SCH3227
0	RESERVED	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED	RESERVED
2	RESERVED	RESERVED	RESERVED	RESERVED
3	RESERVED	PARALLEL PORT	RESERVED	PARALLEL PORT
4	SERIAL PORT 1	SERIAL PORT 1	SERIAL PORT 1	SERIAL PORT 1
5	SERIAL PORT 2	SERIAL PORT 2	SERIAL PORT 2	SERIAL PORT 2
6	RESERVED	RESERVED	RESERVED	RESERVED
7	KEYBOARD	KEYBOARD	KEYBOARD	KEYBOARD
8	RESERVED	RESERVED	RESERVED	RESERVED
9	RESERVED	RESERVED	RESERVED	RESERVED
Ah	RUNTIME REGISTERS	RUNTIME REGISTERS	RUNTIME REGISTERS	RUNTIME REGISTERS
Bh	SERIAL PORT 3	RESERVED	SERIAL PORT 3	SERIAL PORT 3
Ch	SERIAL PORT 4	RESERVED	SERIAL PORT 4	SERIAL PORT 4
Dh	SERIAL PORT 5	SERIAL PORT 5	IF STRAPOPT=1 SERIAL PORTS [5/6] ELSE RESERVED	IF STRAPOPT=1 SERIAL PORTS [5/6] ELSE RESERVED
Eh	SERIAL PORT 6	SERIAL PORT 6		
Fh	RESERVED	RESERVED	RESERVED	RESERVED

TABLE 23-3: CONFIGURATION REGISTER SUMMARY

Index	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Configuration Register
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x7D or 0x7F	0x7D or 0x7F	0x7D or 0x7F	0x7D or 0x7F	Device ID - hard wired SCH3222 - 0x7F SCH3224 - 0x7F SCH3226 - 0x7D or 0x7F SCH3227 - 0x7D or 0x7F STRAPOPT pin selects value for SCH3226 and SCH3227. See this register in Table 23-4.
0x19	R/W	-	0x00	0x00	-	TEST8
0x21	R	Current Revision				Device Rev - hard wired

TABLE 23-4: CHIP-LEVEL (GLOBAL) CONFIGURATION REGISTERS (CONTINUED)

Register	Address	Description
Configuration Address Byte 0 Default Sysopt0 = 0 0x2E Sysopt0 = 1 0x4E on VCC POR and PCI RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 (Note 23-3)
Configuration Address Byte 1 Default Sysopt1 = 0 0x16 Sysopt1 = 1 0x00 n VCC POR and PCI RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] Bits[15:21] = 0 (Note 23-3)
Default = 0x00 on VCC POR, SOFT RESET and PCI RESET	0x28	Bits[7:0] Reserved - Writes are ignored, reads return 0.

Note 23-3 To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a PCI Reset or Vcc POR.

Note: The default configuration address is specified in Table 23-1, “SYSOPT Strap Option Configuration Address Select,” on page 194.

23.1.2 TEST REGISTERS

The following test registers are used in the SCH322x devices.

TABLE 23-5: TEST REGISTER SUMMARY

Register	Address	Description
TEST 8 Default = 0x00, on VCC POR and VTR POR	0x19 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 9 Default = 0x00, on VCC POR and VTR POR	0x25 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST Default = 0x00 Note on VTR_POR BIT0/7 are reset BIT1-6 reset on TST_PORB from resgen block	0x29 R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for MCHP. Users should not write to this register, may produce undesired results.

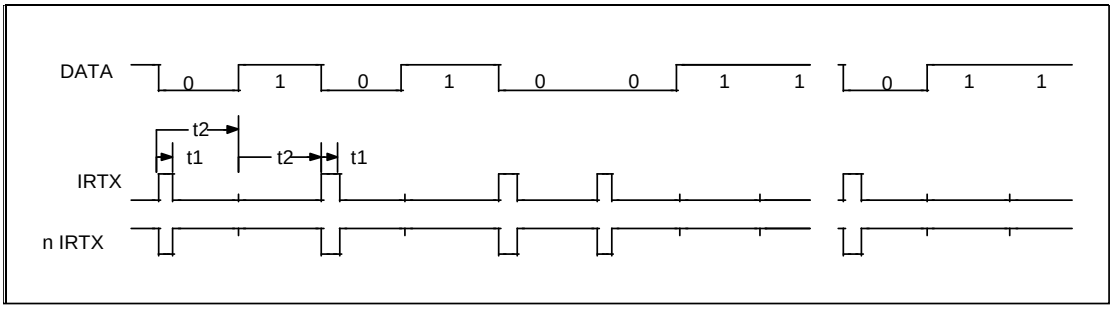
TABLE 24-2: RUNTIME REGISTER POR SUMMARY (CONTINUED)

Register Offset (HEX)	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Vbat POR	Register
36	R/W	-	-	0x84	-	-	GP33
37	R/W	-	-	0x01	-	-	GP34
38	R	-	-	-	-	-	Reserved
39	R/W	-	-	0x01	-	-	GP36
3A	R/W	-	-	0x01	-	-	GP37
3B	R/W	-	-	0x01	-	-	GP40
3C	R	-	-	0x00	-	-	CLK_OUT Register
3D	R/W	-	-	0x01	-	-	GP42
3E	R	-	-	-	-	-	Reserved – reads return 0
3F	R/W	-	-	0x01	-	-	GP50
40	R/W	-	-	0x01	-	-	GP51
41	R/W	-	-	0x01	-	-	GP52
42	R/W	-	-	0x01	-	-	GP53
43	R/W	-	-	0x01	-	-	GP54
44	R/W	-	-	0x01	-	-	GP55
45	R/W	-	-	0x01	-	-	GP56
46	R/W	-	-	0x01	-	-	GP57
47	R/W	-	-	0x01	-	-	GP60
48	R/W	-	-	0x01	-	-	GP61
49	Note 2 4-11	0xxxxxxxx b Note 24-12	-	0xxxxxx11 b Note 24-12	-	0x00000x xb Note 24-12	PWR_REC (SCH3227 or SCH3226, and STRAPOPT=0)
49	R	0xxxxxxxx b Note 24-12	-	0xxxxxx11 b Note 24-12	-	0x00000x xb Note 24-12	RESERVED (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)
4A	R	-	-	-	-	0x00	PS_ON Register (SCH3227 or SCH3226, and STRAPOPT=0)
4A	R	-	-	-	-	0x00	RESERVED (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)
4B	R/W	-	-	0x00	-	-	GP1
4C	R/W	-	-	0x00	-	-	GP2
4D	R/W	-	-	0x00	-	-	GP3
4E	R/W	-	-	0x00	-	-	GP4
4F	R/W	-	-	0x00	-	-	GP5
50	R/W	-	-	0x00	-	-	GP6
51	R	-	-	-	-	-	Reserved – reads return 0
52	R	-	-	-	-	-	Reserved – reads return 0
53	R/W	-	-	-	-	0x00	PS_ON# Previous State (SCH3227 or SCH3226, and STRAPOPT=0)
53	R	-	-	-	-	0x00	RESERVED (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)

TABLE 24-3: DETAILED RUNTIME REGISTER DESCRIPTION (CONTINUED)

Name	REG Offset (HEX)	Description
PME_EN7 Default = 0x00 on Vbat POR (SCH3222, SCH3224, or SCH3227 / SCH3226 with STRAPOPT=1)	10 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_EN bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] RI3 Bit[1] RI4 Bit[2] RI5 Bit[3] RI6 Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
SP12 Option Default = 0x44 on VTR POR	0x12 (R/W)	SP Options for SP1 and SP2 Bit[0] Automatic Direction Control Select SP1 1=FC on 0=FC off Bits[1] Signal select SP1 1=nRTS control 0=nDTR control Bits[2] Polarity SP1 0= Drive low when enabled 1= Drive 1 when enabled Bits[3] RESERVED Bit[4] Automatic Direction Control Select SP2 1=FC on 0=FC off Bits[5] Signal select SP2 1=nRTS control 0=nDTR control Bits[6] Polarity SP2 0= Drive low when enabled 1= Drive 1 when enabled Bits[7] RESERVED
SP34 Option Default = 0x44 on VTR POR (SCH3224)	0x13 (R/W)	Bits[7:0] RESERVED

FIGURE 27-20: IRDA TRANSMIT TIMING

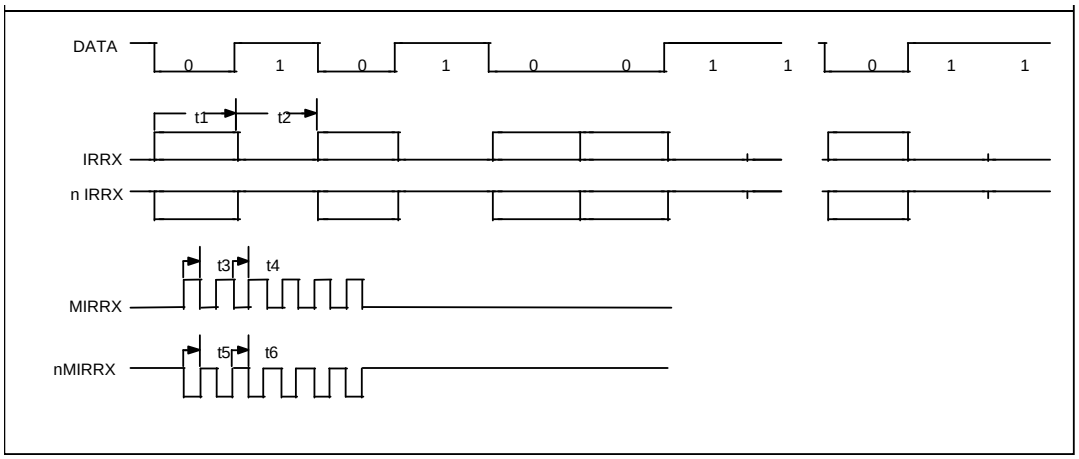


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

FIGURE 27-21: AMPLITUDE SHIFT-KEYED IR RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

APPENDIX D: DATA SHEET REVISION HISTORY

TABLE D-1: SCH3227/SCH3226/SCH3224/SCH3222 REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002121B (03-20-17)	Figure 2-2, "SCH3226 Pin Diagram" and Figure 2-3, "SCH3224 Pin Diagram"	Updated diagrams
	Table 2-2, "SCH3226 Summaries By Strap Option", Table 2-3, "SCH3224 Summary" and Table 2-4, "SCH3222 Summary"	Added footnote to pin TEST, indicating that a connection to VSS is necessary.
DS00002121A (03-02-16)	Document Release	