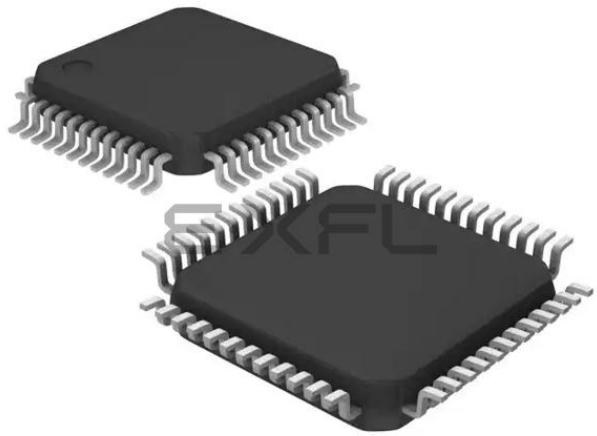

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128amlf

Chapter 28
96 KByte Flash Module (S12FTMRG96K1V1)

Table 1-23. 48-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
31	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
32	PAD11	KWAD11	AN11	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
33	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
34	PAD5	KWAD5	AN5	—	—	V_{DDA}	PER1AD/PPS0AD	Disabled
35	PAD6	KWAD6	AN6	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
36	PAD7	KWAD7	AN7	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
37	VDDA	VRH	—	—	—	—	—	—
38	VSSA	—	—	—	—	—	—	—
39	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
40	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
41	PS2	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
42	PS3	TXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
43	PS4	MISO0	—	—	—	V_{DDX}	PERS/PPSS	Up
44	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
45	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
46	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
47	PM0	RXD2	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
48	PM1	TXD2	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

2.3.11 Pins PJ7-0

Table 2-15. Port J Pins PJ7-0

PJ7	• 64/100 LQFP: The SPI2 $\overline{SS}$ signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: $\overline{SS2}$ > GPO
PJ6	• 64/100 LQFP: The SPI2 SCK signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: SCK2 > GPO
PJ5	• 64/100 LQFP: The SPI2 MOSI signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: MOSI2 > GPO
PJ4	• 64/100 LQFP: The SPI2 MISO signal is mapped to this pin when used with the SPI function.Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: MISO2 > GPO
PJ3	• Except 20 TSSOP and 32 LQFP: The SPI1 $\overline{SS}$ signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI1 the I/O state is forced to be input or output. • 48 LQFP: The PWM channel 7 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 20 TSSOP and 32 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 48 LQFP: $\overline{SS1}$ > PWM7 > GPO 64/100 LQFP: $\overline{SS1}$ > GPO
PJ2	• Except 20 TSSOP and 32 LQFP: The SPI1 SCK signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI1 the I/O state is forced to be input or output. • 48 LQFP: The TIM channel 7 signal is mapped to this pin when used with the TIM function. The TIM forces the I/O state to be an output for a timer port associated with an enabled output. • Except 20 TSSOP and 32 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 48 LQFP: SCK1 > IOC7 > GPO 64/100 LQFP: SCK1 > GPO

Table 2-19. Block Register Map (G1) (continued)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0246 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0247 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0248 PTS	R	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
	W								
0x0249 PTIS	R	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
	W								
0x024A DDRS	R	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
	W								
0x024B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x024C PERS	R	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
	W								
0x024D PPSS	R	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
	W								
0x024E WOMS	R	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
	W								
0x024F PRR0	R	PRR0P3	PRR0P2	PRR0T31	PRR0T30	PRR0T21	PRR0T20	PRR0S1	PRR0S0
	W								
0x0250 PTM	R	0	0	0	0	PTM3	PTM2	PTM1	PTM0
	W								
0x0251 PTIM	R	0	0	0	0	PTIM3	PTIM2	PTIM1	PTIM0
	W								
0x0252 DDRM	R	0	0	0	0	DDRM3	DDRM2	DDRM1	DDRM0
	W								
0x0253 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0254 PERM	R	0	0	0	0	PERM3	PERM2	PERM1	PERM0
	W								

= Unimplemented or Reserved

Table 2-76. PT1AD Register Field Descriptions

Field	Description
7-0 PT1AD	**Port AD general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read if the digital input buffers are enabled (Section 2.3.12, “Pins AD15-0”).

2.4.3.51 Port AD Input Register (PTI0AD)

Address 0x0272 (G1, G2) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTI0AD7	PTI0AD6	PTI0AD5	PTI0AD4	PTI0AD3	PTI0AD2	PTI0AD1	PTI0AD0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0272 (G3) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTI0AD3	PTI0AD2	PTI0AD1	PTI0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-51. Port AD Input Register (PTI0AD)

[1] Read: Anytime
Write: Never

Table 2-77. PTI0AD Register Field Descriptions

Field	Description
7-0 PTI0AD	**Port AD input data**— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.52 Port AD Input Register (PTI1AD)

Address 0x0273 Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTI1AD7	PTI1AD6	PTI1AD5	PTI1AD4	PTI1AD3	PTI1AD2	PTI1AD1	PTI1AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-52. Port AD Input Register (PTI1AD)

[1] Read: Anytime
Write: Never

4.7 Functional Description

The RVA is a prescaler for the ADC reference voltage. If the attenuation is turned off the resistive divider is disconnected from VSSA, VRH_INT is connected to VRH and VRL_INT is connected to VSSA. In this mode the attenuation is bypassed and the resistive divider does not draw current.

If the attenuation is turned on the resistive divider is connected to VSSA, VRH_INT and VRL_INT are connected to intermediate voltage levels:

$$VRH\_INT = 0.9 * (VRH - VSSA) + VSSA \qquad \textit{Eqn. 4-1}$$

$$VRL\_INT = 0.4 * (VRH - VSSA) + VSSA \qquad \textit{Eqn. 4-2}$$

The attenuated reference voltage difference (VRH_INT - VRL_INT) equals 50% of the input reference voltage difference (VRH - VSSA). With reference voltage attenuation the resolution of the ADC is improved by a factor of 2.

NOTE

In attenuation mode the maximum ADC clock is reduced. Please refer to the conditions in appendix A “ATD Accuracy”, table “ATD Conversion Performance 5V range, RVA enabled”.

Table 10-2. Reference Clock Frequency Selection if OSC_LCP is enabled

REFCLK Frequency Ranges (OSCE=1)	REFFRQ[1:0]
1MHz <= f_{REF} <= 2MHz	00
2MHz < f_{REF} <= 6MHz	01
6MHz < f_{REF} <= 12MHz	10
f_{REF} >12MHz	11

10.3.2.3 S12CPMU Post Divider Register (CPMUPOSTDIV)

The POSTDIV register controls the frequency ratio between the VCOCLK and the PLLCLK.

0x0036

	7	6	5	4	3	2	1	0
R	0	0	0	POSTDIV[4:0]				
W								
Reset	0	0	0	0	0	0	1	1

= Unimplemented or Reserved

Figure 10-6. S12CPMU Post Divider Register (CPMUPOSTDIV)

Read: Anytime

Write: Anytime if PLLSEL=1. Else write has no effect.

If PLL is locked (LOCK=1) $$f_{PLL} = \frac{f_{VCO}}{(POSTDIV + 1)}$$

If PLL is not locked (LOCK=0) $$f_{PLL} = \frac{f_{VCO}}{4}$$

If PLL is selected (PLLSEL=1) $$f_{bus} = \frac{f_{PLL}}{2}$$

10.3.2.4 S12CPMU Flags Register (CPMUFLG)

This register provides S12CPMU status bits and flags.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit (see also Table 10-6).
In Stop Mode with PSTP=1 (Pseudo Stop Mode), COPOSCSEL0=1 and COPOSCEL1=0 and PCE=1 the COP continues to run, else the COP counter halts in Stop Mode with COPOSCSEL1 =0.
In Full Stop Mode and Pseudo Stop Mode with COPOSCSEL1=1 the COP continues to run.

0x003C

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W			WRTMASK					
Reset	F	0	0	0	0	F	F	F

After de-assert of System Reset the values are automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 10-12. S12CPMU COP Control Register (CPMUCOP)

Read: Anytime

Write:

1. RSBCK: Anytime in Special Mode; write to “1” but not to “0” in Normal Mode
2. WCOP, CR2, CR1, CR0:
   - Anytime in Special Mode, when WRTMASK is 0, otherwise it has no effect
   - Write once in Normal Mode, when WRTMASK is 0, otherwise it has no effect.
     - Writing CR[2:0] to “000” has no effect, but counts for the “write once” condition.
     - Writing WCOP to “0” has no effect, but counts for the “write once” condition.

When a non-zero value is loaded from Flash to CR[2:0] the COP time-out period is started.

A change of the COPOSCSEL0 or COPSOCSEL1 bit (writing a different value) or loosing UPOSC status while COPOSCSEL1 is clear and COPOSCSEL0 is set, re-starts the COP time-out period.

In Normal Mode the COP time-out period is restarted if either of these conditions is true:

1. Writing a non-zero value to CR[2:0] (anytime in Special Mode, once in Normal Mode) with WRTMASK = 0.
2. Writing WCOP bit (anytime in Special Mode, once in Normal Mode) with WRTMASK = 0.
3. Changing RSBCK bit from “0” to “1”.

In Special Mode, any write access to CPMUCOP register restarts the COP time-out period.

13.3.2.7 ATD Status Register 0 (ATDSTAT0)

This register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-9. ATD Status Register 0 (ATDSTAT0)

Read: Anytime

Write: Anytime (No effect on (CC3, CC2, CC1, CC0))

Table 13-16. ATDSTAT0 Field Descriptions

Field	Description
7 SCF	**Sequence Complete Flag** — This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the following occurs: A) Write “1” to SCF B) Write to ATDCTL5 (a new conversion sequence is started) C) If AFFC=1 and a result register is read 0 Conversion sequence not completed 1 Conversion sequence has completed
5 ETORF	**External Trigger Overrun Flag** — While in edge sensitive mode (ETRIGLE=0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs: A) Write “1” to ETORF B) Write to ATDCTL0,1,2,3,4, ATDCMPE or ATDCMPHT (a conversion sequence is aborted) C) Write to ATDCTL5 (a new conversion sequence is started) 0 No External trigger overrun error has occurred 1 External trigger overrun error has occurred
4 FIFOR	**Result Register Overrun Flag** — This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been overwritten before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs: A) Write “1” to FIFOR B) Write to ATDCTL0,1,2,3,4, ATDCMPE or ATDCMPHT (a conversion sequence is aborted) C) Write to ATDCTL5 (a new conversion sequence is started) 0 No overrun has occurred 1 Overrun condition exists (result register has been written while associated CCFx flag was still set)

16.3.2 Register Descriptions

This section describes in address order all the ADC12B16C registers and their individual bits.

16.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 16-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 16-1. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 16-2.

Table 16-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved[1]
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

Table 18-24. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 18-23. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

[1] Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-25. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

18.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 18.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

18.3.3.3 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.

Module Base + 0x00XC

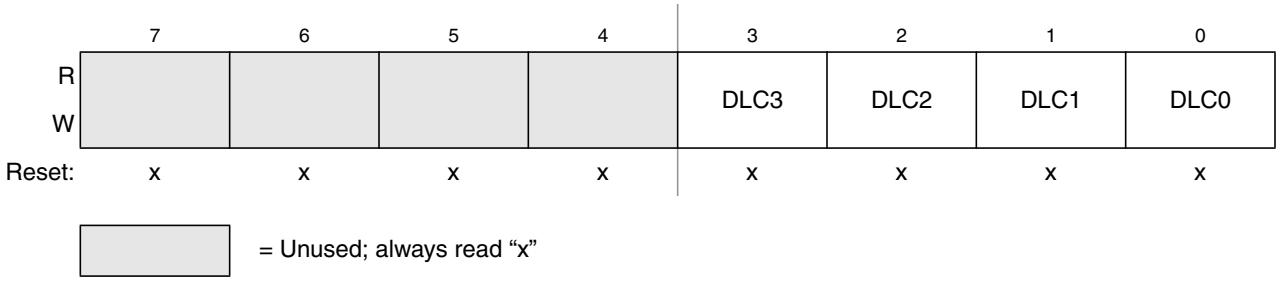

Figure 18-35. Data Length Register (DLR) — Extended Identifier Mapping

Table 18-34. DLR Register Field Descriptions

Field	Description
3-0 DLC[3:0]	**Data Length Code Bits** — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 18-35 shows the effect of setting the DLC bits.

Table 18-35. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

18.3.3.4 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.

20.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

20.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

20.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

During the reset sequence, fields DPOPEN and DPS of the EEPROT register are loaded with the contents of the EEPROM protection byte in the Flash configuration field at global address 0x3_FF0D located in P-Flash memory (see Table 25-4) as indicated by reset condition F in Table 25-23. To change the EEPROM protection that will be loaded during the reset sequence, the P-Flash sector containing the EEPROM protection byte must be unprotected, then the EEPROM protection byte must be programmed. If a double bit fault is detected while reading the P-Flash phrase containing the EEPROM protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the EEPROM memory fully protected.

Trying to alter data in any protected area in the EEPROM memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the EEPROM memory is not possible if any of the EEPROM sectors are protected.

Table 25-22. EEPROT Field Descriptions

Field	Description
7 DPOPEN	EEPROM Protection Control 0 Enables EEPROM memory protection from program and erase with protected address range defined by DPS bits 1 Disables EEPROM memory protection from program and erase
4–0 DPS[4:0]	**EEPROM Protection Size** — The DPS[4:0] bits determine the size of the protected area in the EEPROM memory as shown inTable 25-23 .

Table 25-23. EEPROM Protection Address Range

DPS[4:0]	Global Address Range	Protected Size
00000	0x0_0400 – 0x0_041F	32 bytes
00001	0x0_0400 – 0x0_043F	64 bytes
00010	0x0_0400 – 0x0_045F	96 bytes
00011	0x0_0400 – 0x0_047F	128 bytes
00100	0x0_0400 – 0x0_049F	160 bytes
00101	0x0_0400 – 0x0_04BF	192 bytes
The Protection Size goes on enlarging in step of 32 bytes, for each DPS value increasing of one. . . .		
11111 - to - 11111	0x0_0400 – 0x0_07FF	1,024 bytes

Table 26-6. Memory Controller Resource Fields (NVMRES[1]=1)

Global Address	Size (Bytes)	Description
0x0_4000 – 0x040FF	256	P-Flash IFR (see Table 26-5)
0x0_4100 – 0x0_41FF	256	Reserved.
0x0_4200 – 0x0_57FF		Reserved
0x0_5800 – 0x0_59FF	512	Reserved
0x0_5A00 – 0x0_5FFF	1,536	Reserved
0x0_6000 – 0x0_6BFF	3,072	Reserved
0x0_6C00 – 0x0_7FFF	5,120	Reserved

1 NVMRES - See Section 26.4.3 for NVMRES (NVM Resource) detail.

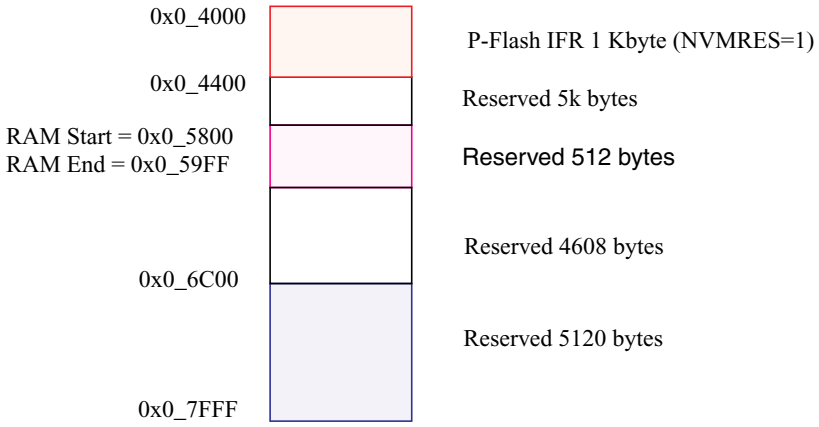

Figure 26-3. Memory Controller Resource Memory Map (NVMRES=1)

26.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013.

In the case of the writable registers, the write accesses are forbidden during Fash command execution (for more detail, see Caution note in Section 26.3).

- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

27.1.2.2 EEPROM Features

- 2 Kbytes of EEPROM memory composed of one 2 Kbyte Flash block divided into 512 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

27.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

27.1.3 Block Diagram

The block diagram of the Flash module is shown in Figure 27-1.

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 27-25. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

27.4 Functional Description

27.4.1 Modes of Operation

The FTMRG64K1 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers (see Table 27-27).

27.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in Table 27-26.

Table 27-26. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

indicated by reset condition F in Figure 30-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 30-9. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 30-10.
5–2 RNV[5:2]	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 30-11. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 30-10. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED[1]
10	ENABLED
11	DISABLED

1 Preferred KEYEN state to disable backdoor key access.

Table 30-11. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED[1]
10	UNSECURED
11	SECURED

1 Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 30.5.

30.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.

Offset Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CCOBIX[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

Table 30-12. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	**Common Command Register Index**— The CCOBIX bits are used to select which word of the FCCOB register array is being read or written to. See <st-blue>30.3.2.11 Flash Common Command Object Register (FCCOB),” for more details.

30.3.2.4 Flash Reserved0 Register (FRSV0)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-8. Flash Reserved0 Register (FRSV0)

All bits in the FRSV0 register read 0 and are not writable.

30.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU.

Offset Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-9. Flash Configuration Register (FCNFG)

CCIE, IGNSF, FDFD, and FSFD bits are readable and writable while remaining bits read 0 and are not writable.

31.4.4.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 31.3.2.3).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 31-26.