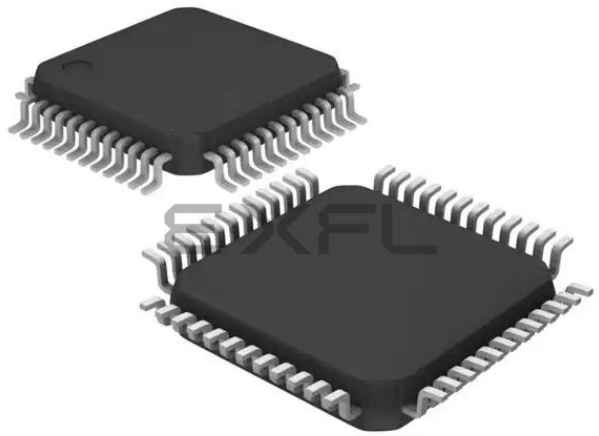

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Product Status	Active
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Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
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Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128amlfr

1.12.3 Effects of Reset

When a reset occurs, MCU registers and control bits are initialized. Refer to the respective block sections for register reset states.

On each reset, the Flash module executes a reset sequence to load Flash configuration registers.

1.12.3.1 Flash Configuration Reset Sequence Phase

On each reset, the Flash module holds CPU activity while loading Flash module registers from the Flash memory. If double faults are detected in the reset phase, Flash module protection and security may be active on leaving reset. This is explained in more detail in the Flash module Section 29.1, “Introduction”.

1.12.3.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

1.12.3.3 I/O Pins

Refer to the PIM section for reset configurations of all peripheral module ports.

1.12.3.4 RAM

The RAM arrays are not initialized out of reset.

1.13 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register at address 0x003C are loaded from the Flash register FOPT. See Table 1-36 and Table 1-37 for coding. The FOPT register is loaded from the Flash configuration field byte at global address 0x3_FF0E during the reset sequence.

Table 1-36. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in CPMUCOP Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

2.4.3.49 Port AD Data Register (PT0AD)

Address 0x0270 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PT0AD7	PT0AD6	PT0AD5	PT0AD4	PT0AD3	PT0AD2	PT0AD1	PT0AD0
Reset	0	0	0	0	0	0	0	0

Address 0x0270 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PT0AD3	PT0AD2	PT0AD1	PT0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-49. Port AD Data Register (PT0AD)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-75. PT0AD Register Field Descriptions

Field	Description
7-0 PT0AD	**Port AD general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read if the digital input buffers are enabled (Section 2.3.12, “Pins AD15-0”).

2.4.3.50 Port AD Data Register (PT1AD)

Address 0x0271 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PT1AD7	PT1AD6	PT1AD5	PT1AD4	PT1AD3	PT1AD2	PT1AD1	PT1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-50. Port AD Data Register (PT1AD)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 3-3. ACMPS Register Field Descriptions

Field	Description
7 ACIF	ACMP Interrupt Flag— ACIF is set when a compare event occurs. Compare events are defined by ACMOD[1:0]. Writing a logic “1” to the bit field clears the flag. 0 Compare event has not occurred 1 Compare event has occurred
6 ACO	ACMP Output— Reading ACO returns the current value of the synchronized ACMP output. Refer to ACE description to account for initialization delay on this path.

3.7 Functional Description

The ACMP compares two analog input voltages applied to ACMPM and ACMPP. The comparator output is high when the voltage at the non-inverting input is greater than the voltage at the inverting input, and is low when the non-inverting input voltage is lower than the inverting input voltage.

The ACMP is enabled with register bit ACMPC[ACE]. When ACMPC[ACE] is set, the input pins are connected to low-pass filters. The comparator output is disconnected from the subsequent logic, which is held at its state for 63 bus clock cycles after setting ACMPC[ACE] to “1” to mask potential glitches. This initialization delay must be accounted for before the first comparison result can be expected.

The initial hold state after reset is zero, thus if input voltages are set to result in “true” result ($V_{ACMPP} > V_{ACMPM}$) before the initialization delay has passed, a flag will be set immediately after this.

Similarly the flag will also be set when disabling the ACMP, then re-enabling it with the inputs changing to produce an opposite result to the hold state before the end of the initialization delay.

By setting the ACMPC[ACICE] bit the gated comparator output can be connected to the synchronized timer input capture channel 5 (see Figure 3-1). This feature can be used to generate time stamps and timer interrupts on ACMP events.

The comparator output signal synchronized to the bus clock is used to read the comparator output status (ACMPS[ACO]) and to set the interrupt flag (ACMPS[ACIF]).

The condition causing the interrupt flag (ACMPS[ACIF]) to assert is selected with register bits ACMPC[ACMOD1:ACMOD0]. This includes any edge configuration, that is rising, or falling, or rising and falling (toggle) edges of the comparator output. Also flag setting can be disabled.

An interrupt will be generated if the interrupt enable bit (ACMPC[ACIE]) and the interrupt flag (ACMPS[ACIF]) are both set. ACMPS[ACIF] is cleared by writing a 1.

The raw comparator output signal ACMPO can be driven out on an external pin by setting the ACMPC[ACOPE] bit.

11.1.3 Block Diagram

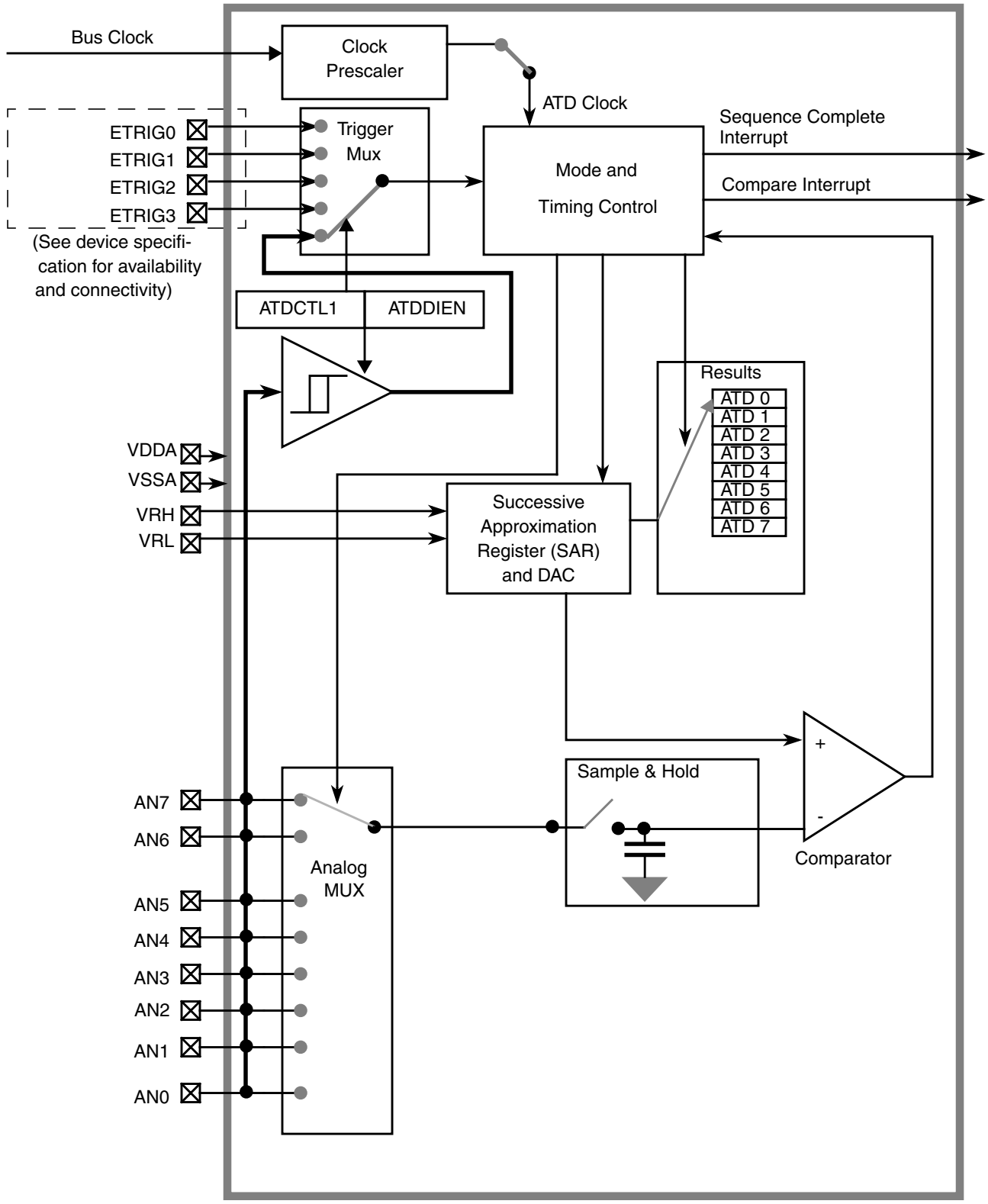

Figure 11-1. ADC10B8C Block Diagram

11.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1	1	1	1	1	1	1	1	IEN[7:0]							
W																
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-12. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 11-19. ATDDIEN Field Descriptions

Field	Description
7–0 IEN[7:0]	**ATD Digital Input Enable on channel *x* (*x*= 7, 6, 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (AN*x*) to the digital data register. 0 Disable digital input buffer to AN*x* pin 1 Enable digital input buffer on AN*x* pin. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

11.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	CMPHT[7:0]							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-13. ATD Compare Higher Than Register (ATDCMPHT)

Table 11-20. ATDCMPHT Field Descriptions

Field	Description
7–0 CMPHT[7:0]	**Compare Operation Higher Than Enable for conversion number *n* (*n*= 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — This bit selects the operator for comparison of conversion results. 0 If result of conversion *n* is **lower or same than** compare value in ATDDR*n*, this is flagged in ATDSTAT2 1 If result of conversion *n* is **higher than** compare value in ATDDR*n*, this is flagged in ATDSTAT2

12.4 Functional Description

The ADC12B8C consists of an analog sub-block and a digital sub-block.

12.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

12.4.1.1 Sample and Hold Machine

The Sample and Hold Machine controls the storage and charge of the sample capacitor to the voltage level of the analog signal at the selected ADC input channel.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.

During the hold process the analog input is disconnected from the storage node.

12.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 8 external analog input channels to the sample and hold machine.

12.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable to be either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages.

By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

When not converting the A/D machine is automatically powered down.

Only analog input signals within the potential range of VRL to VRH (A/D reference potentials) will result in a non-railed digital output code.

12.4.2 Digital Sub-Block

This subsection describes some of the digital features in more detail. See Section 12.3.2, “Register Descriptions” for all details.

12.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to an external event rather than relying only on software to trigger the ATD module when a conversion is about to take place. The external trigger signal (out of reset ATD channel 7, configurable in ATDCTL1) is programmable to be edge

Table 13-5. External Trigger Channel Select Coding

ETRIGSEL	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0	External trigger source is
0	0	0	0	0	AN0
0	0	0	0	1	AN1
0	0	0	1	0	AN2
0	0	0	1	1	AN3
0	0	1	0	0	AN4
0	0	1	0	1	AN5
0	0	1	1	0	AN6
0	0	1	1	1	AN7
0	1	0	0	0	AN8
0	1	0	0	1	AN9
0	1	0	1	0	AN10
0	1	0	1	1	AN11
0	1	1	0	0	AN11
0	1	1	0	1	AN11
0	1	1	1	0	AN11
0	1	1	1	1	AN11
1	0	0	0	0	ETRIG0[1]
1	0	0	0	1	ETRIG1[1]
1	0	0	1	0	ETRIG2[1]
1	0	0	1	1	ETRIG3[1]
1	0	1	X	X	Reserved
1	1	X	X	X	Reserved

[1] Only if ETRIG3-0 input option is available (see device specification), else ETRISEL is ignored, that means external trigger source is still on one of the AD channels selected by ETRIGCH3-0

13.3.2.3 ATD Control Register 2 (ATDCTL2)

Writes to this register will abort current conversion sequence.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-5. ATD Control Register 2 (ATDCTL2)

Read: Anytime

Write: Anytime

14.1.3 Block Diagram

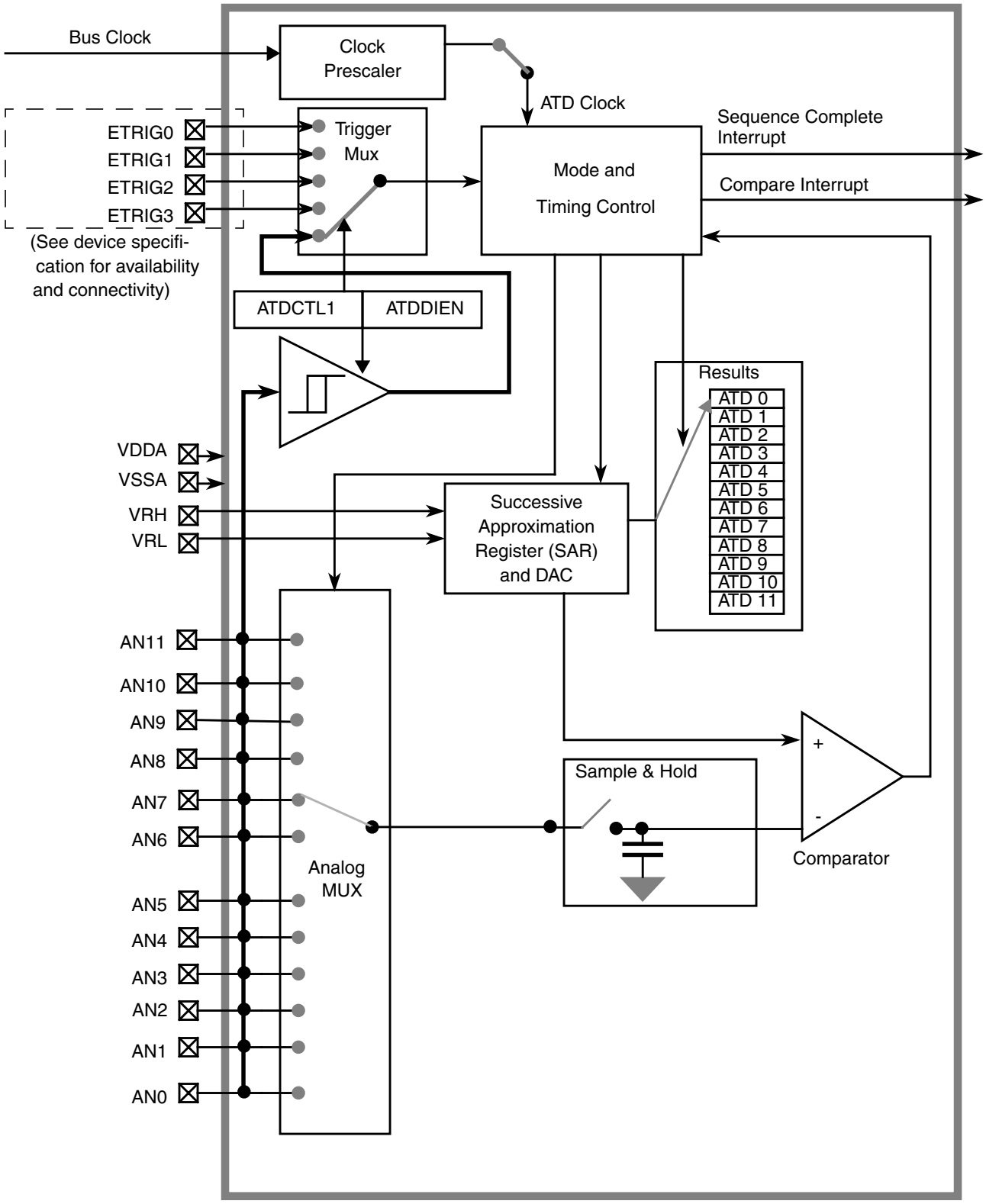

Figure 14-1. ADC12B12C Block Diagram

Table 18-24. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 18-23. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

[1] Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-25. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

18.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 18.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

18.4.5.7 Disabled Mode

The MSCAN is in disabled mode out of reset (CANE=0). All module clocks are stopped for power saving, however the register map can still be accessed as specified.

18.4.5.8 Programmable Wake-Up Function

The MSCAN can be programmed to wake up from sleep or power down mode as soon as CAN bus activity is detected (see control bit WUPE in MSCAN Control Register 0 (CANCTL0). The sensitivity to existing CAN bus action can be modified by applying a low-pass filter function to the RXCAN input line (see control bit WUPM in Section 18.3.2.2, "MSCAN Control Register 1 (CANCTL1)").

This feature can be used to protect the MSCAN from wake-up due to short glitches on the CAN bus lines. Such glitches can result from—for example—electromagnetic interference within noisy environments.

18.4.6 Reset Initialization

The reset state of each individual bit is listed in Section 18.3.2, "Register Descriptions," which details all the registers and their bit-fields.

18.4.7 Interrupts

This section describes all interrupts originated by the MSCAN. It documents the enable bits and generated flags. Each interrupt is listed and described separately.

18.4.7.1 Description of Interrupt Operation

The MSCAN supports four interrupt vectors (see Table 18-39), any of which can be individually masked (for details see Section 18.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)" to Section 18.3.2.8, "MSCAN Transmitter Interrupt Enable Register (CANTIER)").

Refer to the device overview section to determine the dedicated interrupt vector addresses.

Table 18-39. Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Wake-Up Interrupt (WUPIF)	I bit	CANRIER (WUPIE)
Error Interrupts Interrupt (CSCIF, OVRIF)	I bit	CANRIER (CSCIE, OVRIE)
Receive Interrupt (RXF)	I bit	CANRIER (RXFIE)
Transmit Interrupts (TXE[2:0])	I bit	CANTIER (TXEIE[2:0])

18.4.7.2 Transmit Interrupt

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXEx flag of the empty message buffer is set.

Table 20-12. SCISR2 Field Descriptions (continued)

Field	Description
3 RXPOL	**Receive Polarity** — This bit control the polarity of the received data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
2 BRK13	**Break Transmit Character Length** — This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit. 0 Break character is 10 or 11 bit long 1 Break character is 13 or 14 bit long
1 TXDIR	**Transmitter Pin Data Direction in Single-Wire Mode** — This bit determines whether the TXD pin is going to be used as an input or output, in the single-wire mode of operation. This bit is only relevant in the single-wire mode of operation. 0 TXD pin to be used as an input in single-wire mode 1 TXD pin to be used as an output in single-wire mode
0 RAF	**Receiver Active Flag** — RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress 1 Reception in progress

20.3.2.9 SCI Data Registers (SCIDRH, SCIDRL)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	R8	T8	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-12. SCI Data Registers (SCIDRH)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 20-13. SCI Data Registers (SCIDRL)

Read: Anytime; reading accesses SCI receive data register

Write: Anytime; writing accesses SCI transmit data register; writing to R8 has no effect

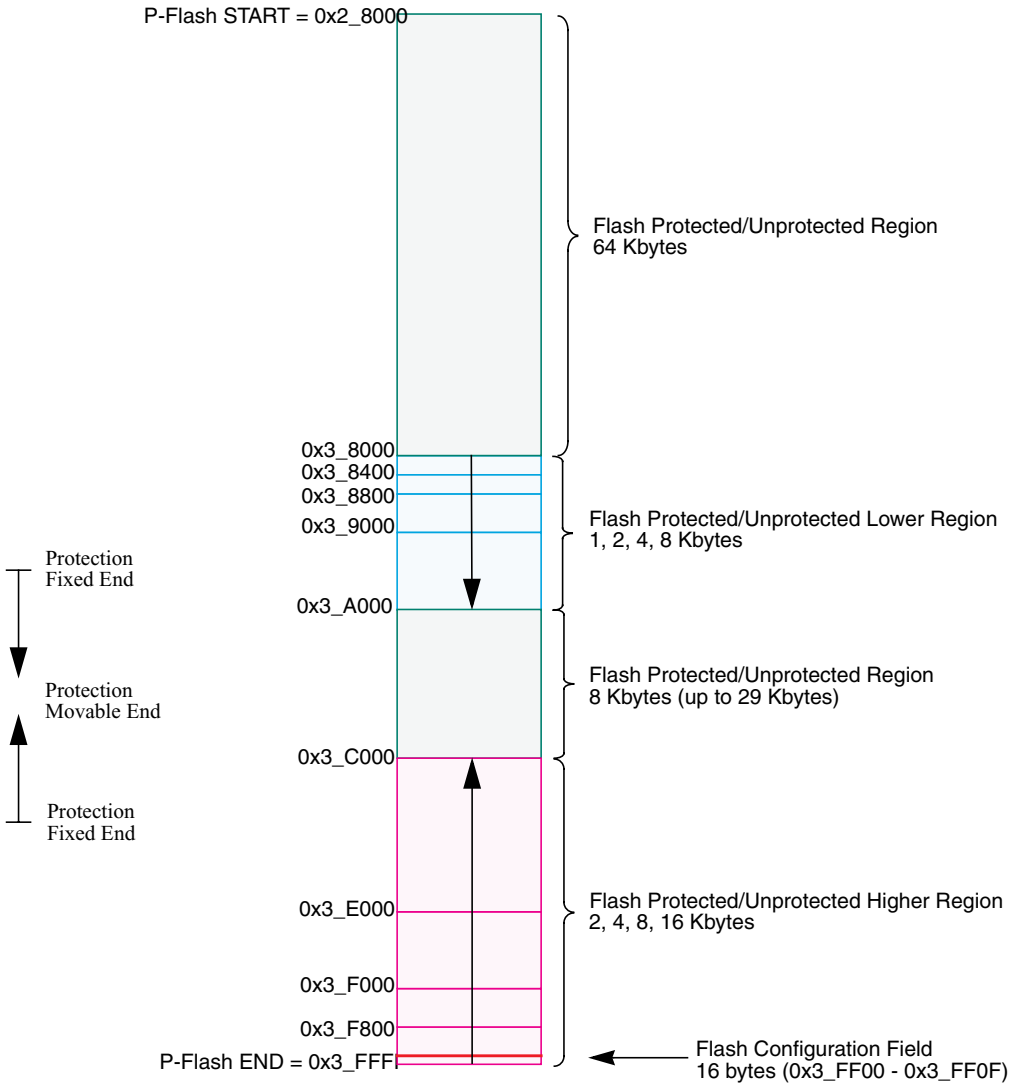

Figure 28-2. P-Flash Memory Map

Table 28-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 28.4.6.6, “Program Once Command”

[1] Used to track firmware patch versions, see Section 28.4.2

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-20. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

28.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

28.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 28-22. Flash Option Register (FOPT)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 28-4) as indicated by reset condition F in Figure 28-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

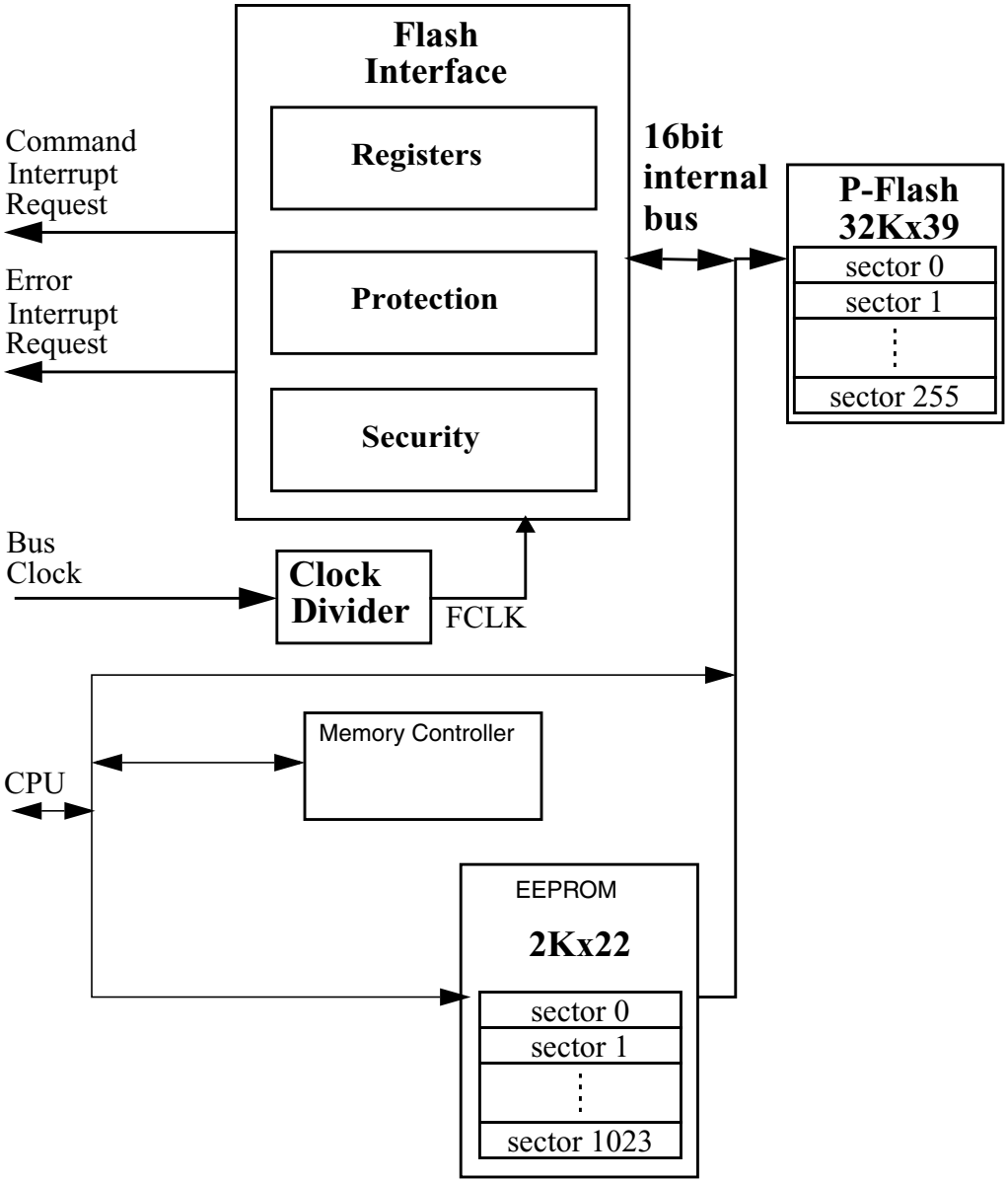

Figure 29-1. FTMRG128K1 Block Diagram

29.2 External Signal Description

The Flash module contains no signals that connect off-chip.

29.3 Memory Map and Registers

This section describes the memory map and registers for the Flash module. Read data from unimplemented memory space in the Flash module is undefined. Write access to unimplemented or reserved memory space in the Flash module will be ignored by the Flash module.

CAUTION

Writing to the Flash registers while a Flash command is executing (that is indicated when the value of flag CCIF reads as '0') is not allowed. If such action is attempted the write operation will not change the register value.

Writing to the Flash registers is allowed when the Flash is not busy executing commands (CCIF = 1) and during initialization right after reset, despite the value of flag CCIF in that case (refer to Section 29.6 for a complete description of the reset sequence).

.

Table 29-2. FTMRG Memory Map

Global Address (in Bytes)	Size (Bytes)	Description
0x0_0000 - 0x0_03FF	1,024	Register Space
0x0_0400 – 0x0_13FF	4,096	EEPROM Memory
0x0_4000 – 0x0_7FFF	16,284	NVMRES[1]=1 : NVM Resource area (see Figure 29-3)
0x2_0000 – 0x3_FFFF	131,072	P-Flash Memory

[1] See NVMRES description in Section 29.4.3

29.3.1 Module Memory Map

The S12 architecture places the P-Flash memory between global addresses 0x2_0000 and 0x3_FFFF as shown in Table 29-3.The P-Flash memory map is shown in Figure 29-2.

Table 29-3. P-Flash Memory Addressing

Global Address	Size (Bytes)	Description
0x2_0000 – 0x3_FFFF	128 K	P-Flash Block Contains Flash Configuration Field (see Table 29-4)

Table 31-15. FSTAT Field Descriptions (continued)

Field	Description
3 MGBUSY	**Memory Controller Busy Flag** — The MGBUSY flag reflects the active state of the Memory Controller. 0 Memory Controller is idle 1 Memory Controller is busy executing a Flash command (CCIF = 0)
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. See Section 31.4.6, “Flash Command Description,” and Section 31.6, “Initialization” for details.

31.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Offset Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 31-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 31-16. FERSTAT Field Descriptions

Field	Description
1 DFDIF	**Double Bit Fault Detect Interrupt Flag** — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.[1] The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF.[2] 0 No double bit fault detected 1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.[1] The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted while command running

1 The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (Flash array read operation returning invalid data attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

2 There is a one cycle delay in storing the ECC DFDIF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

Table 31-29. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x08	Erase All Blocks	Erase all EEPROM (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the EEPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a EEPROM (or P-Flash) block. An erase of the full EEPROM block is only possible when DPOPEN bit in the EEPROT register is set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all EEPROM (and P-Flash) blocks and verifying that all EEPROM (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the EEPROM block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the EEPROM block (special modes only).
0x10	Erase Verify EEPROM Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program EEPROM	Program up to four words in the EEPROM block.
0x12	Erase EEPROM Sector	Erase all bytes in a sector of the EEPROM block.

31.4.5 Allowed Simultaneous P-Flash and EEPROM Operations

Only the operations marked ‘OK’ in Table 31-30 are permitted to be run simultaneously on the Program Flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the EEPROM, providing read (P-Flash) while write (EEPROM) functionality.

Table 31-30. Allowed P-Flash and EEPROM Simultaneous Operations

	EEPROM				
Program Flash	**Read**	**Margin Read[1]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read		OK	OK	OK	
Margin Read[1]					
Program					
Sector Erase					
Mass Erase[2]					OK

1 A ‘Margin Read’ is any read after executing the margin setting commands ‘Set User Margin Level’ or ‘Set Field Margin Level’ with anything but the ‘normal’ level specified. See the Note on margin settings in Section 31.4.6.12 and Section 31.4.6.13.

2 The ‘Mass Erase’ operations are commands ‘Erase All Blocks’ and ‘Erase Flash Block’

CAUTION

Field margin levels must only be used during verify of the initial factory programming.

NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

31.4.6.14 Erase Verify EEPROM Section Command

The Erase Verify EEPROM Section command will verify that a section of code in the EEPROM is erased. The Erase Verify EEPROM Section command defines the starting point of the data to be verified and the number of words.

Table 31-60. Erase Verify EEPROM Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [17:16] to identify the EEPROM block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify EEPROM Section command, the Memory Controller will verify the selected section of EEPROM memory is erased. The CCIF flag will set after the Erase Verify EEPROM Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 31-61. Erase Verify EEPROM Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 31-27)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested section breaches the end of the EEPROM block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

Table A-12. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUOSC	OSCE=1, External Square wave on EXTAL f_{EXTAL}=4MHz, V_{IH}= 1.8V, V_{IL}=0V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-13. CPMU Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]=01,SYNDIV[5:0] = 24
CPMUPOSTDIV	POSTDIV[4:0]=0
CPMUCLKS	PLLSEL=1
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz
API settings for STOP current measurement	
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0
CPMUAPITR	trimmed to 10Khz
CPMUAPIRH/RL	set to $FFFF

Table A-14. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
MSCAN	Configured to loop-back mode using a bit rate of 1Mbit/s
SPI	Configured to master mode, continuously transmit data (0x55 or 0xAA) at 1Mbit/s
SCI	Configured into loop mode, continuously transmit data (0x55) at speed of 57600 baud
PWM	Configured to toggle its pins at the rate of 40kHz
ADC	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.

Table A-24. ADC Conversion Performance 5V range (Junction Temperature From +150°C To +160°C)

S12GN16, S12GN32								
Supply voltage 4.5V < V_{DDA} < 5.5 V, 150°C < T_J < 160°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	M	Resolution	10-Bit	LSB		5		mV
2	M	Differential Nonlinearity	10-Bit	DNL		±0.5		counts
3	M	Integral Nonlinearity	10-Bit	INL		±1		counts
4	M	Absolute Error[2]	10-Bit[3] 10-Bit[4]	AE		±2 ±2		counts
5	C	Resolution	8-Bit	LSB		20		mV
6	C	Differential Nonlinearity	8-Bit	DNL		±0.3		counts
7	C	Integral Nonlinearity	8-Bit	INL		±0.5		counts
8	C	Absolute Error[2]	8-Bit	AE		±1		counts

1 The 8-bit mode operation is structurally tested in production test. Absolute values are tested in 10-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

3 LQFP 48 and bigger

4 LQFP 32 and smaller

Table A-25. ADC Conversion Performance 3.3V range (Junction Temperature From –40°C To +150°C)

S12GNA16, S12GNA32, S12GAS48, S12GA64, S12GA96, S12GA128, S12GA192 and S12GA240								
Supply voltage 3.13V < V_{DDA} < 4.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	12-Bit	LSB		0.80		mV
2	P	Differential Nonlinearity	12-Bit	DNL	-6	±3	6	counts
3	P	Integral Nonlinearity	12-Bit	INL	-7	±3	7	counts
4	P	Absolute Error[2]	12-Bit	AE	-8	±4	8	counts
5	C	Resolution	10-Bit	LSB		3.22		mV
6	C	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
7	C	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	C	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution	8-Bit	LSB		12.89		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.