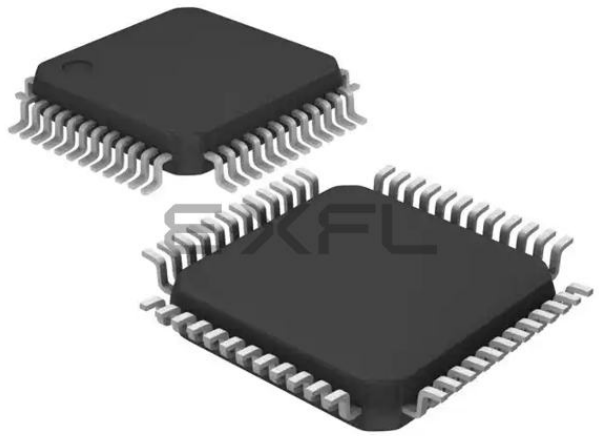

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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128avlf

Table 1-22. 100-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	V_{DDX}	PERJ/PPSJ	Up
4	PA0	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
5	PA1	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
6	PA2	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
7	PA3	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
8	RESET	—	—	—	V_{DDX}	PULLUP	
9	VDDX1	—	—	—	—	—	—
10	VDDR	—	—	—	—	—	—
11	VSSX1	—	—	—	—	—	—
12	PE0[1]	EXTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
13	VSS	—	—	—	—	—	—
14	PE1[1]	XTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
15	TEST	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
16	PA4	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
17	PA5	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
18	PA6	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
19	PA7	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
20	PJ0	KWJ0	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
21	PJ1	KWJ1	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
22	PJ2	KWJ2	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
23	PJ3	KWJ3	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
24	BKGD	MODC	—	—	V_{DDX}	PUCR/BKPUE	Up
25	PB0	ECLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
26	PB1	API_EXTCLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
27	PB2	ECLKX2	—	—	V_{DDX}	PUCR/PUPBE	Disabled

Table 2-18. Block Memory Map (0x0000-0x027F) (continued)

Port	Global Address	Register	Access	Reset Value	Section/Page
T	0x0240	PTT—Port T Data Register	R/W	0x00	2.4.3.15/2-207
	0x0241	PTIT—Port T Input Register	R	[3]	2.4.3.16/2-207
	0x0242	DDRT—Port T Data Direction Register	R/W	0x00	2.4.3.17/2-208
	0x0243	Reserved	R	0x00	
	0x0244	PERT—Port T Pull Device Enable Register	R/W	0x00	2.4.3.18/2-209
	0x0245	PPST—Port T Polarity Select Register	R/W	0x00	2.4.3.19/2-210
	0x0246	Reserved	R	0x00	
	0x0247	Reserved	R	0x00	
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.4.3.20/2-210
	0x0249	PTIS—Port S Input Register	R	[3]	2.4.3.21/2-211
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.4.3.22/2-211
	0x024B	Reserved	R	0x00	
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.4.3.23/2-212
	0x024D	PPSS—Port S Polarity Select Register	R/W	0x00	2.4.3.24/2-212
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.4.3.25/2-213
	0x024F	PRR0—Pin Routing Register 0[4]	R/W	0x00	2.4.3.26/2-213
M	0x0250	PTM—Port M Data Register	R/W	0x00	2.4.3.27/2-215
	0x0251	PTIM—Port M Input Register	R	[3]	2.4.3.29/2-216
	0x0252	DDRM—Port M Data Direction Register	R/W	0x00	2.4.3.29/2-216
	0x0253	Reserved	R	0x00	
	0x0254	PERM—Port M Pull Device Enable Register	R/W	0x00	2.4.3.30/2-217
	0x0255	PPSM—Port M Polarity Select Register	R/W	0x00	2.4.3.31/2-218
	0x0256	WOMM—Port M Wired-Or Mode Register	R/W	0x00	2.4.3.32/2-218
	0x0257	PKGCR—Package Code Register	R/W	[5]	2.4.3.33/2-219
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.4.3.34/2-220
	0x0259	PTIP—Port P Input Register	R	[3]	2.4.3.35/2-221
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.4.3.36/2-222
	0x025B	Reserved	R	0x00	
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0x00	2.4.3.37/2-222
	0x025D	PPSP—Port P Polarity Select Register	R/W	0x00	2.4.3.38/2-223
	0x025E	PIEP—Port P Interrupt Enable Register	R/W	0x00	2.4.3.39/2-224
	0x025F	PIFP—Port P Interrupt Flag Register	R/W	0x00	2.4.3.40/2-224

Table 2-54. DDRM Register Field Descriptions

Field	Description
3-0 DDRM	**Port M data direction**— This bit determines whether the associated pin is a general-purpose input or output. 1 Associated pin configured as output 0 Associated pin configured as input

2.4.3.30 Port M Pull Device Enable Register (PERM)

Address 0x0254 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERM3	PERM2	PERM1	PERM0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0254 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PERM1	PERM0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-31. Port M Pull Device Enable Register (PERM)

[1] Read: Anytime
Write: Anytime

Table 2-55. PERM Register Field Descriptions

Field	Description
3-1 PERM	**Port M pull device enable**—Enable pull device on input pin or wired-or output pin This bit controls whether a pull device on the associated port input pin is active. The polarity is selected by the related polarity select register bit. If a pin is used as output this bit has only effect if used in wired-or mode with a pullup device. 1 Pull device enabled 0 Pull device disabled
0 PERM	**Port M pull device enable**—Enable pull device on input pin or wired-or output pin This bit controls whether a pull device on the associated port input pin is active. The polarity is selected by the related polarity select register bit. If a pin is used as output this bit has only effect if used in wired-or mode with a pullup device. If CAN is active the selection of a pulldown device on the RXCAN input will have no effect. 1 Pull device enabled 0 Pull device disabled

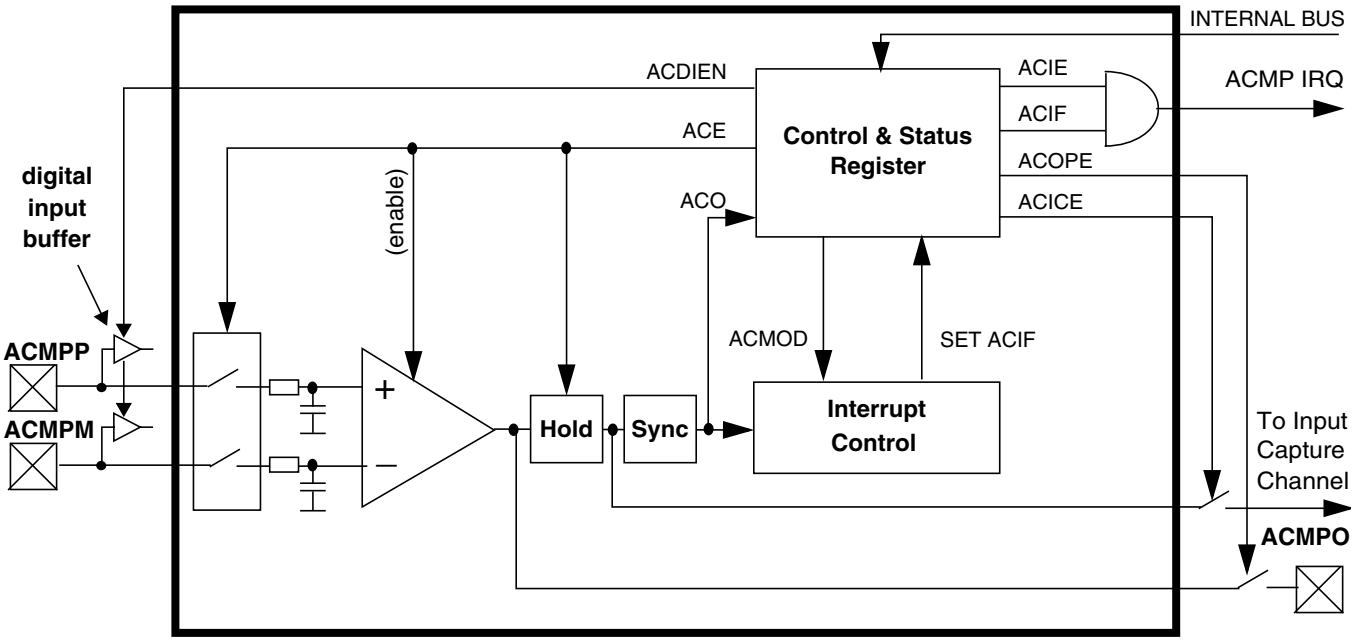

Figure 3-1. ACMP Block Diagram

Figure 3-2.

3.4 External Signals

The ACMP has two analog input signals, ACMPP and ACMPM, and one digital output, ACMPO. The associated pins are defined by the package option.

The ACMPP signal is connected to the non-inverting input of the comparator. The ACMPM signal is connected to the inverting input of the comparator. Each of these signals can accept an input voltage that varies across the full 5V operating voltage range. The module monitors the voltage on these inputs independent of any other functions in use (GPIO, ADC).

The raw comparator output signal can optionally be driven on an external pin.

3.5 Modes of Operation

1. Normal Mode
   The ACMP is operating when enabled and not in STOP mode.
2. Shutdown Mode
   The ACMP is held in shutdown mode either when disabled or during STOP mode. In this case the supply of the analog block is disconnected for power saving. ACMPO drives zero in shutdown mode.

16.4 Functional Description

The ADC12B16C consists of an analog sub-block and a digital sub-block.

16.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

16.4.1.1 Sample and Hold Machine

The Sample and Hold Machine controls the storage and charge of the sample capacitor to the voltage level of the analog signal at the selected ADC input channel.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.

During the hold process the analog input is disconnected from the storage node.

16.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

16.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable to be either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages.

By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

When not converting the A/D machine is automatically powered down.

Only analog input signals within the potential range of VRL to VRH (A/D reference potentials) will result in a non-railed digital output code.

16.4.2 Digital Sub-Block

This subsection describes some of the digital features in more detail. See Section 16.3.2, “Register Descriptions” for all details.

16.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to an external event rather than relying only on software to trigger the ATD module when a conversion is about to take place. The external trigger signal (out of reset ATD channel 15, configurable in ATDCTL1) is programmable to be

Table 17-5. DAC Modes of Operation

Operational amplifier	001	disabled	enabled	disabled	depend on AMPP and AMPM input
Unbuffered DAC	100	enabled	disabled	unbuffered resistor output voltage	disconnected
Unbuffered DAC with Operational amplifier	101	enabled	enabled	unbuffered resistor output voltage	depend on AMPP and AMPM input
Buffered DAC	111	enabled	enabled	disconnected	buffered resistor output voltage

The DAC resistor network itself can work on two different voltage ranges:

Table 17-6. DAC Resistor Network Voltage ranges

DAC Mode	Description
Full Voltage Range (FVR)	DAC resistor network provides a output voltage over the complete input voltage range, default after reset
Reduced Voltage Range	DAC resistor network provides a output voltage over a reduced input voltage range

Table 17-7 shows the control signal decoding for each mode. For more detailed mode description see the sections below.

Table 17-7. DAC Control Signals

DACM		DAC resistor network	Operational Amplifier	Switch S1	Switch S2	Switch S3
Off	000	disabled	disabled	open	open	open
Operational amplifier	001	disabled	enabled	closed	open	open
Unbuffered DAC	100	enabled	disabled	open	open	closed
Unbuffered DAC with Operational amplifier	101	enabled	enabled	closed	open	closed
Buffered DAC	111	enabled	enabled	open	closed	open

17.5.2 Mode “Off”

The “Off” mode is the default mode after reset and is selected by DACCTL.DACM[2:0] = 0x0. During this mode the DAC resistor network and the operational amplifier are disabled and all switches are open. This mode provides the lowest power consumption. For decoding of the control signals see Table 17-7.

17.5.3 Mode “Operational Amplifier”

The “Operational Amplifier” mode is selected by DACCTL.DACM[2:0] = 0x1. During this mode the operational amplifier can be used independent from the DAC resister network. All required amplifier signals, AMP, AMPP and AMPM are available on the pins. The DAC resistor network output is disconnected from the DACU pin. The connection between the amplifier output and the negative amplifier input is open. For decoding of the control signals see Table 17-7.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
Reset	0	0	0	0	0	0	0	0

Figure 19-4. PWM Polarity Register (PWMPOL)

Read: Anytime

Write: Anytime

NOTE

PPOLx register bits can be written anytime. If the polarity is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition

Table 19-3. PWMPOL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7–0 PPOL[7:0]	**Pulse Width Channel 7–0 Polarity Bits** 0 PWM channel 7–0 outputs are low at the beginning of the period, then go high when the duty count is reached. 1 PWM channel 7–0 outputs are high at the beginning of the period, then go low when the duty count is reached.

19.3.2.3 PWM Clock Select Register (PWMCLK)

Each PWM channel has a choice of four clocks to use as the clock source for that channel as described below.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
Reset	0	0	0	0	0	0	0	0

Figure 19-5. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLK0 to PCLK7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

19.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 19-16. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed, as described in Section 19.4.2.3, “PWM Period and Duty”. The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

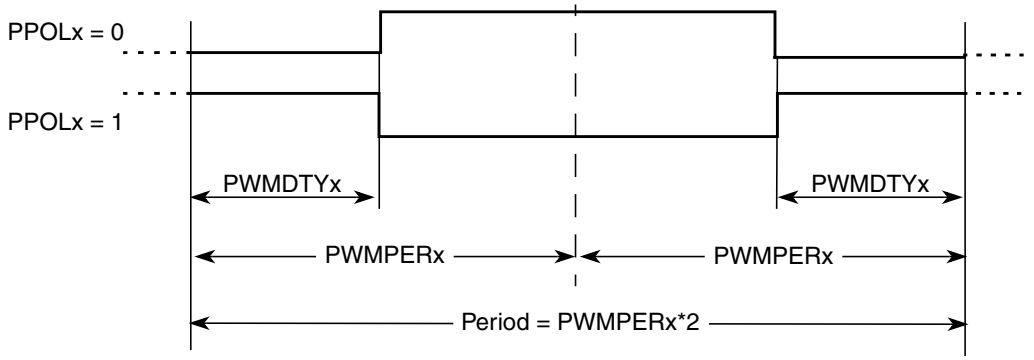

Figure 19-19. PWM Center Aligned Output Waveform

To calculate the output frequency in center aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by twice the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / (2*PWMPERx)
- PWMx Duty Cycle (high time as a% of period):
  - — Polarity = 0 (PPOLx = 0)

    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - — Polarity = 1 (PPOLx = 1)

    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a center aligned output, consider the following case:

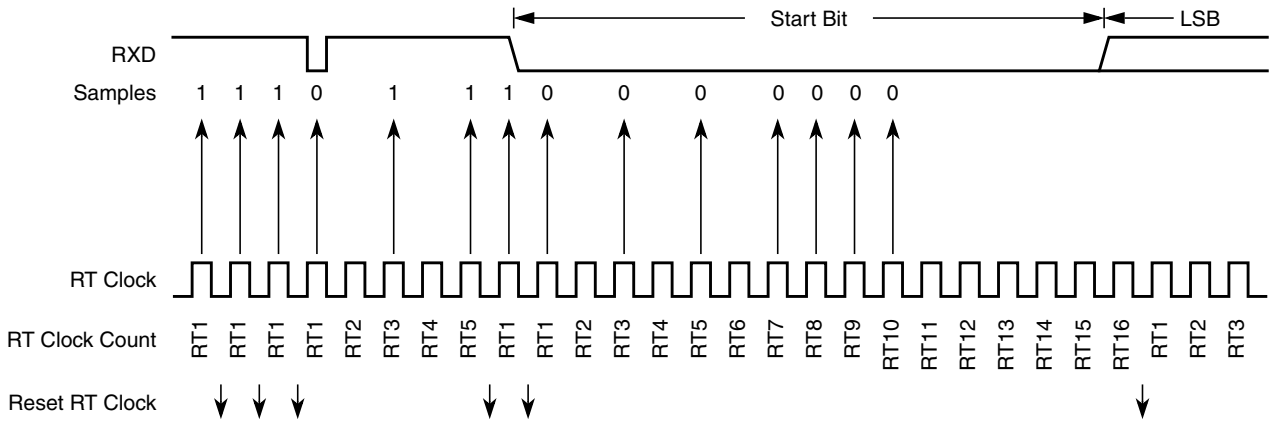

Figure 20-22. Start Bit Search Example 1

In Figure 20-23, verification sample at RT3 is high. The RT3 sample sets the noise flag. Although the perceived bit time is misaligned, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

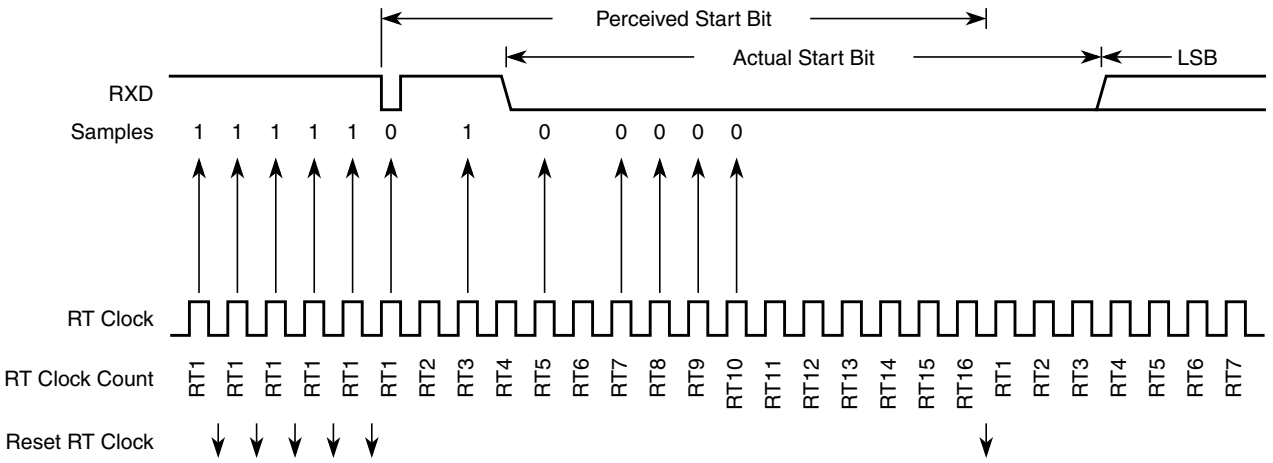

Figure 20-23. Start Bit Search Example 2

In Figure 20-24, a large burst of noise is perceived as the beginning of a start bit, although the test sample at RT5 is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

24.4.4.3 Valid Flash Module Commands

Table 24-25 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input mmc_ss_mode_ts2 asserted. MCU Secured state is selected by input mmc_secure input asserted.

Table 24-25. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

1 Unsecured Normal Single Chip mode
2 Unsecured Special Single Chip mode.
3 Secured Normal Single Chip mode.
4 Secured Special Single Chip mode.

24.4.4.4 P-Flash Commands

Table 24-26 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 24-26. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.

25.4.6.2 Erase Verify Block Command

The Erase Verify Block command allows the user to verify that an entire P-Flash or EEPROM block has been erased. The FCCOB FlashBlockSelectionCode[1:0] bits determine which block must be verified.

Table 25-33. Erase Verify Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x02	Flash block selection code [1:0]. See Table 25-34

Table 25-34. Flash block selection code description

Selection code[1:0]	Flash block to be verified
00	EEPROM
01	Invalid (ACCERR)
10	Invalid (ACCERR)
11	P-Flash

Upon clearing CCIF to launch the Erase Verify Block command, the Memory Controller will verify that the selected P-Flash or EEPROM block is erased. The CCIF flag will set after the Erase Verify Block operation has completed.If the block is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 25-35. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

25.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

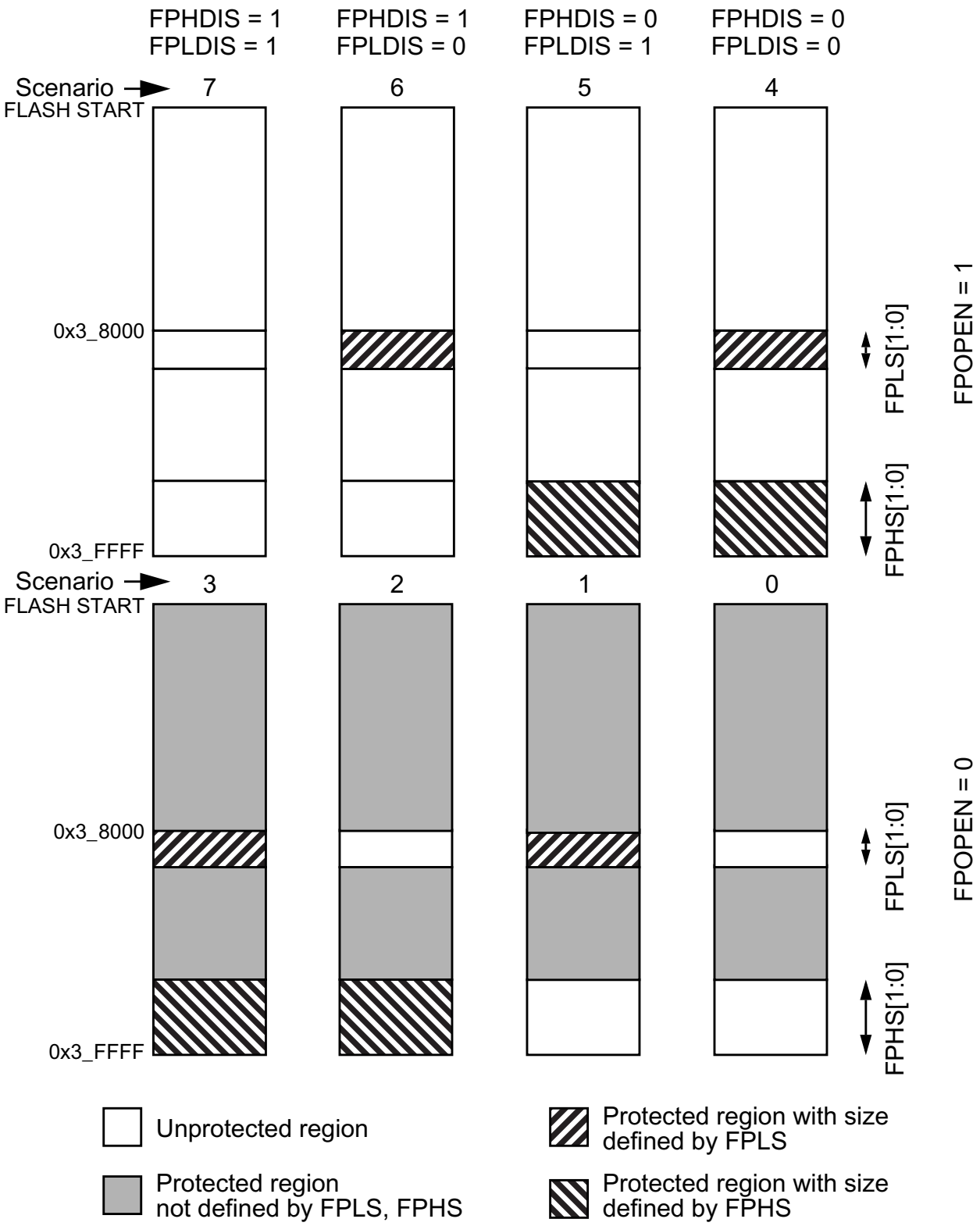

Figure 26-14. P-Flash Protection Scenarios

28.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 28-16. Flash Common Command Object High Register (FCCOBHI)

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 28-17. Flash Common Command Object Low Register (FCCOBLO)

28.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 28-24. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 28-24 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 28.4.6.

Table 28-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	6'h0, Global address [17:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]

29.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 29.4.7, “Interrupts”).

29.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

29.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 29-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x3_FF0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

29.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x3_FF00-0x3_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 29.3.2.2), the Verify Backdoor Access Key command (see Section 29.4.6.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 29-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

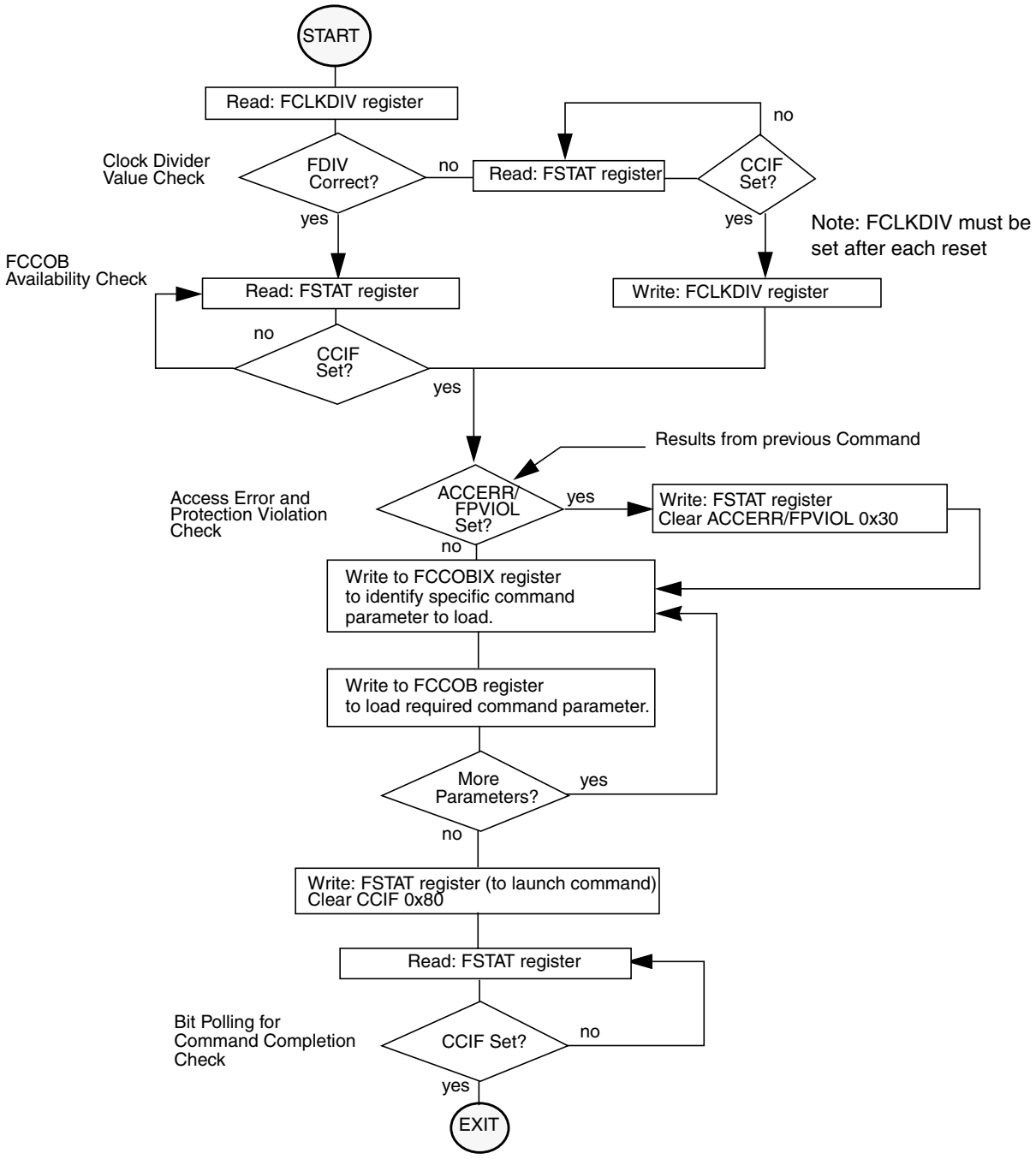

Figure 30-26. Generic Flash Command Write Sequence Flowchart

Table 31-41. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 31-27)
		Set if an invalid global address [17:0] is supplied see Table 31-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

31.4.6.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 31.4.6.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 31-42. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

31.4.7.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with the DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 31.3.2.5, “Flash Configuration Register (FCNFG)”, Section 31.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 31.3.2.7, “Flash Status Register (FSTAT)”, and Section 31.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 31-27.

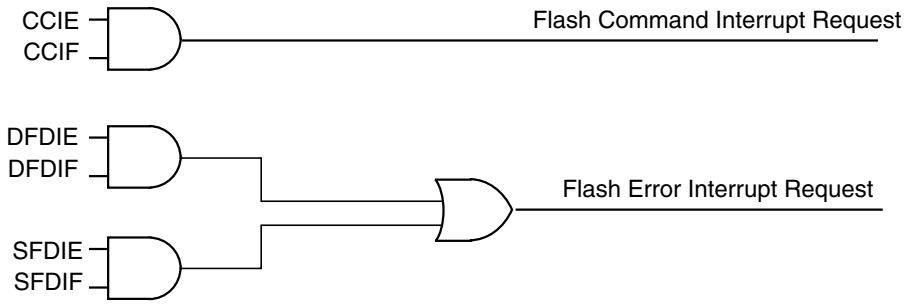

Figure 31-27. Flash Module Interrupts Implementation

31.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 31.4.7, “Interrupts”).

31.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	S12GN32, S12GNA32, S12GN16, S12GNA16	S12G64, S12GA64, S12G48, S12GN48, S12GA64	S12G128, S12GA128, S12G96, S12GA96	S12G240, S12GA240, S12G192, S12GA192	Unit
20-pin TSSOP								
1	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}	91				°C/W
2	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}	72				°C/W
3	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}	58				°C/W
4	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}	51				°C/W
5	D	Junction to Board[4]	θ_{JB}	29				°C/W
6	D	Junction to Case[5]	θ_{JC}	20				°C/W
7	D	Junction to Package Top[6]	Ψ_{JT}	4				°C/W
32-pin LQFP								
8	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}	81	84			°C/W
9	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}	68	70			°C/W
10	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}	57	56			°C/W
11	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}	50	49			°C/W
12	D	Junction to Board[4]	θ_{JB}	35	32			°C/W
13	D	Junction to Case[5]	θ_{JC}	25	23			°C/W
14	D	Junction to Package Top[6]	Ψ_{JT}	8	6			°C/W
48-pin LQFP								
15	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}	81	80	79	75	°C/W
16	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}	68	67	66	62	°C/W
17	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}	57	56	56	51	°C/W
18	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}	50	50	49	45	°C/W
19	D	Junction to Board[4]	θ_{JB}	35	34	33	30	°C/W
20	D	Junction to Case[5]	θ_{JC}	25	24	21	19	°C/W
21	D	Junction to Package Top[6]	Ψ_{JT}	8	6	4	N/A	°C/W

Table D-1. Bondpad Coordinates

Die Pad	Bond Post	Die Pad X Coordinate	Die Pad Y Coordinate	Function
28	28	-1315.5	-1472.06	PB[3]
29	29	-1134.5	-1472.06	PP[0]
30	30	-964.5	-1472.06	PP[1]
31	31	-794.5	-1472.06	PP[2]
32	32	-660.5	-1472.06	PP[3]
33	33	-526.5	-1472.06	PP[4]
34	34	-404.5	-1472.06	PP[5]
35	35	-292.5	-1472.06	PP[6]
36	36	-190.5	-1472.06	PP[7]
37	37	-105.5	-1472.06	VDDX3
38	38	-0.5	-1472.06	VSSX3
39	39	93.5	-1472.06	PT[7]
40	40	189.5	-1472.06	PT[6]
41	41	291.5	-1472.06	PT[5]
42	42	403.5	-1472.06	PT[4]
43	43	525.5	-1472.06	PT[3]
44	44	659.5	-1472.06	PT[2]
45	45	805.5	-1472.06	PT[1]
46	46	964.5	-1472.06	PT[0]
47	47	1120.5	-1472.06	PB[4]
48	48	1242.5	-1472.06	PB[5]
49	49	1412.5	-1472.06	PB[6]
50	50	1582.5	-1472.06	PB[7]
51	51	-1832.06	-1347.5	PC[0]
52	52	-1832.06	-1139.5	PC[1]
53	53	-1832.06	-1022.5	PC[2]
54	54	-1832.06	-905.5	PC[3]
55	55	-1832.06	-788.5	PAD[0]
56	56	-1832.06	-681.5	PAD[8]
57	57	-1832.06	-574.5	PAD[1]