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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128avlhr

- Interrupt flag register for pin interrupts on ports P, J and AD
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Routing register to support programmable signal redirection in 20 TSSOP only
- Routing register to support programmable signal redirection in 100 LQFP package only
- Package code register preset by factory related to package in use, writable once after reset. Also includes bit to reprogram routing of API_EXTCLK in all packages.
- Control register for free-running clock outputs
-

1.3.5 Main External Oscillator (XOSCLCP)

- Loop control Pierce oscillator using a 4 MHz to 16 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals
  - Oscillator pins can be shared w/ GPIO functionality

1.3.6 Internal RC Oscillator (IRC)

- Trimmable internal reference clock.
  - Frequency: 1 MHz
  - Trimmed accuracy over –40˚C to +125˚C ambient temperature range:
    ±1.0% for temperature option C and V (see Table A-4)
    ±1.3% for temperature option M (see Table A-4)

1.3.7 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - External 4–16 MHz resonator/crystal (XOSCLCP)
    - Internal 1 MHz RC oscillator (IRC)

Table 2-4. Signals and Priorities

Port	Pin	Signal	Signals per Device and Package (signal priority on pin from top to bottom)																		I/O	Description
			GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GN32 / GNA32	GN16 / GNA16	G64 / G48	GN48	GN32	GN16	GN32	GN16		
			100			64					48							32				20			
E	PE1	XTAL	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	-	CPMU OSC signal
		TXD0																				❑	❑	I/O	SCI transmit
		IOC3																				❍	❍	I/O	Timer channel
		PWM1																				■	■	O	PWM channel
		ETRIG1																				■	■	I	ADC external trigger
		[PE1]	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I/O	GPIO
	PE0	EXTAL	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	-	CPMU OSC signal
		RXD0																				❑	❑	I	SCI receive
		IOC2																				❍	❍	I/O	Timer channel
		PWM0																				■	■	O	PWM channel
		ETRIG0																				■	■	I	ADC external trigger
		[PE0]	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I/O	GPIO
T	PT7-PT6	IOC7-IOC6	■	■	■	■	■	■																I/O	Timer channel
		[PTT7:PTT6]	■	■	■	■	■	■	■	■														I/O	GPIO
	PT5-PT4	IOC5-IOC4	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■							I/O	Timer channel
		[PTT5:PTT4]	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■							I/O	GPIO
	PT3-PT2	IOC3-IOC2	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			I/O	Timer channel
		[PTT3:PTT2]	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			I/O	GPIO
	PT1	$\overline{\text{IRQ}}$				■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I	Maskable level- or falling-edge sensitive interrupt
		IOC1	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I/O	Timer channel
		[PTT1]	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I/O	GPIO
	PT0	$\overline{\text{XIRQ}}$				■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I	Non-maskable level-sensitive interrupt
		IOC0	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I/O	Timer channel
		[PTT0]	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	I/O	GPIO

Legend

■	Signal available on pin
❍	Routing option on pin
❑	Routing reset location
	Not available on pin

Table 2-85. PPS0AD Register Field Descriptions

Field	Description
7-0 PPS0AD	**Port AD pull device select**—Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. This bit also selects the polarity of the active pin interrupt edge. 1 Pulldown device selected; rising edge selected 0 Pullup device selected; falling edge selected

2.4.3.60 Port AD Polarity Select Register (PPS1AD)

Address 0x027B

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PPS1AD7	PPS1AD6	PPS1AD5	PPS1AD4	PPS1AD3	PPS1AD2	PPS1AD1	PPS1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-59. Port AD Polarity Select Register (PPS1AD)

[1] Read: Anytime
Write: Anytime

Table 2-86. PPS1AD Register Field Descriptions

Field	Description
7-0 PPS1AD	**Port AD pull device select**—Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. This bit also selects the polarity of the active pin interrupt edge. 1 Pulldown device selected; rising edge selected 0 Pullup device selected; falling edge selected

Both interrupts are capable to wake-up the device from stop mode. Means for glitch filtering are not provided on these pins.

2.5.4.2 Pin Interrupts and Wakeup

Ports P, J and AD offer pin interrupt capability. The related interrupt enable (PIE) as well as the sensitivity to rising or falling edges (PPS) can be individually configured on per-pin basis. All bits/pins in a port share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a port interrupt flag (PIF) and its corresponding port interrupt enable (PIE) are both set. The pin interrupt feature is also capable to wake up the CPU when it is in stop or wait mode.

A digital filter on each pin prevents short pulses from generating an interrupt. A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level. Else the sampling logic is restarted.

In run and wait mode the filters are continuously clocked by the bus clock. Pulses with a duration of $t_{PULSE} < n_{P\_MASK}/f_{bus}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > n_{P\_PASS}/f_{bus}$ guarantee a pin interrupt.

In stop mode the clock is generated by an RC-oscillator. The minimum pulse length varies over process conditions, temperature and voltage (Figure 2-65). Pulses with a duration of $t_{PULSE} < t_{P\_MASK}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > t_{P\_PASS}$ guarantee a wakeup event.

Please refer to the appendix table “Pin Interrupt Characteristics” for pulse length limits.

To maximize current saving the RC oscillator is active only if the following condition is true on any individual pin:

Sample count <= 4 (at active or passive level) and interrupt enabled (PIE=1) and interrupt flag not set (PIF=0).

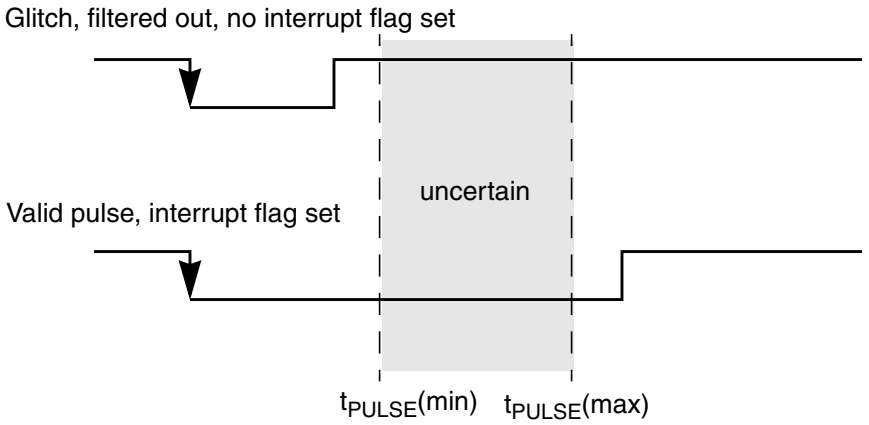


Figure 2-65. Interrupt Glitch Filter (here: active low level selected)

Chapter 10
S12 Clock, Reset and Power Management Unit (S12CPMU)

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V04.03	29 Jan 10	29 Jan 10		Added Note in section 10.3.2.16/10-380 to precise description of API behavior after feature enable for the first time-out period.
V04.04	03 Mar 10	03 Mar 10		Corrected typos.
V04.05	23. Mar 10	23 Mar 10		Corrected typos.
V04.06	13 Apr 10	13 Apr 10		Corrected typo in Table 10-6
V04.07	28 Apr 10	28 Apr 10		Major rework fixing typos, figures and tables and improved description of Adaptive Oscillator Filter.
V04.08	03 May 10	03 Mail 10		Improved pin description in Section 10.2, “Signal Description
V04.09	22 Jun 10	22 Jun 10		Changed IP-Name from OSCLCP to XOSCLCP, added OSCCLK_LCP clock name intoFigure 10-1 and Figure 10-2 updated description of Section 10.2.2, “EXTAL and XTAL.
V04.10	01 Jul 10	01 Jul 10		Added TC trimming to feature list
V04.11	23 Aug 10	23 Aug 10		Removed feature of adaptive oscillator filter. Register bits 6 and 4to 0in the CPMUOSC register are marked reserved and do not alter.
V04.12	27 April 12	27 April 12		Corrected wording for API interrupt flag Changed notation of IRC trim values for 0x00000 to 0b00000
V04.13	6 Mar 13	6 Mar 13		Table 10-19. correction: substituted f_{ACLK} by ACLK Clock Period

10.1 Introduction

This specification describes the function of the Clock, Reset and Power Management Unit (S12CPMU).

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical quartz crystals and ceramic resonators.
- The Voltage regulator (IVREG) operates from the range 3.13V to 5.5V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.

0x0037

	7	6	5	4	3	2	1	0
R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
W								
Reset	0	Note 1	Note 2	0	0	Note 3	0	0

1. PORF is set to 1 when a power on reset occurs. Unaffected by System Reset.
2. LVRF is set to 1 when a low voltage reset occurs. Unaffected by System Reset. Set by power on reset.
3. ILAF is set to 1 when an illegal address reset occurs. Unaffected by System Reset. Cleared by power on reset.

= Unimplemented or Reserved

Figure 10-7. S12CPMU Flags Register (CPMUFLG)

Read: Anytime

Write: Refer to each bit for individual write conditions

Table 10-3. CPMUFLG Field Descriptions

Field	Description
7 RTIF	**Real Time Interrupt Flag** — RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE=1), RTIF causes an interrupt request. 0 RTI time-out has not yet occurred. 1 RTI time-out has occurred.
6 PORF	**Power on Reset Flag** — PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on reset has not occurred. 1 Power on reset has occurred.
5 LVRF	**Low Voltage Reset Flag** — LVRF is set to 1 when a low voltage reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Low voltage reset has not occurred. 1 Low voltage reset has occurred.
4 LOCKIF	**PLL Lock Interrupt Flag** — LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (LOCKIE=1), LOCKIF causes an interrupt request. 0 No change in LOCK bit. 1 LOCK bit has changed.
3 LOCK	**Lock Status Bit** — LOCK reflects the current state of PLL lock condition. Writes have no effect. While PLL is unlocked (LOCK=0) fPLL is fVCO / 4 to protect the system from high core clock frequencies during the PLL stabilization time tlock. 0 VCOCLK is not within the desired tolerance of the target frequency. $f_{PLL} = f_{VCO}/4$. 1 VCOCLK is within the desired tolerance of the target frequency. $f_{PLL} = f_{VCO}/(POSTDIV+1)$.
2 ILAF	**Illegal Address Reset Flag** — ILAF is set to 1 when an illegal address reset occurs. Refer to MMC chapter for details. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Illegal address reset has not occurred. 1 Illegal address reset has occurred.

Table 13-9. Examples of ideal decimal ATD Results

Input Signal VRL = 0 Volts VRH = 5.12 Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	Reserved
5.120 Volts	255	1023	Reserved
...	...	...	
0.022	1	4	
0.020	1	4	
0.018	1	4	
0.016	1	3	
0.014	1	3	
0.012	1	2	
0.010	1	2	
0.008	0	2	
0.006	0	1	
0.004	0	1	
0.003	0	1	
0.002	0	0	
0.000	0	0	

Table 13-10. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	12
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	12
1	1	1	0	12
1	1	1	1	12

Table 13-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion

15.5 Resets

At reset the ADC10B16C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 15.3.2, “Register Descriptions”) which details the registers and their bit-field.

15.6 Interrupts

The interrupts requested by the ADC10B16C are listed in Table 15-24. Refer to MCU specification for related vector address and priority.

Table 15-24. ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2
Compare Interrupt	I bit	ACMPIE in ATDCTL2

See Section 15.3.2, “Register Descriptions” for further details.

16.1.2 Modes of Operation

16.1.2.1 Conversion Modes

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

16.1.2.2 MCU Operating Modes

- **Stop Mode**
  Entering Stop Mode aborts any conversion sequence in progress and if a sequence was aborted restarts it after exiting stop mode. This has the same effect/consequences as starting a conversion sequence with write to ATDCTL5. So after exiting from stop mode with a previously aborted sequence all flags are cleared etc.
- **Wait Mode**
  ADC12B16C behaves same in Run and Wait Mode. For reduced power consumption continuous conversions should be aborted before entering Wait mode.
- **Freeze Mode**
  In Freeze Mode the ADC12B16C will either continue or finish or stop converting according to the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 24-17. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Operation Enable** — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 24-18 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS bit defines an unprotected address range as specified by the FPHS bits 1 When FPOPEN is set, the FPHDIS bit enables protection for the address range specified by the FPHS bits
6 RNV[6]	**Reserved Nonvolatile Bit** — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown inTable 24-19. The FPHS bits can only be written to while the FPHDIS bit is set.
2–0 RNV[2:0]	**Reserved Nonvolatile Bits** — These RNV bits should remain in the erased state.

Table 24-18. P-Flash Protection Function

FPOPEN	FPHDIS	Function[1]
1	1	No P-Flash Protection
1	0	Protected High Range
0	1	Full P-Flash Memory Protected
0	0	Unprotected High Range

[1] For range sizes, refer to Table 24-19.

Table 24-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

24.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 24-21. Flash Option Register (FOPT)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 24-4) as indicated by reset condition F in Figure 24-21. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 24-23. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

24.3.2.17 Flash Reserved5 Register (FRSV5)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-22. Flash Reserved5 Register (FRSV5)

All bits in the FRSV5 register read 0 and are not writable.

24.3.2.18 Flash Reserved6 Register (FRSV6)

This Flash register is reserved for factory testing.

25.4.4.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 25.3.2.3).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 25-26.

Table 26-28. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x02	Erase Verify Block	Verify that a P-Flash block is erased.
0x03	Erase Verify P-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x04	Read Once	Read a dedicated 64 byte field in the nonvolatile information register in P-Flash block that was previously programmed using the Program Once command.
0x06	Program P-Flash	Program a phrase in a P-Flash block.
0x07	Program Once	Program a dedicated 64 byte field in the nonvolatile information register in P-Flash block that is allowed to be programmed only once.
0x08	Erase All Blocks	Erase all P-Flash (and EEPROM) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the EEPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a P-Flash (or EEPROM) block. An erase of the full P-Flash block is only possible when FPLDIS, FPHDIS and FPOPEN bits in the FPROT register are set prior to launching the command.
0x0A	Erase P-Flash Sector	Erase all bytes in a P-Flash sector.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all P-Flash (and EEPROM) blocks and verifying that all P-Flash (and EEPROM) blocks are erased.
0x0C	Verify Backdoor Access Key	Supports a method of releasing MCU security by verifying a set of security keys.
0x0D	Set User Margin Level	Specifies a user margin read level for all P-Flash blocks.
0x0E	Set Field Margin Level	Specifies a field margin read level for all P-Flash blocks (special modes only).

26.4.4.5 EEPROM Commands

Table 26-29 summarizes the valid EEPROM commands along with the effects of the commands on the EEPROM block.

Table 26-29. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x01	Erase Verify All Blocks	Verify that all EEPROM (and P-Flash) blocks are erased.
0x02	Erase Verify Block	Verify that the EEPROM block is erased.

Table 27-63. Program EEPROM Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 27-27)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the EEPROM block
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

27.4.6.16 Erase EEPROM Sector Command

The Erase EEPROM Sector operation will erase all addresses in a sector of the EEPROM block.

Table 27-64. Erase EEPROM Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x12	Global address [17:16] to identify EEPROM block
001	Global address [15:0] anywhere within the sector to be erased. See Section 27.1.2.2 for EEPROM sector size.	

Upon clearing CCIF to launch the Erase EEPROM Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase EEPROM Sector operation has completed.

Table 27-65. Erase EEPROM Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 27-27)
		Set if an invalid global address [17:0] is suppliedsee Table 27-3)
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

28.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 28-36. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 28-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid global address [17:0] is supplied see Table 28-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG96K1.

2 As found in the memory map for FTMRG96K1.

28.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 28.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 28-38. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	S12GN32, S12GNA32, S12GN16, S12GNA16	S12G64, S12GA64, S12G48, S12GN48, S12GA64	S12G128, S12GA128, S12G96, S12GA96	S12G240, S12GA240, S12G192, S12GA192	Unit
48-pin QFN								
22	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}	82				°C/W
23	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}	67				°C/W
24	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}	28				°C/W
25	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}	23				°C/W
26	D	Junction to Board[4]	θ_{JB}	11				°C/W
27	D	Junction to Case[5]	θ_{JC}	N/A				°C/W
28	D	Junction to Package Top[6]	Ψ_{JT}	4				°C/W
64-pin LQFP								
29	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}		70	70	70	°C/W
30	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}		59	58	58	°C/W
31	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}		52	52	52	°C/W
32	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}		46	46	45	°C/W
33	D	Junction to Board[4]	θ_{JB}		34	34	35	°C/W
34	D	Junction to Case[5]	θ_{JC}		20	18	17	°C/W
35	D	Junction to Package Top[6]	Ψ_{JT}		5	4	N/A	°C/W
100-pin LQFP								
36	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}			61	62	°C/W
37	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}			51	55	°C/W
38	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}			49	51	°C/W
39	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}			43	47	°C/W
40	D	Junction to Board[4]	θ_{JB}			34	37	°C/W
41	D	Junction to Case[5]	θ_{JC}			16	17	°C/W
42	D	Junction to Package Top[6]	Ψ_{JT}			3	N/A	°C/W

A.4.3.1 ADC Accuracy Definitions

For the following definitions see also Figure A-1.
Differential non-linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The integral non-linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

Table A-23. ADC Conversion Performance 5V range (Junction Temperature From –40°C To +150°C)

S12GN16, S12GN32, S12GN48, S12G48, S12G64, S12G96, S12G128, S12G192, and S12G240								
Supply voltage 4.5V < V_{DDA} < 5.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	10-Bit	LSB		5		mV
2	P	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
3	P	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
4	P	Absolute Error[2]	10-Bit[3] 10-Bit[4]	AE	-3 -4	±2 ±2	3 4	counts
5	C	Resolution	8-Bit	LSB		20		mV
6	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
7	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
8	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit mode operation is structurally tested in production test. Absolute values are tested in 10-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

3 LQFP 48 and bigger

4 LQFP 32 and smaller

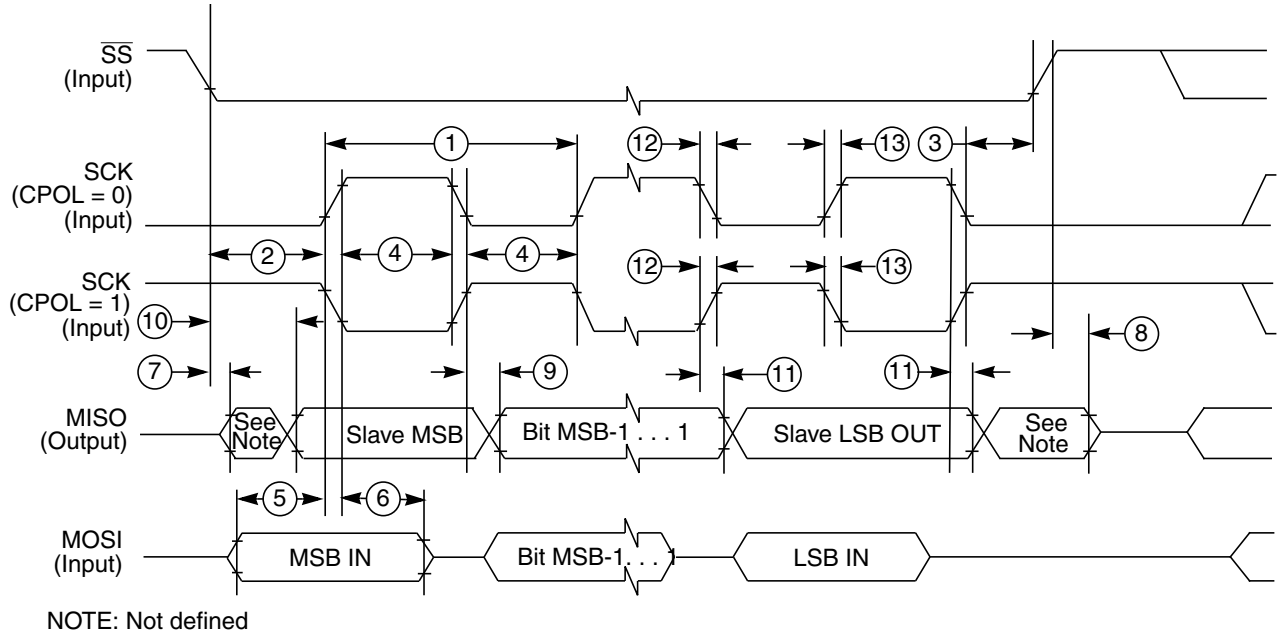
In Table A-51 the timing characteristics for master mode are listed.

Table A-51. SPI Master Mode Timing Characteristics

Conditions are 4.5 V < V_{DD35} < 5.5 V junction temperature from –40°C to T_{Jmax}.							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	D	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	D	Enable Lead Time	t_L	—	1/2	—	t_{sck}
3	D	Enable Trail Time	t_T	—	1/2	—	t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	15	ns
10	D	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	D	Data Hold Time (Outputs)	t_{ho}	0	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	9	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	9	ns

A.15.2 Slave Mode

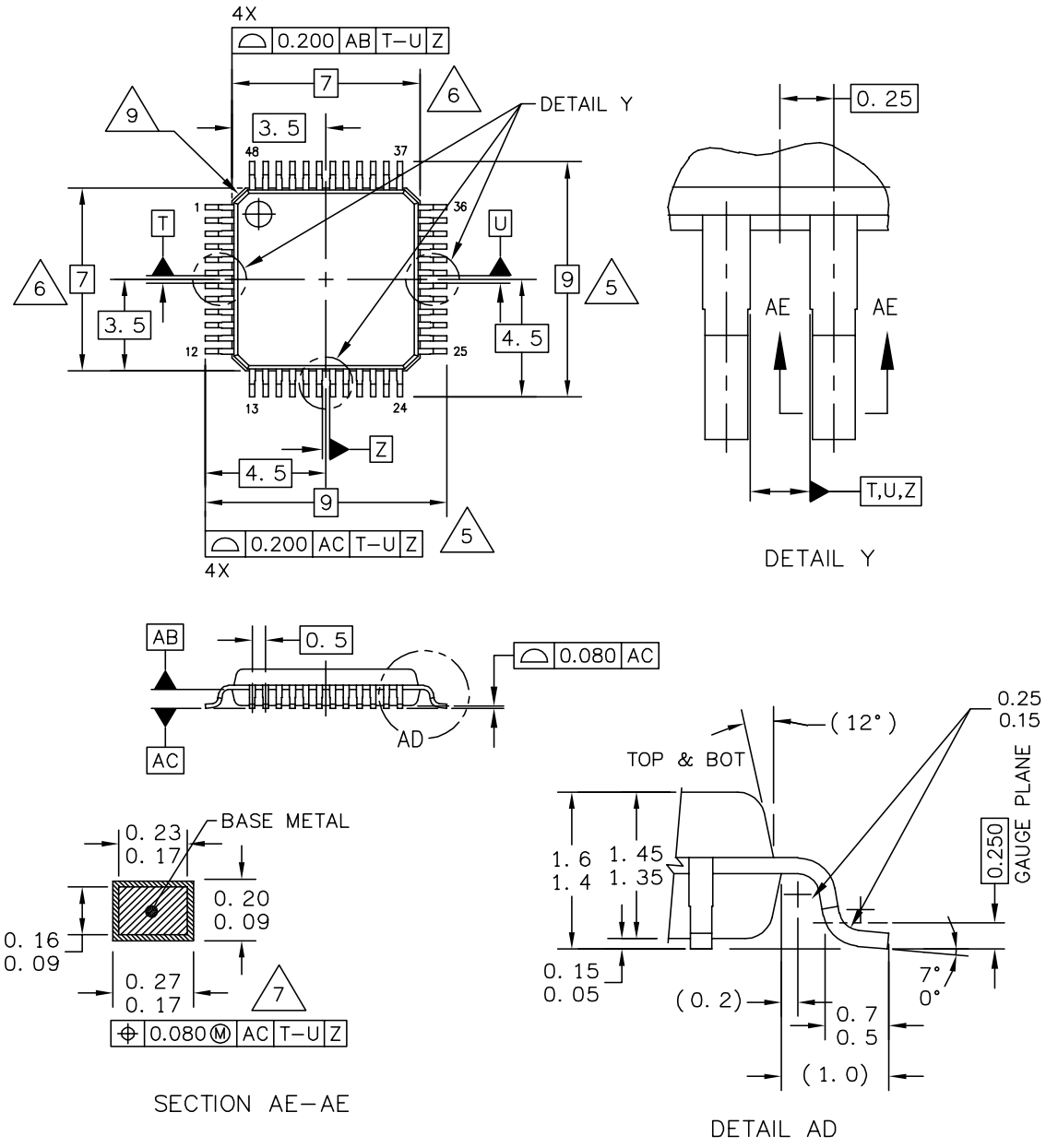
In Figure A-9 the timing diagram for slave mode with transmission format CPHA = 0 is depicted.



NOTE: Not defined

Figure A-9. SPI Slave Timing (CPHA = 0)

D.3 48 LQFP Mechanical Dimensions



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