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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

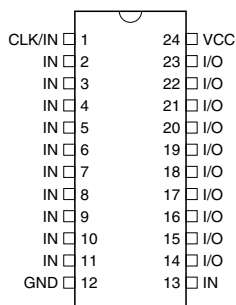
Details

| | |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status | Obsolete |
| Programmable Type | EE PLD |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 10 |
| Number of Gates | - |
| Number of I/O | 10 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 24-SO |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atf750c-10sc |

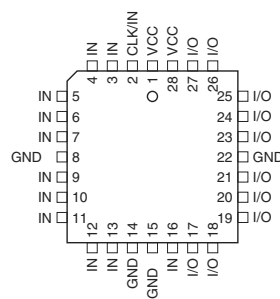
2. Pin Configurations

| Pin | Function |
|-----|------------------------|
| CLK | Clock |
| IN | Logic Inputs |
| I/O | Bi-directional Buffers |
| GND | Ground |
| VCC | +5V Supply |

2.1 DIP/SOIC/TSSOP



2.2 PLCC/LCC



Note: For PLCC, pins 1, 8, 15, and 22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to pins 8, 15, and 22.

3. Description

The ATF750C(L)s are twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations

translate into more usable gates. High-speed logic and uniform predictable delays guarantee fast in-system performance. The ATF750C(L) is a high-performance CMOS (electrically-erasable) complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology.

Each of the ATF750C(L)'s 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

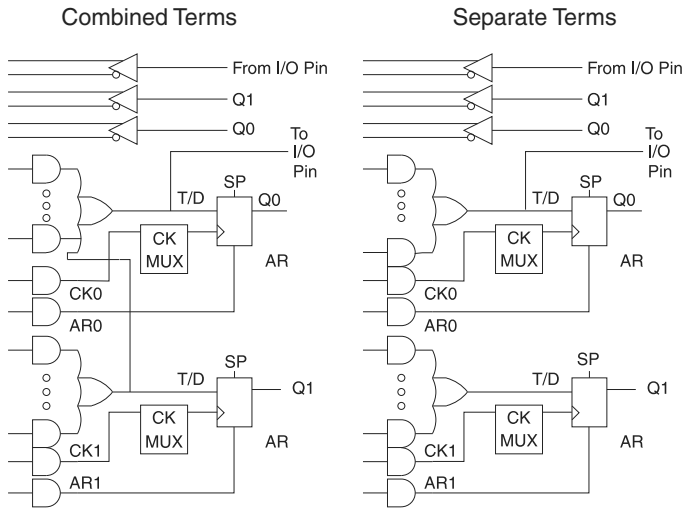
There are 171 total product terms available. There are two sum terms per output, providing added flexibility. A variable format is used to assign between four to eight product terms per sum term. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

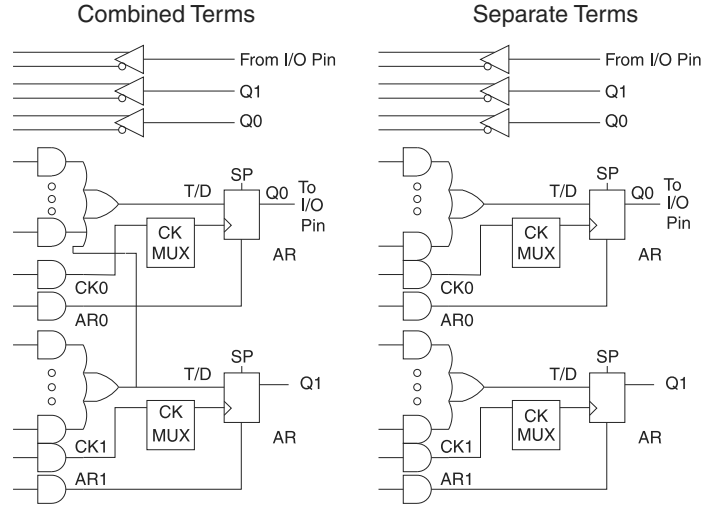
The ATF750CL is a low-power device with speeds as fast as 15 ns. The ATF750CL provides the optimum low-power CPLD solution. This device significantly reduces total system power, thereby allowing battery-powered operations.

6. Logic Options

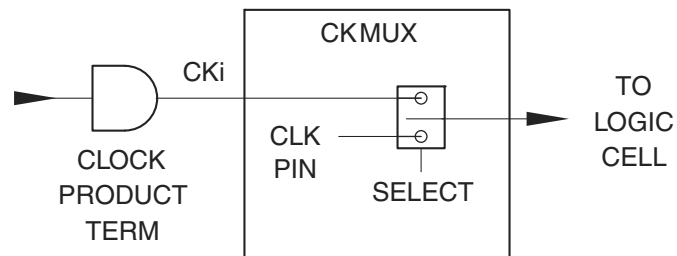
Combinatorial Output



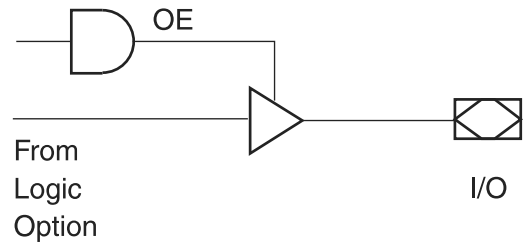
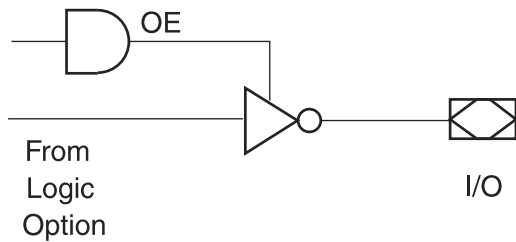
Registered Output



7. Clock Mux



8. Output Options



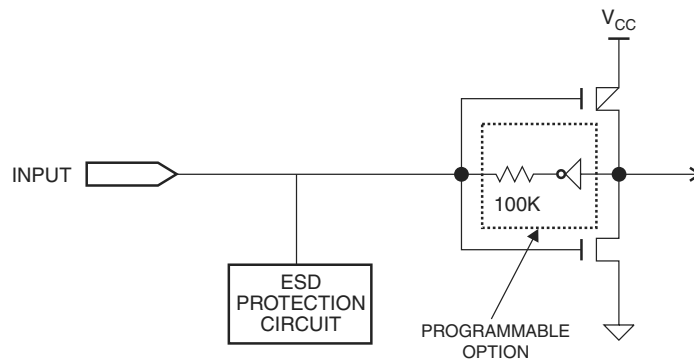
9. Bus-friendly Pin-keeper Input and I/Os

All input and I/O pins on the ATF750C(L) have programmable “pin-keeper” circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

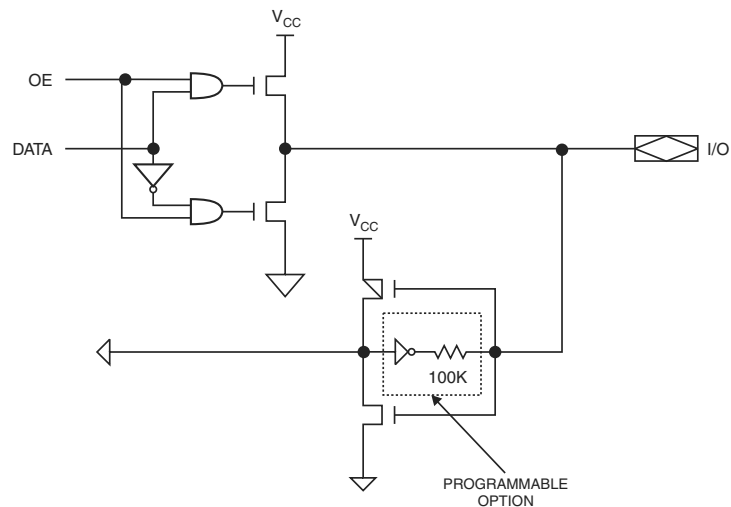
This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Enabling or disabling of the pin-keeper circuits is controlled by the device type chosen in the logic compiler device selection menu. Please refer to the software compiler table for more details. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

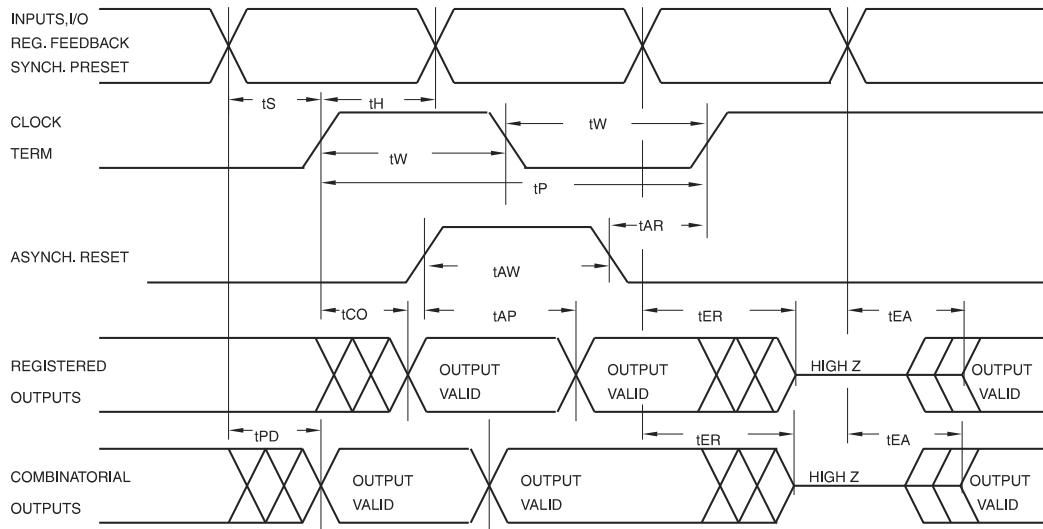
10. Input Diagram



11. I/O Diagram



15. AC Waveforms, Product Term Clock⁽¹⁾



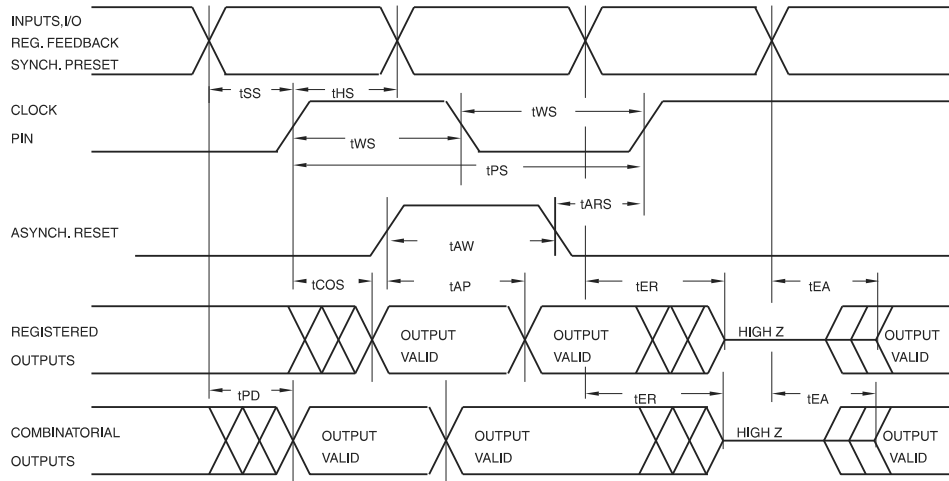
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

16. AC Characteristics, Product Term Clock⁽¹⁾

| Symbol | Parameter | -7 | | -10 | | C/CL-15 | | Units |
|-----------|-----------------------------------------------|-----|-----|-----|-----|---------|-------|-------|
| | | Min | Max | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Non-registered Output | | 7.5 | | 10 | | 15 | ns |
| t_{EA} | Input to Output Enable | | 7.5 | | 10 | | 15 | ns |
| t_{ER} | Input to Output Disable | | 7.5 | | 10 | | 15 | ns |
| t_{CO} | Clock to Output | 3 | 7.5 | 4 | 10 | 5 | 12 | ns |
| t_{CF} | Clock to Feedback | 1 | 5 | 4 | 7.5 | 5 | 9 | ns |
| t_S | Input Setup Time | 3 | | 4 | | 8/12 | | ns |
| t_{SF} | Feedback Setup Time | 3 | | 4 | | 7 | | ns |
| t_H | Hold Time | 1 | | 2 | | 5 | | ns |
| t_P | Clock Period | 7 | | 11 | | 14 | | ns |
| t_W | Clock Width | 3.5 | | 5.5 | | 7 | | ns |
| f_{MAX} | External Feedback $1/(t_S + t_{CO})$ | | 95 | | 71 | | 50/41 | MHz |
| | Internal Feedback $1/(t_{SF} + t_{CF})$ | | 125 | | 86 | | 62 | MHz |
| | No Feedback $1/(t_P)$ | | 142 | | 90 | | 71 | MHz |
| t_{AW} | Asynchronous Reset Width | 5 | | 10 | | 15 | | ns |
| t_{AR} | Asynchronous Reset Recovery Time | 3 | | 10 | | 15 | | ns |
| t_{AP} | Asynchronous Reset to Registered Output Reset | | 8 | | 12 | | 15 | ns |
| t_{SP} | Setup Time, Synchronous Preset | 4 | | 7 | | 8 | | ns |

Note: 1. See ordering information for valid part numbers.

17. AC Waveforms, Input Pin Clock⁽¹⁾

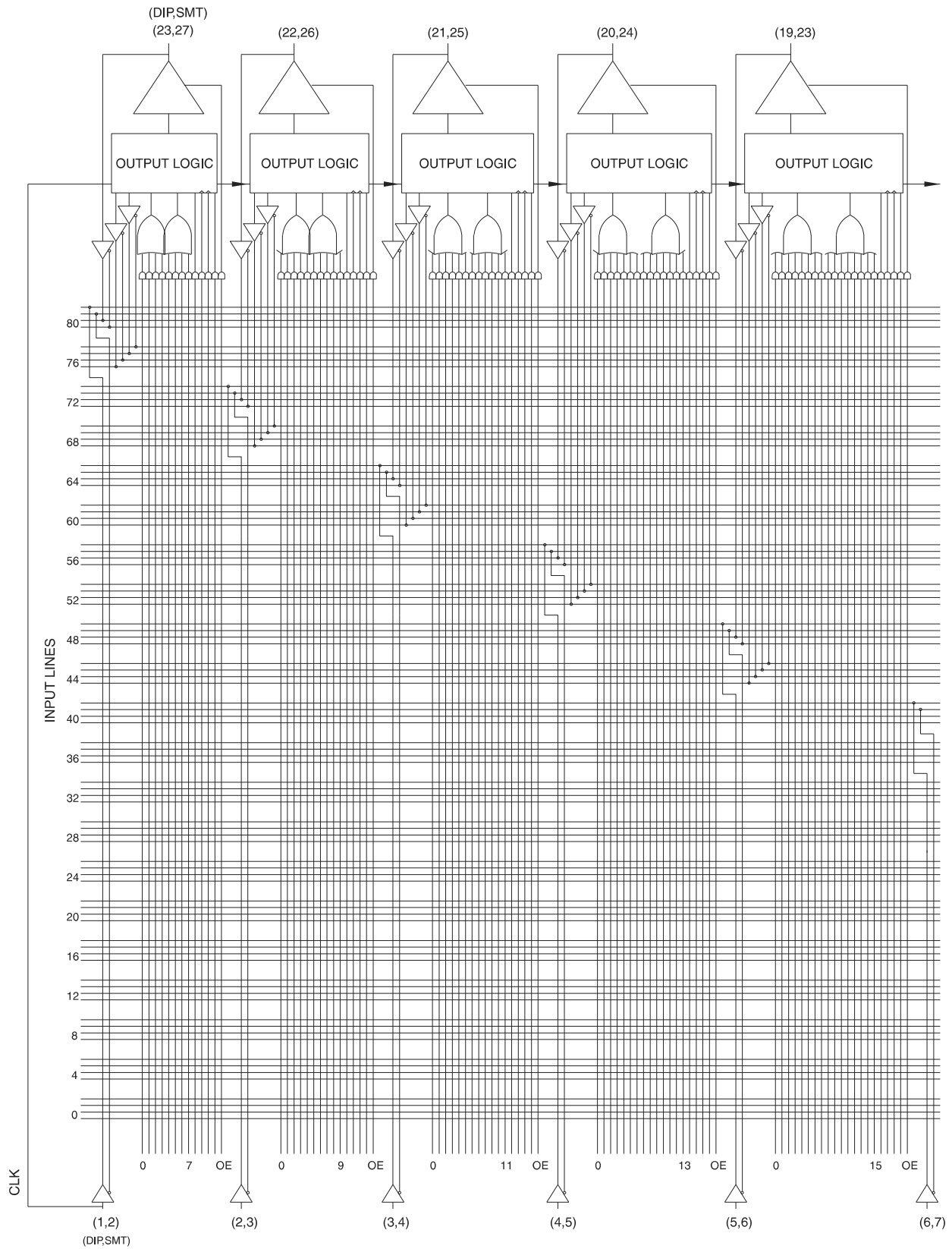


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

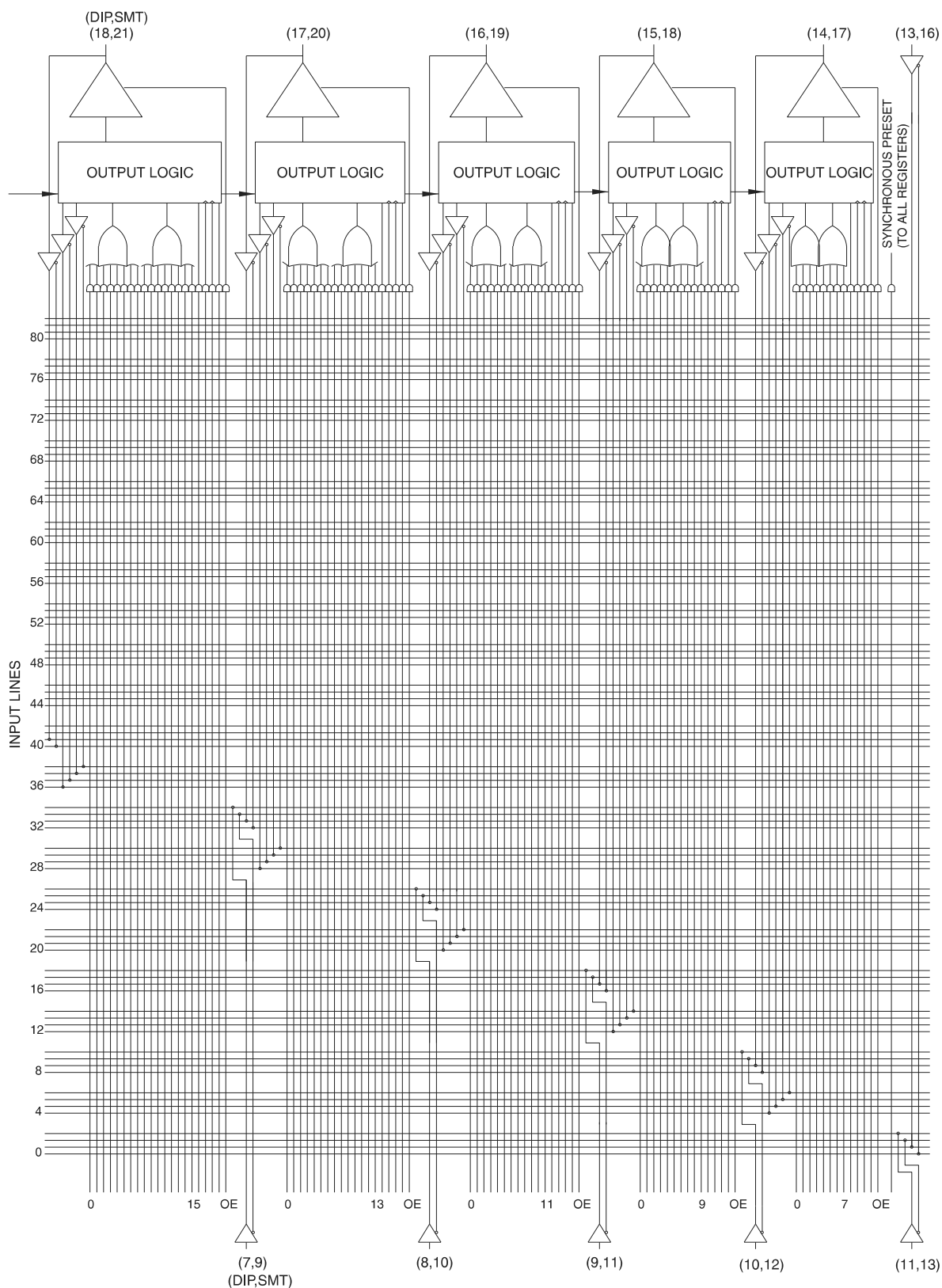
18. AC Characteristics, Input Pin Clock

| Symbol | Parameter | -7 | | -10 | | C/CL-15 | | Units |
|------------|-----------------------------------------------|-----|-----|-----|-----|---------|-------|-------|
| | | Min | Max | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Non-registered Output | | 7.5 | | 10 | | 15 | ns |
| t_{EA} | Input to Output Enable | | 7.5 | | 10 | | 15 | ns |
| t_{ER} | Input to Output Disable | | 7.5 | | 10 | | 15 | ns |
| t_{COS} | Clock to Output | 0 | 6.5 | 0 | 7 | 0 | 10 | ns |
| t_{CFS} | Clock to Feedback | 0 | 3.5 | 0 | 5 | 0 | 5.5 | ns |
| t_{SS} | Input Setup Time | 4 | | 5 | | 8/12.5 | | ns |
| t_{SFS} | Feedback Setup Time | 4 | | 5 | | 7 | | ns |
| t_{HS} | Hold Time | 0 | | 0 | | 0 | | ns |
| t_{PS} | Clock Period | 7 | | 10 | | 12 | | ns |
| t_{WS} | Clock Width | 3.5 | | 5 | | 6 | | ns |
| f_{MAXS} | External Feedback $1/(t_{SS} + t_{COS})$ | | 95 | | 83 | | 55/44 | MHz |
| | Internal Feedback $1/(t_{SFS} + t_{CFS})$ | | 133 | | 100 | | 80 | MHz |
| | No Feedback $1/(t_{PS})$ | | 142 | | 100 | | 83 | MHz |
| t_{AW} | Asynchronous Reset Width | 5 | | 10 | | 15 | | ns |
| t_{ARS} | Asynchronous Reset Recovery Time | 5 | | 10 | | 15 | | ns |
| t_{AP} | Asynchronous Reset to Registered Output Reset | | 8 | | 10 | | 15 | ns |
| t_{SPS} | Setup Time, Synchronous Preset | 5 | | 5/9 | | 11 | | ns |

19. Functional Logic Diagram ATF750C, Upper Half



20. Functional Logic Diagram ATF750C, Lower Half

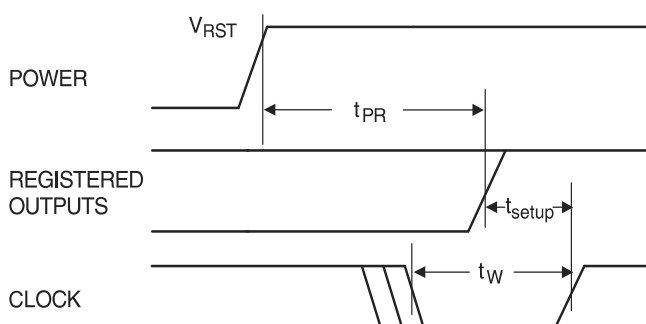


21. Power-up Reset

The registers in the ATF750C(L)s are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock terms or pin high, and
3. The clock pin, or signals from which clock terms are derived, must remain stable during t_{PR} .



| Parameter | Description | Typ | Max | Units |
|-----------|------------------------|-----|------|-------|
| t_{PR} | Power-up Reset Time | 600 | 1000 | ns |
| V_{RST} | Power-up Reset Voltage | 2.0 | 4.5 | V |

22. Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}^{(1)}$

| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 5 | 8 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 6 | 8 | pF | $V_{OUT} = 0V$ |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

23. Using the ATF750C's Many Advanced Features

The ATF750C(L)'s advanced flexibility packs more usable gates into 24 pins than any other logic device. The ATF750C(L)s start with the popular 22V10 architecture, and add several enhanced features:

- **Selectable D- and T-type Registers**

Each ATF750C(L) flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.

- **Selectable Asynchronous Clocks**

Each of the ATF750C(L)'s flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.

- **A Full Bank of Ten More Registers**

The ATF750C(L) provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.

- **Independent I/O Pin and Feedback Paths**

Each I/O pin on the ATF750C(L) has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

24. Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATF750C(L). The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

25. Software Support

All family members of the ATF750C(L) can be designed with Atmel®-WinCUPL.

Additionally, the ATF750C may be programmed to perform the ATF750(L) functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATF750 JEDEC file. In this case, the ATF750C becomes a direct replacement or speed upgrade for the ATF750. The ATF750C is a direct replacement for the ATF750(L) and the ATF750B(L).

26. Software Compiler Mode Selection

Table 26-1. Software Compiler Mode Selection

| Device | Atmel - WinCupL Device Mnemonic | Pin-keeper |
|--------------|---------------------------------|---------------------|
| ATF750C-DIP | V750C V750CPPK | Disabled Enabled |
| ATF750C-PLCC | V750LCC V750CPPKLCC | Disabled Enabled |

27. Third Party Programmer Support

Table 27-1. Third Party Programmer Support

| Device | Description |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ATF750C (V750) | V750 Cross-programming. JEDEC file compatible with standard V750 JEDEC file (total fuses in JEDEC file = 14394). The Programmer will automatically program "0"s into the User Row (UES), and disable the Pin-keeper features. The Fuse Checksum will be the same as the old ATV750/L file. This device type is recommended for customers that are directly migrating from an ATV750/L device to an ATF750C/CL device. |
| ATF750C (V750B) | V750B Cross-programming. JEDEC file compatible with standard V750B JEDEC file (total fuses in JEDEC file = 14435). The Programmer will automatically program "0"s into the User Row (UES), and disable the Pin-keeper feature. The Fuse Checksum will be the same as the old ATV750B/BL file. This device type is recommended for customers that are directly migrating from an ATV750B/BL device to an ATF750C/CL device. |
| ATF750C | Programming of User Row (UES) bits supported and Pin-keeper bit is user-programmable. (Total fuses in JEDEC file = 14504). This is the default device type and is recommended for users that have re-compiled their source design files to specifically target the ATF750C device. |

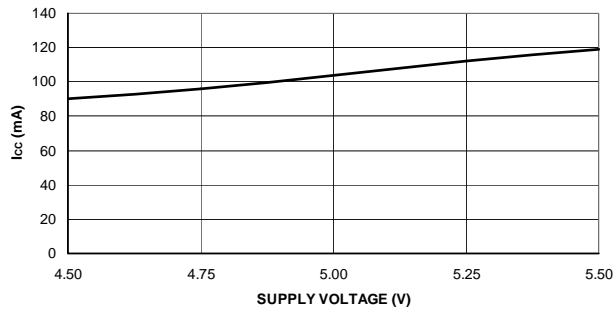
Note: 1. The ATF750C has 14,504 JEDEC fuses.

28. Security Fuse Usage

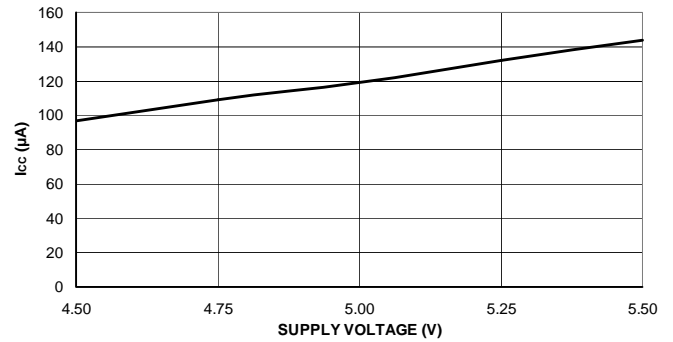
A single fuse is provided to prevent unauthorized copying of the ATF750C(L) fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

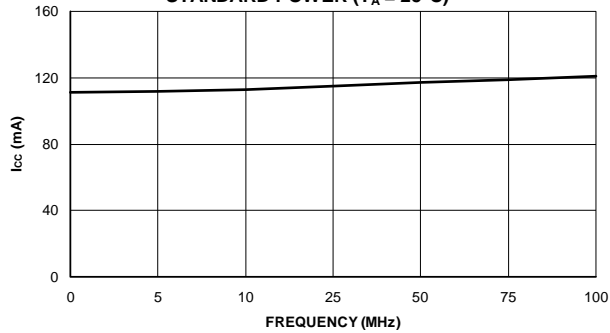
**ATF750C SUPPLY CURRENT VS.
SUPPLY VOLTAGE ($T_A = 25^\circ\text{C}$)**



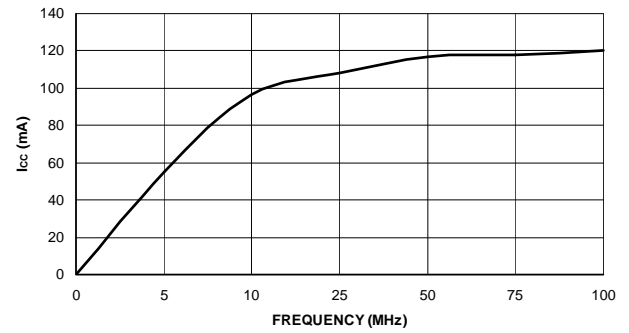
**ATF750CL SUPPLY CURRENT
VS. SUPPLY VOLTAGE ($T_A = 25^\circ\text{C}$)**



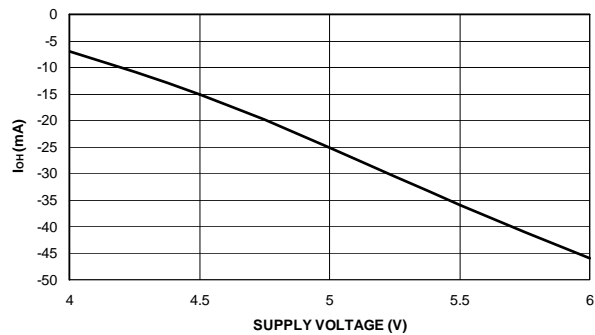
**SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER ($T_A = 25^\circ\text{C}$)**



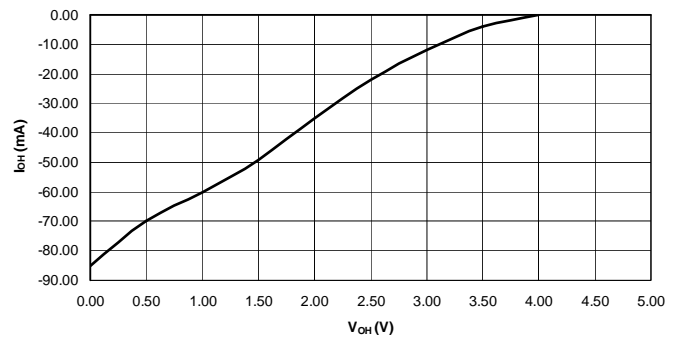
**SUPPLY CURRENT VS. FREQUENCY
LOW-POWER ("L") VERSION ($T_A = 25^\circ\text{C}$)**



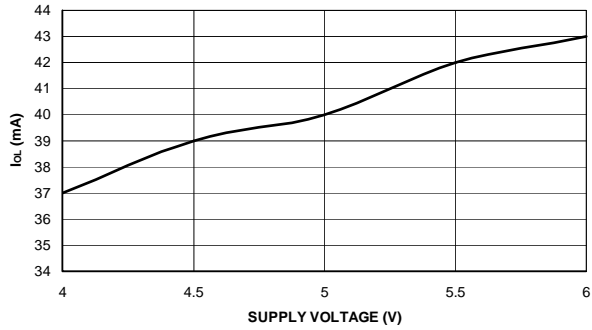
**ATF750C/CL OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE ($V_{OH} = 2.4\text{V}$)**



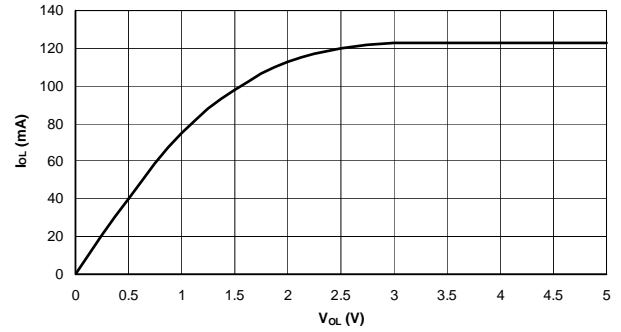
**ATF750C/CL OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)**



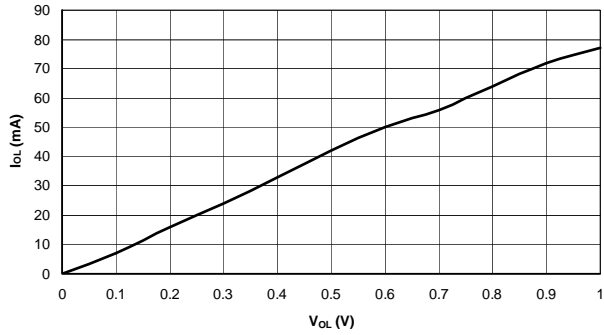
**ATF750C/CL OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE ($V_{OL} = 0.5V$)**



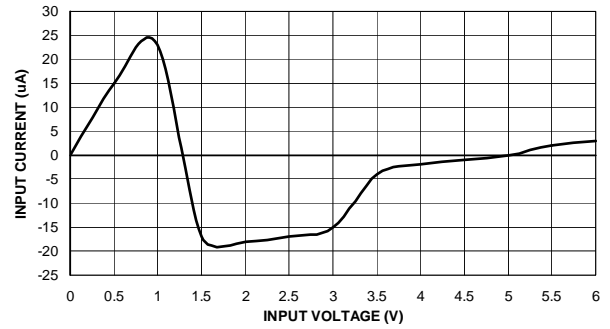
**ATF750C/CL OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE ($V_{CC} = 5V$, $T_A = 25^\circ C$)**



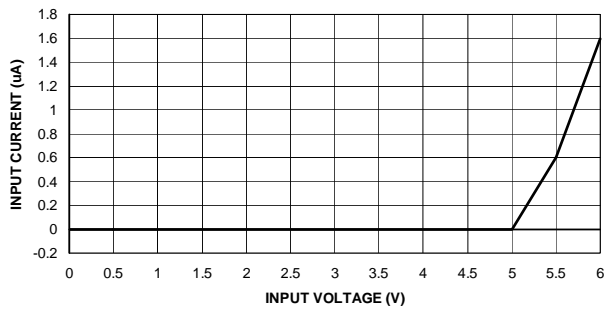
**ATF750C/CL OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE ($V_{CC} = 5V$, $T_A = 25^\circ C$)**



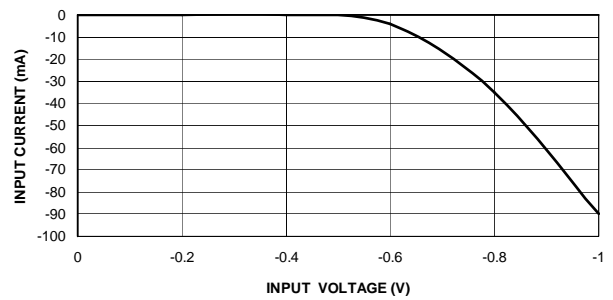
**ATF750C/CL INPUT CURRENT VS. INPUT VOLTAGE
($V_{CC} = 5V$, $T_A = 25^\circ C$)**



**ATF750C/CL INPUT CURRENT VS. INPUT VOLTAGE
($V_{CC} = 5V$, $T_A = 25^\circ C$)
WITHOUT PIN-KEEPER**



**ATF750C/CL INPUT CLAMP CURRENT
VS. INPUT VOLTAGE ($V_{CC} = 5V$, $T_A = 35^\circ C$)**



30. ATF750C(L) Military Ordering Information

| t_{PD} (ns) | t_{COS} (ns) | Ext. f_{MAXS} (MHz) | Ordering Code | Package | Operation Range |
|------------------|-------------------|-----------------------------|----------------------------------------------------------------------------|----------------------------|--------------------------------------------------------------|
| 10 | 7 | 83 | ATF750C-10GM/883 ATF750C-10NM/883 5962-0720101MLA 5962-0720101M3A | 24D3 28L 24D3 28L | Military/883 (-55°C to 125°C) Class B, Fully Compliant |
| 15 | 10 | 55 | ATF750C-15GM/883 ATF750C-15NM/883 5962-0720102MLA 5962-0720102M3A | 24D3 28L 24D3 28L | |

Note: 1. Special order only: TSSOP package requires special thermal management.

31. ATF750C(L) Green Package Options (Pb/Halide-free/RoHS Compliant)

| t_{PD} (ns) | t_{COS} (ns) | Ext. f_{MAXS} (MHz) | Ordering Code | Package | Operation Range |
|------------------|-------------------|-----------------------------|------------------------------------------------------------------|---------------------------|-------------------------------|
| 7.5 | 6.5 | 95 | ATF750C-7JX ATF750C-7PX ATF750C-7SX | 28J 24P3 24S | Commercial (0°C to 70°C) |
| 10 | 7 | 83 | ATF750C-10JU ATF750C-10PU ATF750C-10SU ATF750C-10XU | 28J 24P3 24S 24X | Industrial (-40°C to 85°C) |
| 15 | 10 | 44 | ATF750CL-15JU ATF750CL-15PU ATF750CL-15SU ATF750CL-15XU | 28J 24P3 24S 24X | Industrial (-40°C to 85°C) |

32. Using “C” Product for Industrial

To use commercial product for industrial ranges, down-grade one speed grade from the Industrial to the Commercial device (7 ns “X” = 10 ns “U”) and de-rate power by 30%.

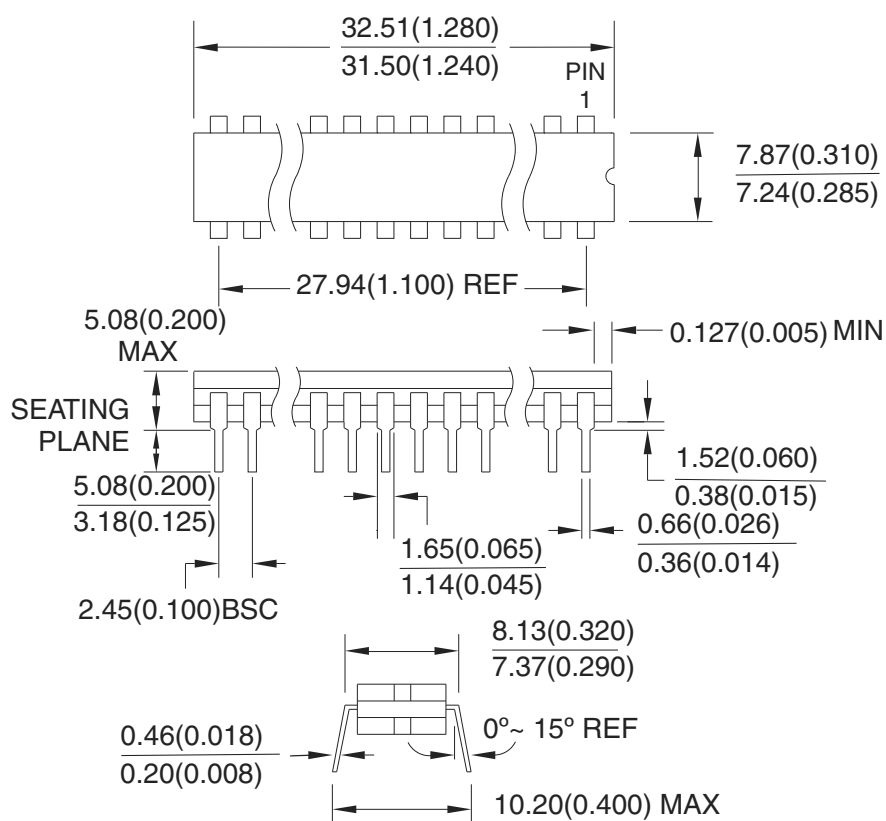
| Package Type | |
|--------------------------|-------------------------------------------------------------------------|
| 24D3 | 24-lead, 0.300" Wide, Non-windowed Ceramic Dual Inline Package (CerDIP) |
| 28J | 28-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 28L | 28-pad, Non-Windowed Ceramic Leadless Chip Carrier (LCC) |
| 24P3 | 24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 24S | 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 24X⁽¹⁾ | 24-lead, 0.173" Wide, Thin Shrink Small Outline (TSSOP) |

Note: 1. Special order only: TSSOP package requires special thermal management.

33. Packaging Information

33.1 24D3 – CerDIP

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 D-9 Config A (Glass Sealed)

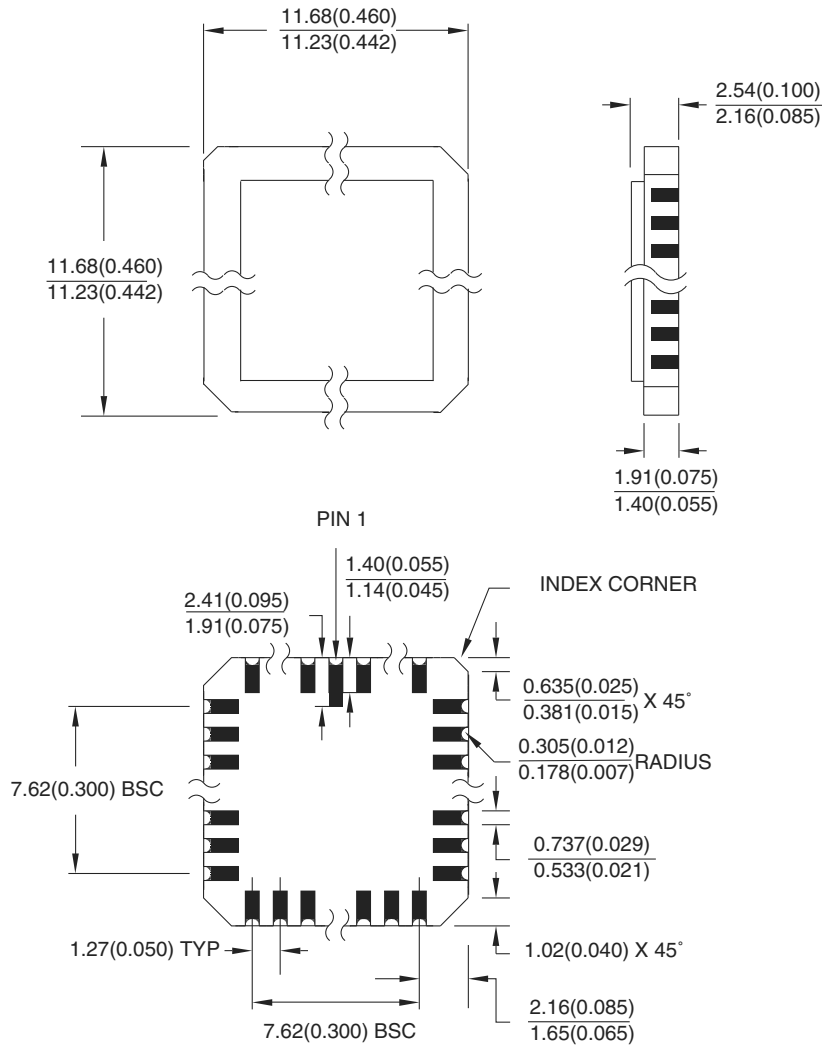


10/21/03

| | | | |
|--------------------------------------------|-----------------------------------------------------------------------------------------------------------|----------------------------|------------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 24D3 , 24-lead, 0.300" Wide. Non-windowed, Ceramic Dual Inline Package (Cerdip) | DRAWING NO. 24D3 | REV. B |
|--------------------------------------------|-----------------------------------------------------------------------------------------------------------|----------------------------|------------------|

33.3 28L – LCC

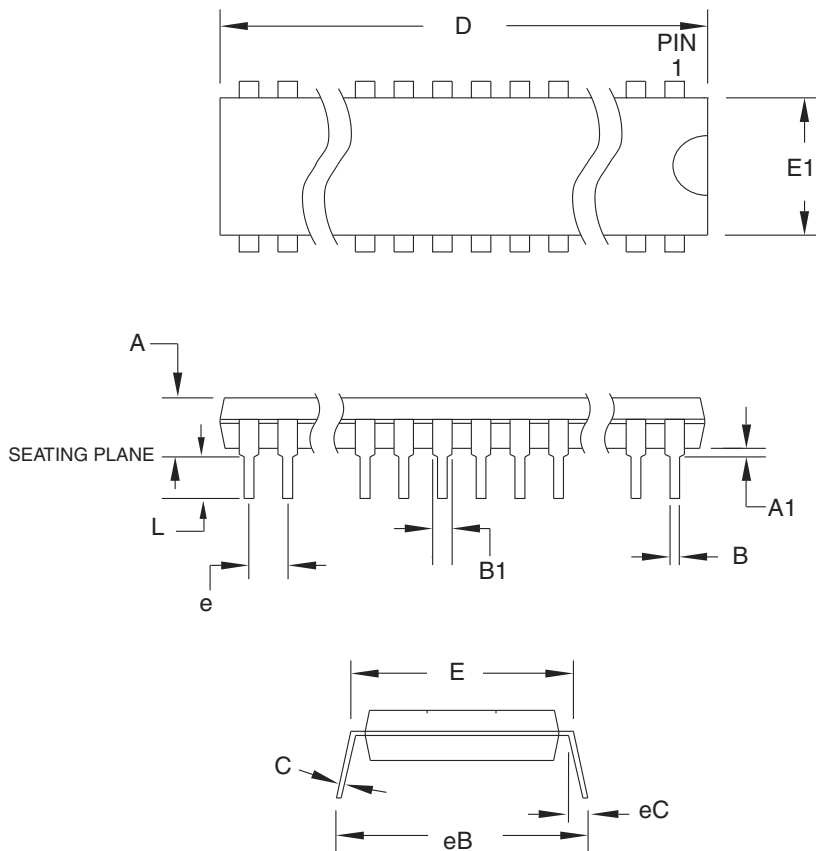
Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 C-4



10/21/03

| | | | |
|--------------------------------------------|---------------------------------------------------------------------------------------------|---------------------------|------------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 28L , 28-pad, Non-windowed, Ceramic Lid, Leadless Chip Carrier (LCC) | DRAWING NO. 28L | REV. B |
|--------------------------------------------|---------------------------------------------------------------------------------------------|---------------------------|------------------|

33.4 24P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | – | – | 5.334 | |
| A1 | 0.381 | – | – | |
| D | 31.623 | – | 32.131 | Note 2 |
| E | 7.620 | – | 8.255 | |
| E1 | 6.096 | – | 7.112 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.270 | – | 1.651 | |
| L | 2.921 | – | 3.810 | |
| C | 0.203 | – | 0.356 | |
| eB | – | – | 10.922 | |
| eC | 0.000 | – | 1.524 | |
| e | 2.540 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-001, Variation AF.
 2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

6/1/04



2325 Orchard Parkway
San Jose, CA 95131

TITLE

24P3, 24-lead (0.300"/7.62 mm Wide) Plastic Dual
Inline Package (PDIP)

DRAWING NO.

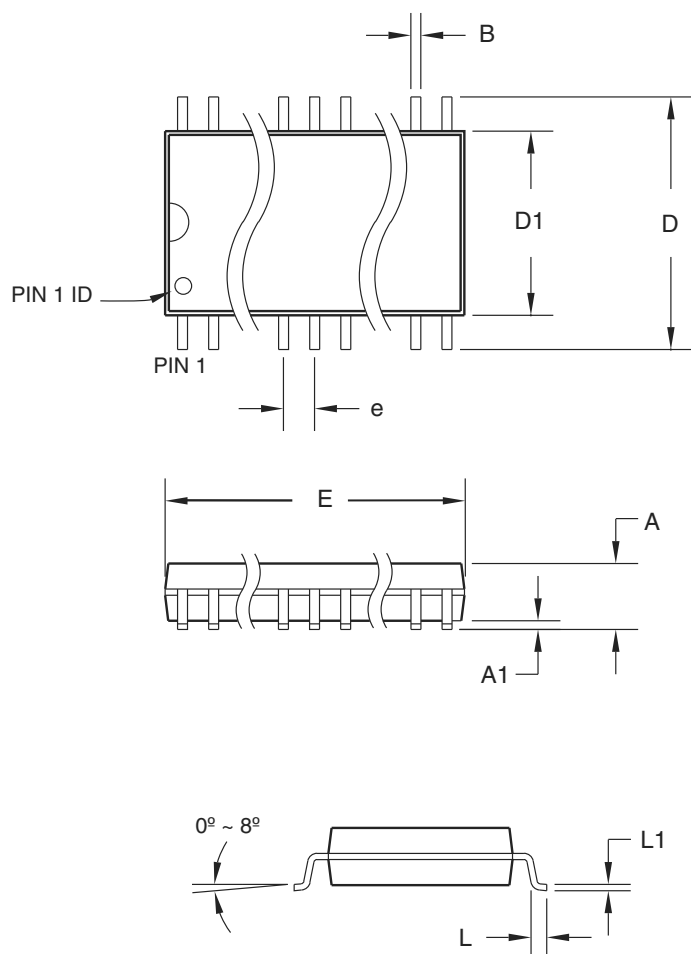
24P3

REV.

D



33.5 24S – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

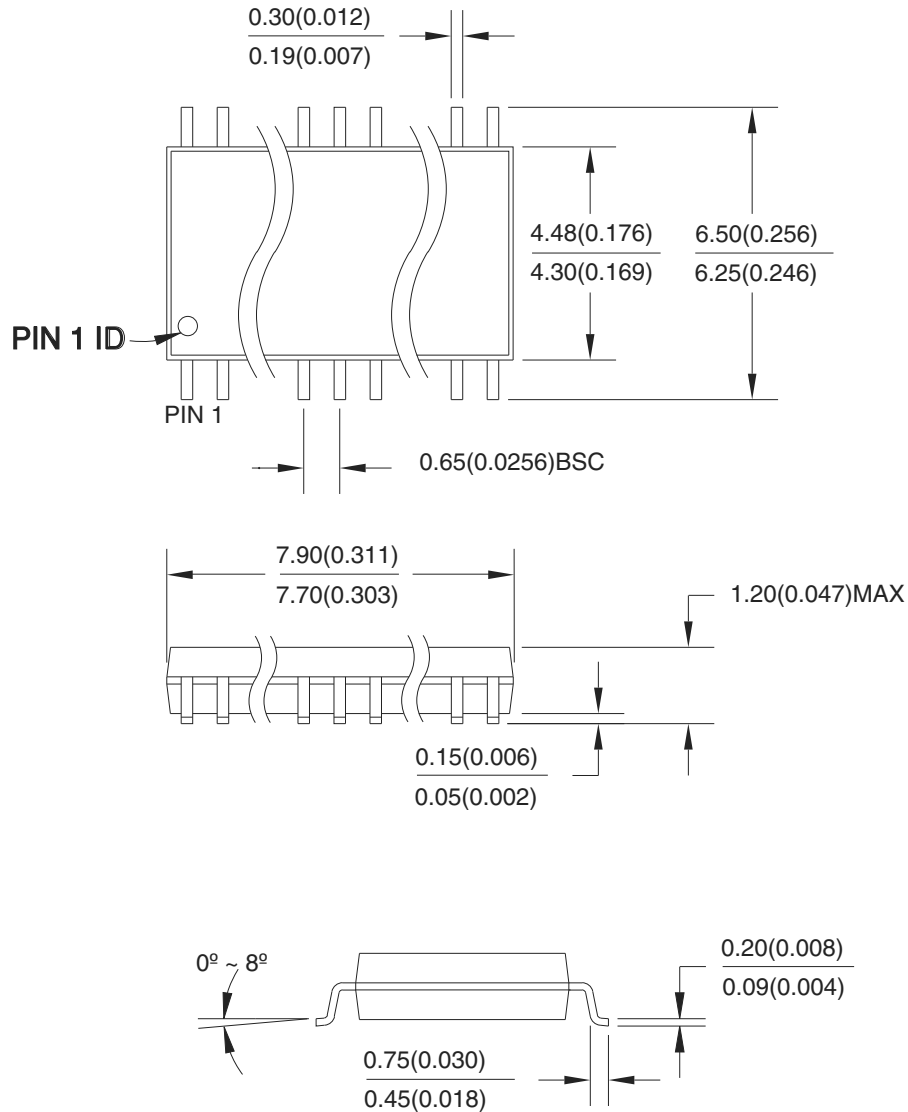
| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|-------|------|
| A | – | – | 2.65 | |
| A1 | 0.10 | – | 0.30 | |
| D | 10.00 | – | 10.65 | |
| D1 | 7.40 | – | 7.60 | |
| E | 15.20 | – | 15.60 | |
| B | 0.33 | – | 0.51 | |
| L | 0.40 | – | 1.27 | |
| L1 | 0.23 | – | 0.32 | |
| e | 1.27 BSC | | | |

06/17/2002

| | | | |
|--------------------------------------------|------------------------------------------------------------------------------------------|---------------------------|------------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 24S, 24-lead (0.300" body) Plastic Gull Wing Small Outline (SOIC) | DRAWING NO. 24S | REV. B |
|--------------------------------------------|------------------------------------------------------------------------------------------|---------------------------|------------------|

33.6 24X – TSSOP

Dimensions in Millimeter and (Inches)*
JEDEC STANDARD MO-153 AD
Controlling dimension: millimeters



04/11/2001

| | | | |
|--------------------------------------------|------------------------------------------------------------------------------------------------------------|---------------------------|------------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 24X , 24-lead (4.4 mm body width) Plastic Thin Shrink Small Outline Package (TSSOP) | DRAWING NO. 24X | REV. A |
|--------------------------------------------|------------------------------------------------------------------------------------------------------------|---------------------------|------------------|

34. Revision History

| Revision Level – Release Date | History |
|-------------------------------|----------------------------------------------------------------------------------------------------------------|
| K – July 2007 | Added military-grade devices. Added fully-green RoHS-compliant devices in select speed grades and packages. |
| L – November 2008 | Removed commercial grade leaded package options. |



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