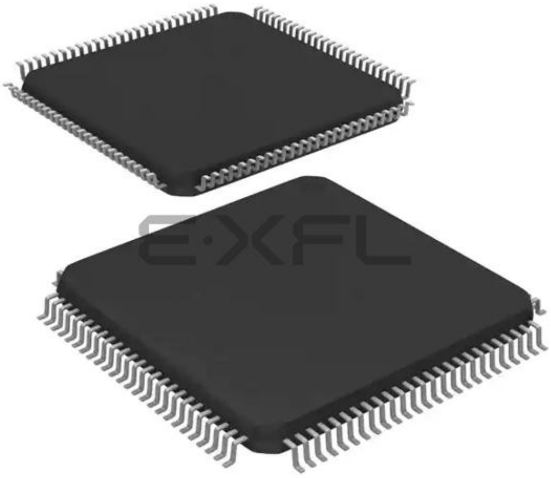

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg980f256-qfp100

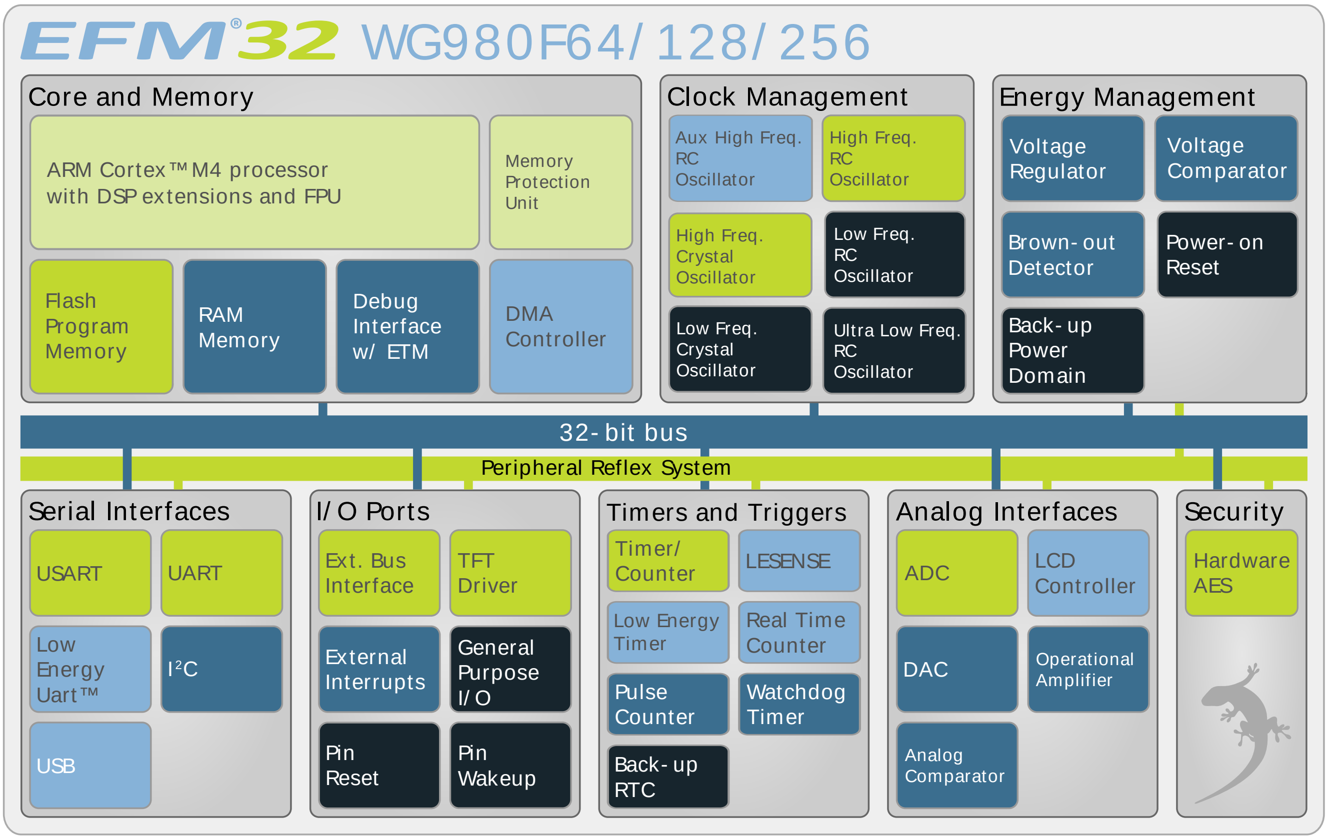
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG980 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG980 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

Module	Configuration	Pin Connections
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	81 pins	Available pins are shown in Table 4.3 (p. 70)
LCD	Full configuration	LCD_SEG[33:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

2.3 Memory Map

The *EFM32WG980* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG980 Memory Map with largest RAM and Flash sizes

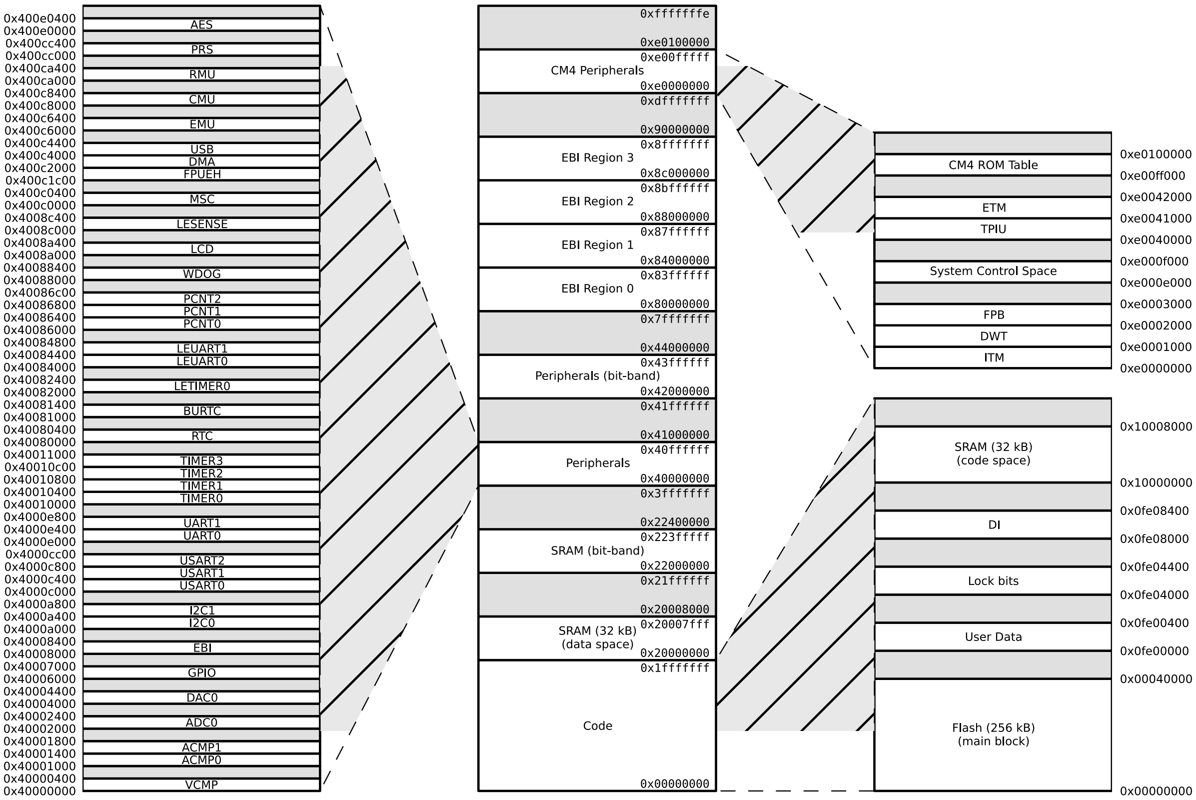


Figure 3.3. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz

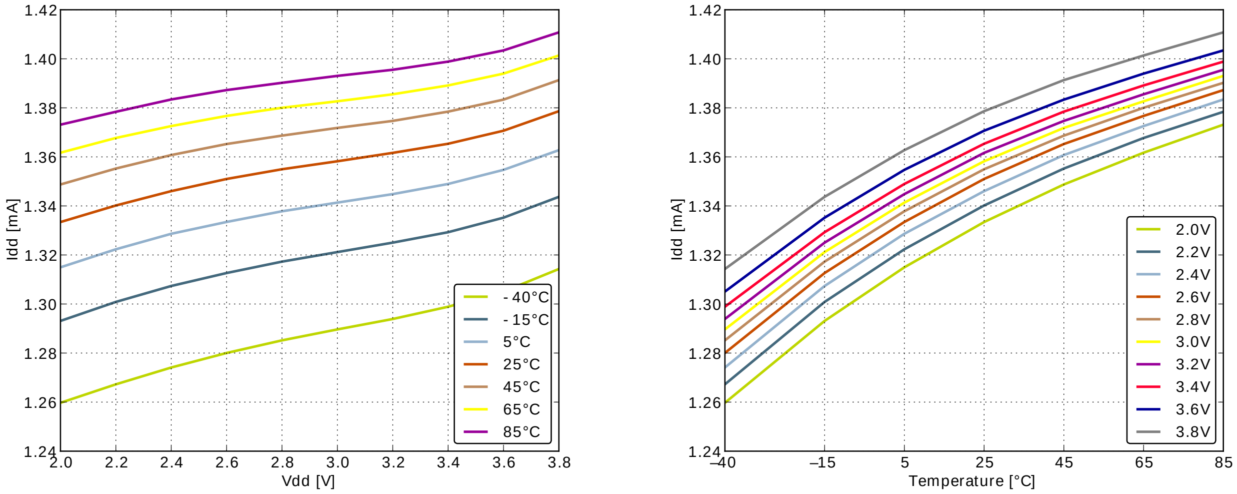


Figure 3.4. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz

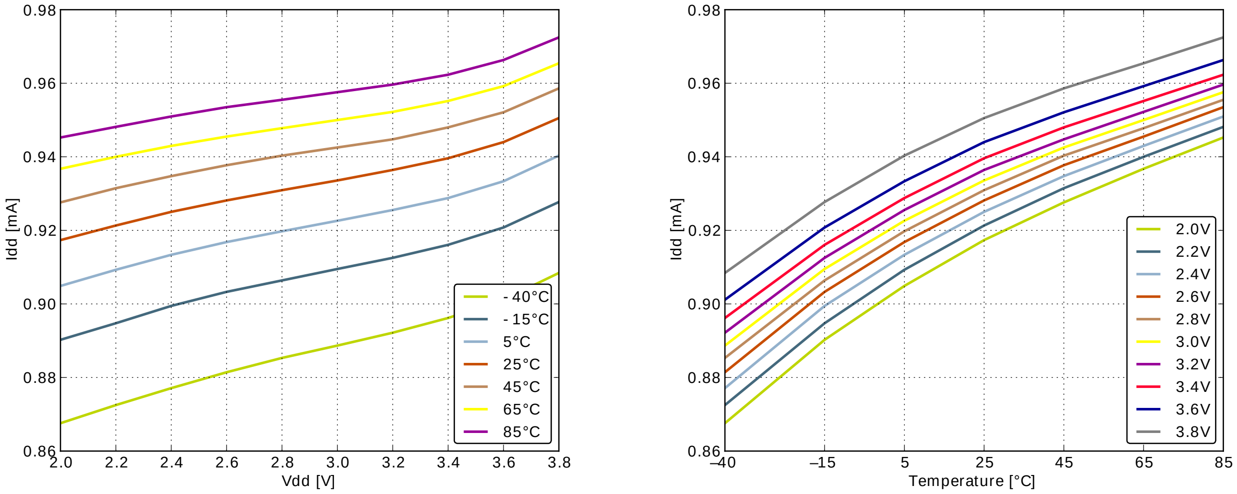
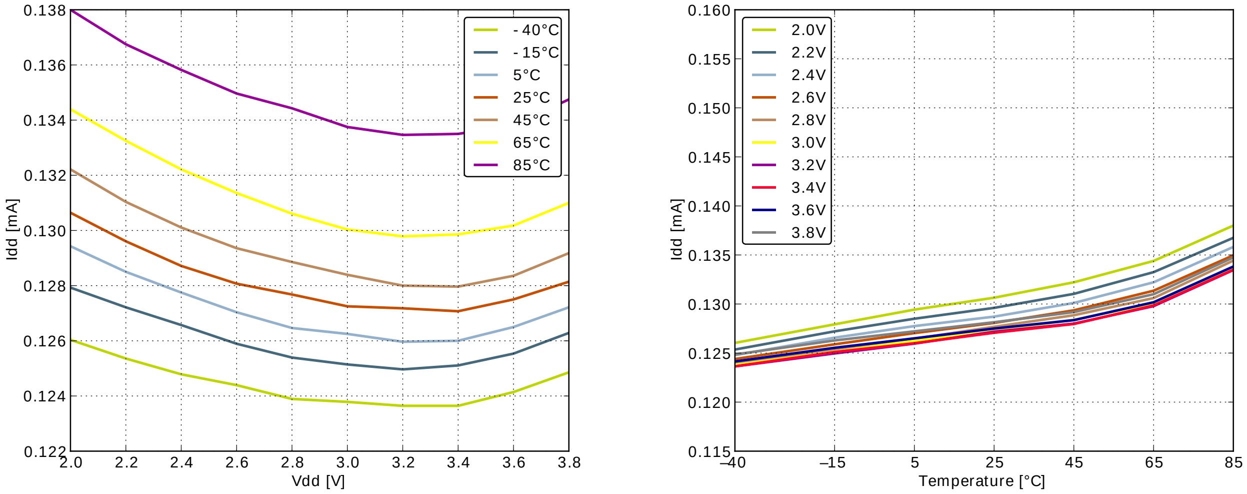
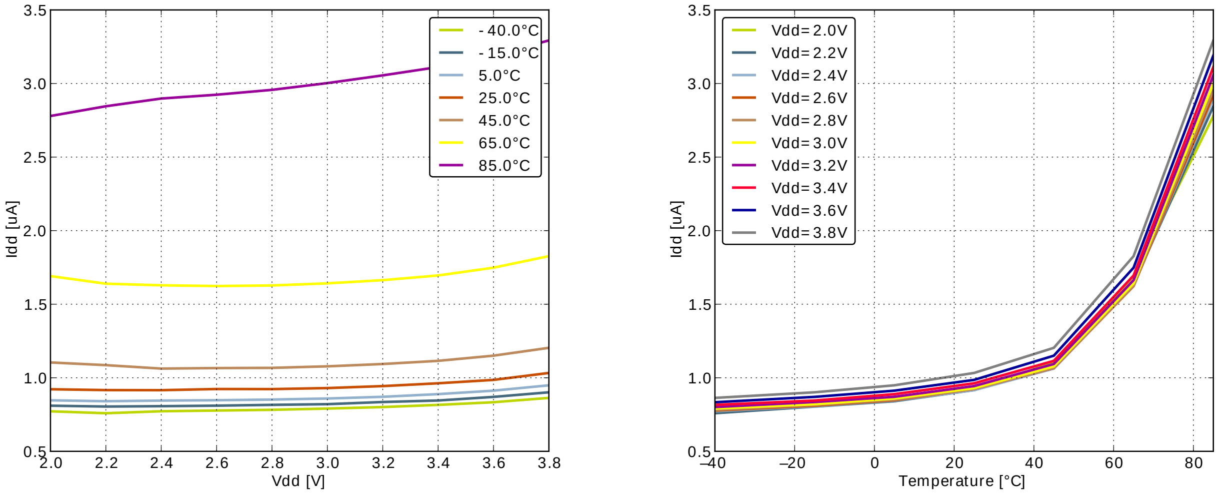


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 1.2MHz



3.4.2 EM2 Current Consumption

Figure 3.8. EM2 current consumption. RTC[1] prescaled to 1kHz, 32.768 kHz LFRCO.



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[1] Using backup RTC.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V_{DD}			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V_{DD}		V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V_{DD}	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		±0.1	±100	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.98 - 3.8 V	0.10V_{DD}			V

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1] See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.10. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2	9	mV
		After calibration, differential		2		mV
DNL_{DAC}	Differential non-linearity			±1		LSB
INL_{DAC}	Integral non-linearity			±5		LSB
MC_{DAC}	No missing codes			12		bits

[1] Measured with a static input code and no loading on the output.

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.17. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OPAMP}	Active Current	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		370	460	µA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		95	135	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	25	µA
G_{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW_{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM_{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C_L=75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
R_{INPUT}	Input Resistance			100		Mohm
R_{LOAD}	Load Resistance		200			Ohm
I_{LOAD_DC}	DC Load Current				11	mA
V_{INPUT}	Input Voltage	OPAxHCMDIS=0	V_{SS}		V_{DD}	V
		OPAxHCMDIS=1	V_{SS}		V_{DD}-1.2	V
V_{OUTPUT}	Output Voltage		V_{SS}		V_{DD}	V
V_{OFFSET}	Input Offset Voltage	Unity Gain, $V_{SS}<V_{in}<V_{DD}$, OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, $V_{SS}<V_{in}<_{DD}$-1.2, OPAxHCMDIS=1		1		mV
V_{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR_{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/µs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/µs
N_{OPAMP}	Voltage Noise	V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0		101		µV_{RMS}
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1		141		µV_{RMS}

Table 3.20. EBI Write Enable Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_WEn} [1,2,3,4]	Output hold time, from trailing EBI_WEn/ EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	-6.00 + (WRHOLD * $t_{HFCORECLK}$)			ns
t_{OSU_WEn} [1,2,3,4,5]	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/ EBI_NANDWEn edge	-14.00 + (WRSETUP * $t_{HFCORECLK}$)			ns
t_{WIDTH_WEn} [1,2,3,4,5]	EBI_WEn/EBI_NANDWEn pulse width	-7.00 + ((WRSTRB +1) * $t_{HFCORECLK}$)			ns

[1] Applies for all addressing modes (figure only shows D16 addressing mode)

[2] Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * $t_{HFCLKNODIV}$.

Figure 3.39. EBI Address Latch Enable Related Output Timing

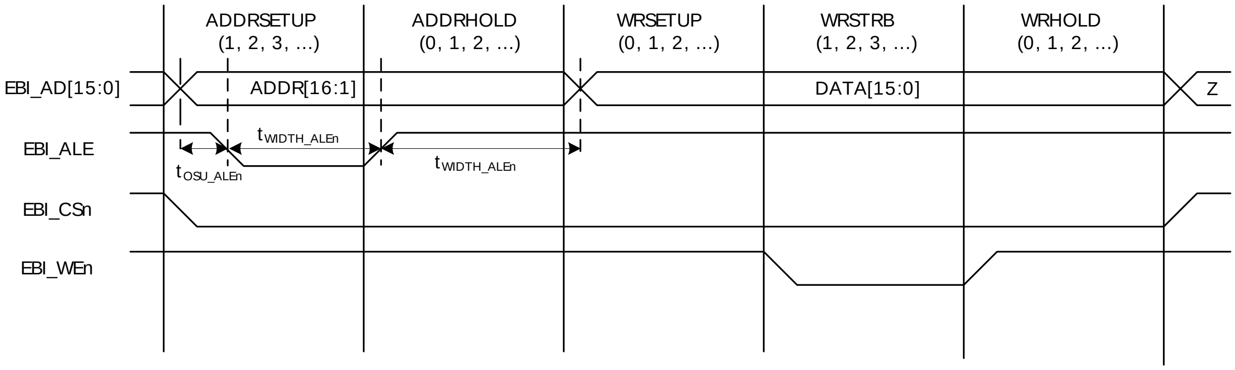


Table 3.21. EBI Address Latch Enable Related Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_ALEn} [1,2,3,4]	Output hold time, from trailing EBI_ALE edge to EBI_AD invalid	-6.00 + (ADDRHOLD[5] * $t_{HFCORECLK}$)			ns
t_{OSU_ALEn} [1,2,4]	Output setup time, from EBI_AD valid to leading EBI_ALE edge	-13.00 + (0 * $t_{HFCORECLK}$)			ns
t_{WIDTH_ALEn} [1,2,3,4]	EBI_ALEn pulse width	-7.00 + (ADDRSETUP+1) * $t_{HFCORECLK}$)			ns

[1] Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)

[2] Applies for all polarities (figure only shows active low signals)

[3] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of tOH_ALEn by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

Table 3.28. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and a START condition	0.5			µs

[1] For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.18 USART SPI

Figure 3.43. SPI Master Timing

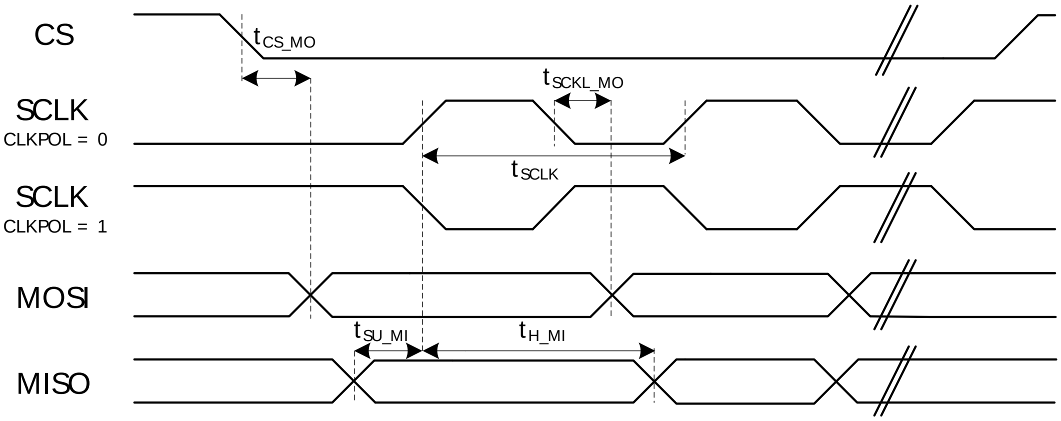


Table 3.29. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPERCLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	36.00			ns
t_{H_MI} [1] [2]	MISO hold time		-6.00			ns

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32WG980.

4.1 Pinout

The *EFM32WG980* pinout is shown in Figure 4.1 (p. 58) and Table 4.1 (p. 58). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32WG980 Pinout (top view, not to scale)

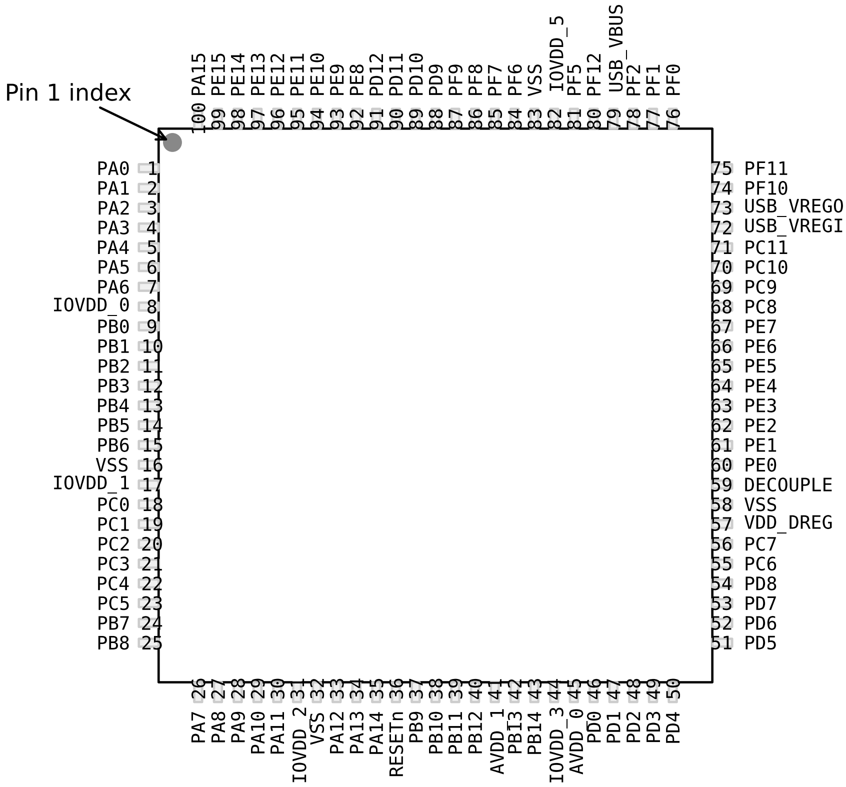


Table 4.1. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2	LCD_SEG15	EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
						ETM_TD0 #3
4	PA3	LCD_SEG16	EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
5	PA4	LCD_SEG17	EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
6	PA5	LCD_SEG18	EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6	LCD_SEG19	EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
8	IOVDD_0	Digital IO power supply 0.				
9	PB0	LCD_SEG32	EBI_A16 #0/1/2	TIM1_CC0 #2		
10	PB1	LCD_SEG33	EBI_A17 #0/1/2	TIM1_CC1 #2		
11	PB2	LCD_SEG34	EBI_A18 #0/1/2	TIM1_CC2 #2		
12	PB3	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
13	PB4	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
14	PB5	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
15	PB6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
16	VSS	Ground				
17	IOVDD_1	Digital IO power supply 1.				
18	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
19	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
20	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
21	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
22	PC4	ACMP0_CH4 DAC0_P0 / OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
23	PC5	ACMP0_CH5 DAC0_N0 / OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
24	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
25	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
26	PA7	LCD_SEG35	EBI_CSTFT #0/1/2			
27	PA8	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
28	PA9	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
29	PA10	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
30	PA11	LCD_SEG39	EBI_HSNC #0/1/2			

Alternate	LOCATION							
Functionality	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**Description**
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX
BOOT_TX	PE10							Bootloader TX
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE		PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn		PF8						External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32WG980* is shown in Table 4.3 (p. 70). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	-	-	-	-	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	-	-	PF2	PF1	PF0

4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32WG980* is shown in Figure 4.2 (p. 70) .

Figure 4.2. Opamp Pinout

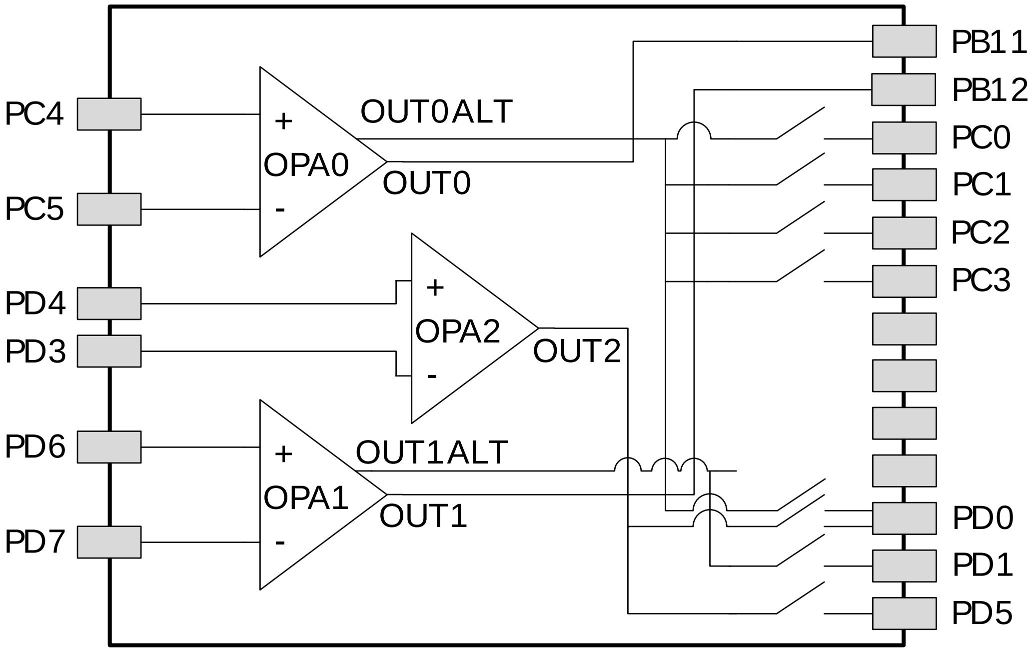


Figure 5.2. LQFP100 PCB Solder Mask

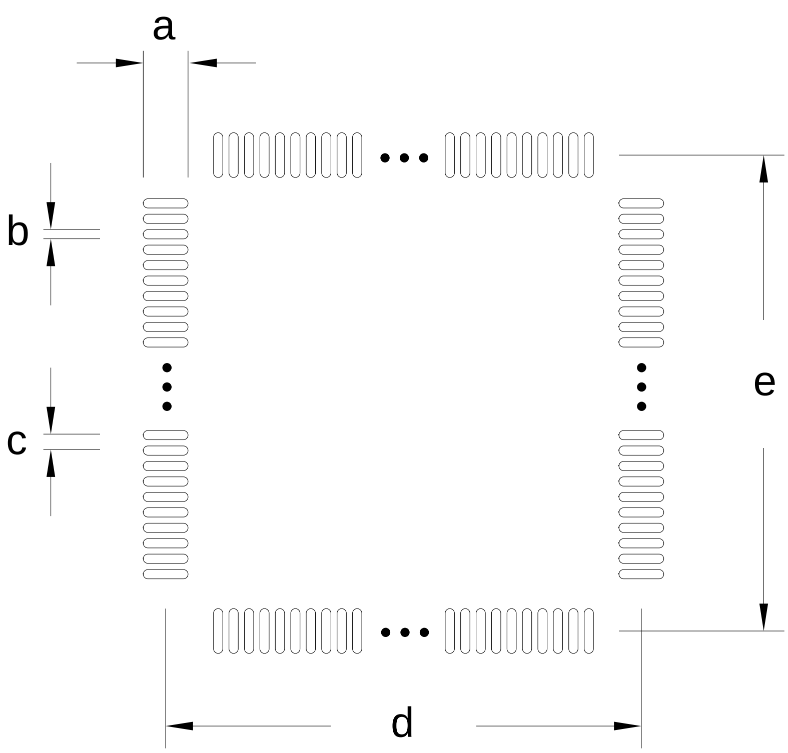


Table 5.2. QFP100 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.57
b	0.42
c	0.50
d	15.40
e	15.40

Figure 5.3. LQFP100 PCB Stencil Design

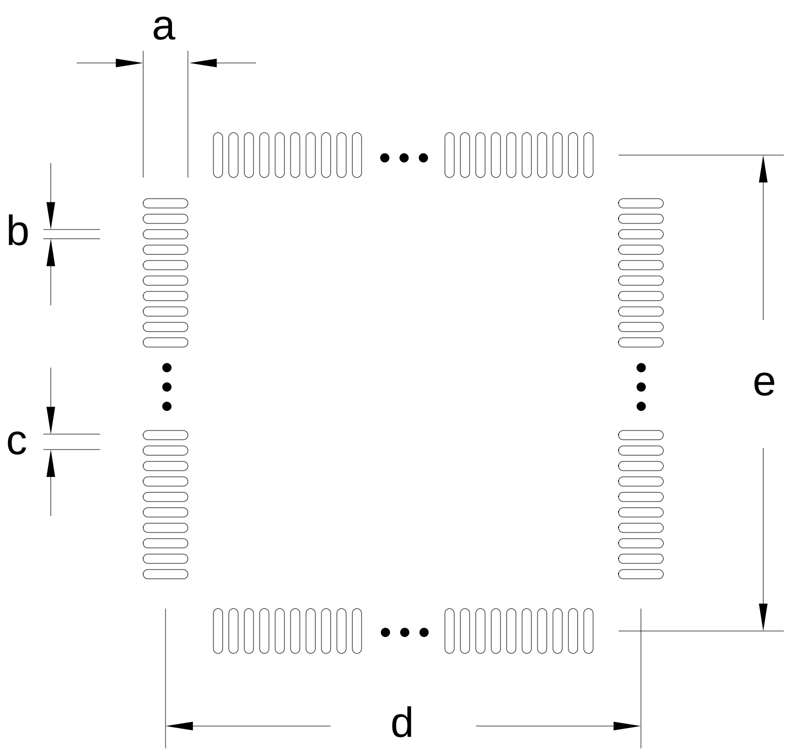


Table 5.3. QFP100 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.35
b	0.20
c	0.50
d	15.40
e	15.40

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 71) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

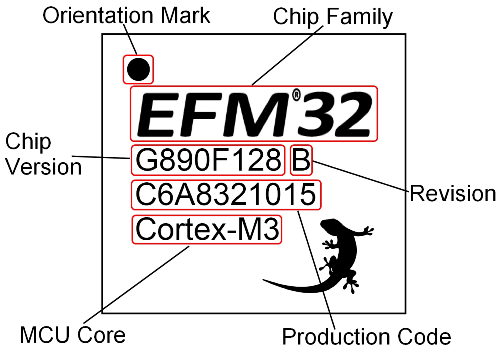
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 76) .

6.3 Errata

Please see the errata document for EFM32WG980 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

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