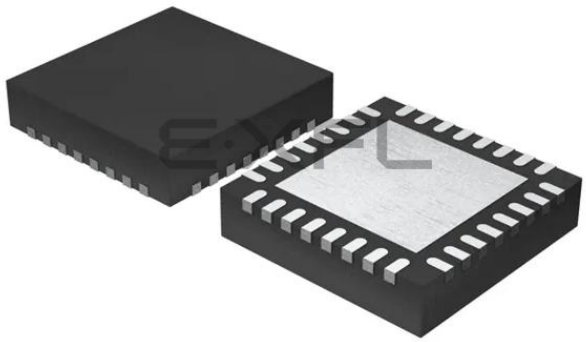


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 56800EX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3K x 16 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 6x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount, Wettable Flank |
| Package / Case | 32-VFQFN Exposed Pad |
| Supplier Device Package | 32-HVQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82723vfm |

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging
- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except for RESETB pin which is a 3.3 V pin only)
  - Operation ambient temperature: V temperature option: -40°C to 105°C
  - Operation ambient temperature: M temperature option: -40°C to 125°C
- 64-pin LQFP, 48-pin LQFP, 32-pin QFN, and 32-pin LQFP packages

# Table of Contents

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

## 1.3 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode
- Operation ambient temperature:
  V Temperature option:-40 ºC to 105ºC
  M Temperature option:-40 ºC to 125ºC
- Single 3.3 V power supply
- Supply range: $V_{DD}$ - $V_{SS}$ = 2.7 V to 3.6 V, $V_{DDA}$ - $V_{SSA}$ = 2.7 V to 3.6 V

## 1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory

## Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP | Type | State During Reset | Signal Description |
|---|---|---|---|---|---|---|
| | | | | | | high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1. |
| **GPIOA3** | 16 | 12 | — | Input/Output | Input, internal pullup enabled | GPIO Port A3: After reset, the default state is GPIOA3. |
| (ANA3&VREFLA&CMPA_IN2) | | | | Input | | ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A. |
| **GPIOA4** | 12 | 8 | — | Input/Output | Input, internal pullup enabled | GPIO Port A4: After reset, the default state is GPIOA4. |
| (ANA4&CMPD_IN0) | | | | Input | | ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D. |
| **GPIOA5** | 11 | — | — | Input/Output | Input, internal pullup enabled | GPIO Port A5: After reset, the default state is GPIOA5. |
| (ANA5&CMPD_IN1) | | | | Input | | ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D. |
| **GPIOA6** | 10 | — | — | Input/Output | Input, internal pullup enabled | GPIO Port A6: After reset, the default state is GPIOA6. |
| (ANA6&CMPD_IN2) | | | | Input | | ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D. |
| **GPIOA7** | 9 | — | — | Input/Output | Input, internal pullup enabled | GPIO Port A7: After reset, the default state is GPIOA7. |
| (ANA7&CMPD_IN3) | | | | Input | | ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D. |
| **GPIOB0** | 24 | 17 | 11 | Input/Output | Input, internal pullup enabled | GPIO Port B0: After reset, the default state is GPIOB0. |
| (ANB0&CMPB_IN3) | | | | Input | | ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0. |
| **GPIOB1** | 25 | 18 | 12 | Input/Output | Input, internal pullup enabled | GPIO Port B1: After reset, the default state is GPIOB1. |
| (ANB1&CMPB_IN0) | | | | Input | | ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. The ADC control register configures this input as ANB1. |

*Table continues on the next page...*

## Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP | Type | State During Reset | Signal Description |
|---|---|---|---|---|---|---|
| DACB_O | | | | Analog Output | | 12-bit digital-to-analog output |
| **GPIOB2** | 27 | 20 | 13 | Input/Output | Input, internal pullup enabled | GPIO Port B2: After reset, the default state is GPIOB2. |
| (ANB2&VERFHB &CMPC_IN3) | | | | Input | | ANB2 is analog input to channel 2 of ADCB; VREFHB is analog reference high of ADCB; CMPC_IN3 is positive input 3 of analog comparator C. When used as an analog input, the signal goes to both ANB2 and CMPC_IN3. |
| **GPIOB3** | 28 | 21 | — | Input/Output | Input, internal pullup enabled | GPIO Port B3: After reset, the default state is GPIOB3. |
| (ANB3&VREFLB& CMPC_IN0) | | | | Input | | ANB3 is analog input to channel 3 of ADCB; VREFLB is analog reference low of ADCB; CMPC_IN0 is negative input 0 of analog comparator C. |
| **GPIOB4** | 21 | 14 | — | Input/Output | Input, internal pullup enabled | GPIO Port B4: After reset, the default state is GPIOB4. |
| (ANB4&CMPC_IN 1) | | | | Input | | ANB4 is analog input to channel 4 of ADCB; CMPC_IN1 is negative input 1 of analog comparator C. |
| **GPIOB5** | 20 | — | — | Input/Output | Input, internal pullup enabled | GPIO Port B5: After reset, the default state is GPIOB5. |
| (ANB5&CMPC_IN 2) | | | | Input | | ANB5 is analog input to channel 5 of ADCB; CMPC_IN2 is negative input 2 of analog comparator C. |
| **GPIOB6** | 19 | — | — | Input/Output | Input, internal pullup enabled | GPIO Port B6: After reset, the default state is GPIOB6. |
| (ANB6&CMPB_IN 1) | | | | Input | | ANB6 is analog input to channel 6 of ADCB; CMPB_IN1 is negative input 1 of analog comparator B. |
| **GPIOB7** | 17 | — | — | Input/Output | Input, internal pullup enabled | GPIO Port B7: After reset, the default state is GPIOB7. |
| (ANB7&CMPB_IN 2) | | | | Input | | ANB7 is analog input to channel 7 of ADCB; CMPB_IN2 is negative input 2 of analog comparator B. |
| **GPIOC0** | 3 | 3 | — | Input/Output | Input, internal pullup enabled | GPIO Port C0: After reset, the default state is GPIOC0. |
| (EXTAL) | | | | Analog Input | | The external crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator. |
| (CLKIN0) | | | | Input | | External clock input 0[1] |
| **GPIOC1** | 4 | 4 | — | Input/Output | Input, internal pullup enabled | GPIO Port C1: After reset, the default state is GPIOC1. |
| (XTAL) | | | | Input | | The external crystal oscillator output (XTAL) connects the internal crystal |

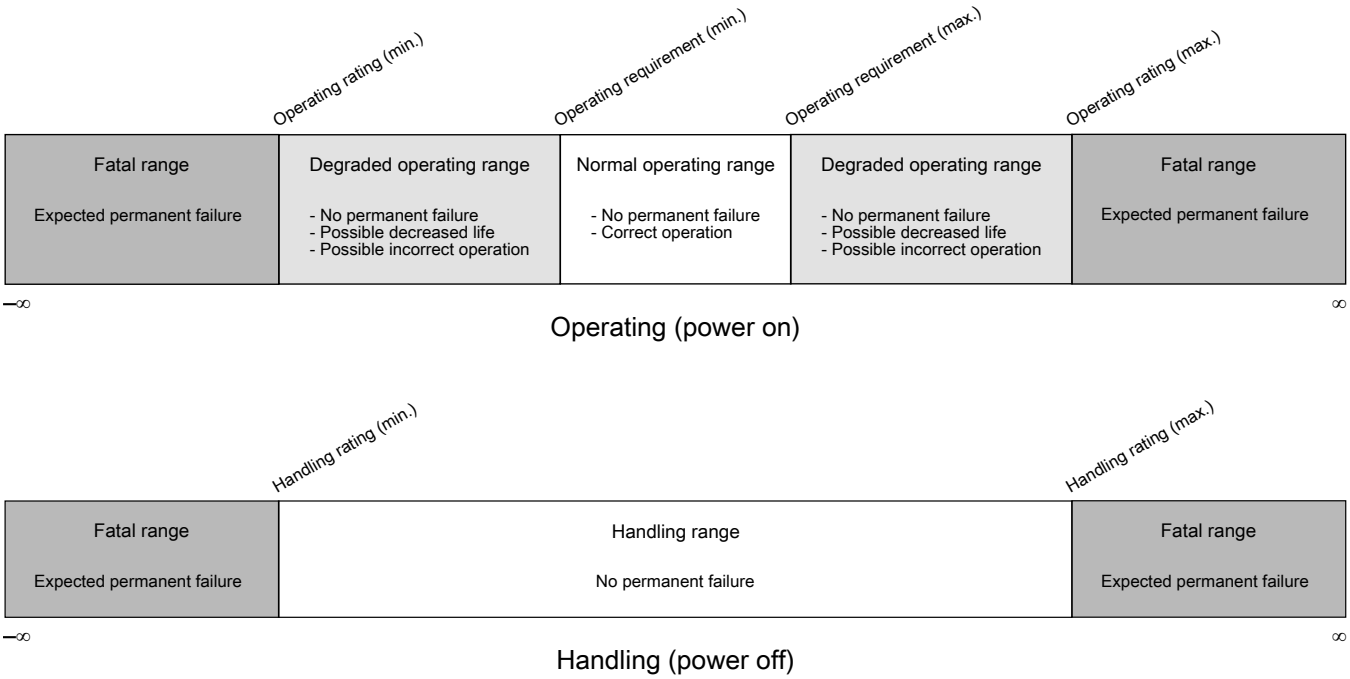
*Table continues on the next page...*

## Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP | Type | State During Reset | Signal Description |
|---|---|---|---|---|---|---|
| ($\overline{SS0\_B}$) | | | | Input/Output | | In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received. |
| (TXD0) | | | | Output | | SCI0 transmit data output or transmit/ receive in single wire operation |
| (XB_IN8) | | | | Input | | Crossbar module input 8 |
| **GPIOC8** | 33 | 25 | 16 | Input/Output | Input, internal pullup enabled | GPIO Port C8: After reset, the default state is GPIOC8. |
| (MISO0) | | | | Input/Output | | Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. |
| (RXD0) | | | | Input | | SCI0 receive data input |
| (XB_IN9) | | | | Input | | Crossbar module input 9 |
| (XB_OUT6) | | | | Output | | Crossbar module output 6 |
| **GPIOC9** | 34 | 26 | 17 | Input/Output | Input, internal pullup enabled | GPIO Port C9: After reset, the default state is GPIOC9. |
| (SCLK0) | | | | Input/Output | | SPI0 serial clock. In master mode, SCLK0 pin is an output, clocking slaved listeners. In slave mode, SCLK0 pin is the data clock input. |
| (XB_IN4) | | | | Input | | Crossbar module input 4 |
| (TXD0) | | | | Output | | SCI0 transmit data output or transmit/ receive in single wire operation |
| (XB_OUT8) | | | | Output | | Crossbar module output 8 |
| **GPIOC10** | 35 | 27 | 18 | Input/Output | Input, internal pullup enabled | GPIO Port C10: After reset, the default state is GPIOC10. |
| (MOSI0) | | | | Input/Output | | Master out/slave in for SPI0 — In master mode, MOSI0 pin is the data output. In slave mode, MOSI0 pin is the data input. |
| (XB_IN5) | | | | Input | | Crossbar module input 4 |
| (MISO0) | | | | Input/Output | | Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. |
| (XB_OUT9) | | | | Output | | Crossbar module output 9 |
| **GPIOC11** | 37 | 29 | — | Input/Output | Input, internal pullup enabled | GPIO Port C11: After reset, the default state is GPIOC11. |
| (CANTX) | | | | Open-drain Output | | CAN transmit data output |
| (SCL0) | | | | Input/Open-drain Output | | $I^2C0$ serial clock |

*Table continues on the next page...*

## 5.6 Relationship between ratings and operating requirements




## 5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

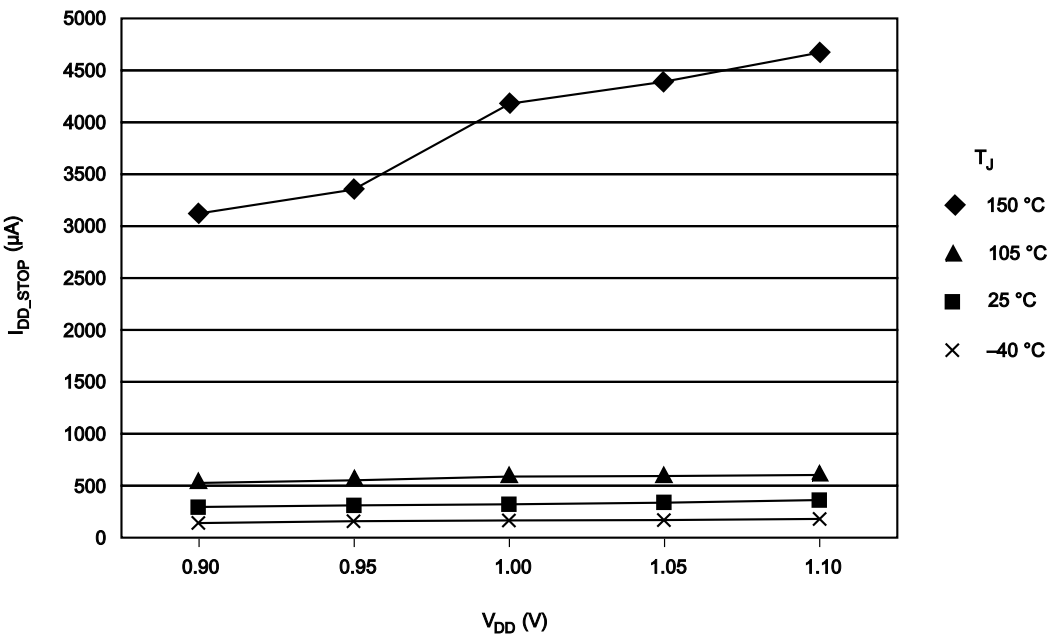
### 5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

## 7.1 General characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except for the $\overline{\text{RESET}}$ pin which is 3.3V only. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 5 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

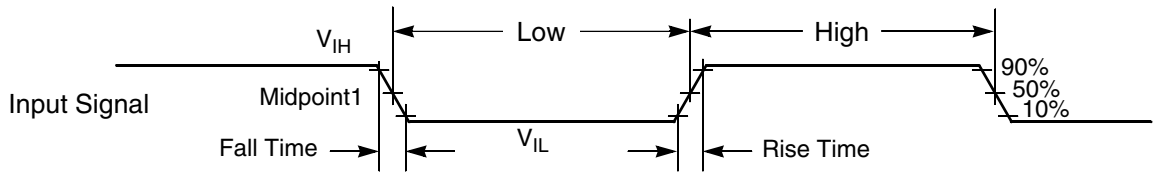
Unless otherwise stated, all specifications within this chapter apply to the temperature range specified in Table 5 over the following supply ranges: $V_{SS}$=$V_{SSA}$=0V, $V_{DD}$=$V_{DDA}$=3.0V to 3.6V, CL≤50 pF, $f_{OP}$=50MHz.

**CAUTION**

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

## 7.2 AC electrical characteristics

Tests are conducted using the input levels specified in Table 8. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.




The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

**Figure 3. Input signal measurement references**

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached $V_{OL}$ or $V_{OH}$
- Data Invalid state, when a signal level is in transition between $V_{OL}$ and $V_{OH}$

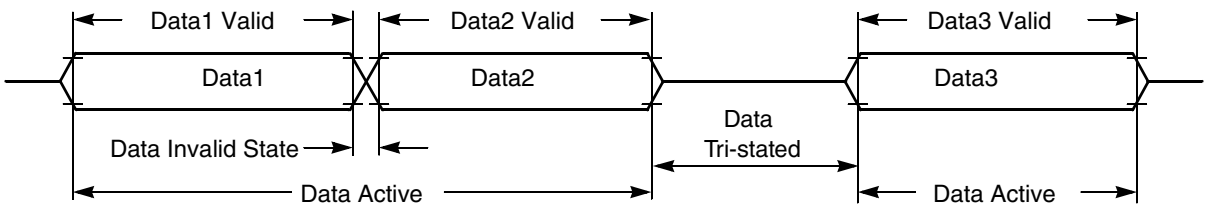



**Figure 4. Signal states**

## 7.3 Nonswitching electrical specifications

### 7.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

**NOTE**

Recommended $V_{DD}$ ramp rate is between 1 ms and 200 ms.

**Table 6. Recommended Operating Conditions ($V_{REFLx}$=0V, $V_{SSA}$=0V, $V_{SS}$=0V)**

| Characteristic | Symbol | Notes[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$, $V_{DDA}$ | | 2.7 | 3.3 | 3.6 | V |
| ADC (Cyclic) Reference Voltage High | $V_{REFHA}$<br>$V_{REFHB}$ | | $V_{DDA}$-0.6 | | $V_{DDA}$ | V |
| Voltage difference $V_{DD}$ to $V_{DDA}$ | ΔVDD | | -0.1 | 0 | 0.1 | V |
| Voltage difference $V_{SS}$ to $V_{SSA}$ | ΔVSS | | -0.1 | 0 | 0.1 | V |
| Input Voltage High (digital inputs) | $V_{IH}$ | Pin Group 1 | 0.7 x $V_{DD}$ | | 5.5 | V |
| $\overline{\text{RESET}}$ Voltage High | $V_{IH\_RESET}$ | Pin Group 2 | 0.7 x $V_{DD}$ | — | $V_{DD}$ | V |

*Table continues on the next page...*

**Table 9. Reset, stop, wait, and interrupt timing (continued)**

| Characteristic | Symbol | Typical Min | Typical Max | Unit | See Figure |
|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ deassertion to First Address Fetch | $t_{RDA}$ | 865 x $T_{OSC}$ + 8 x T | | ns | — |
| Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop) | $t_{IF}$ | 361.3 | 570.9 | ns | — |

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 µF on $\overline{\text{RESET}}$.

**NOTE**

In Table 9, T = system clock cycle and $T_{OSC}$ = oscillator clock cycle. For an operating frequency of 50MHz, T=20 ns. At 4 MHz (used coming out of reset and stop modes), T=250 ns.

**Table 10. Power mode transition behavior**

| Symbol | Description | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $T_{POR}$ | After a POR event, the amount of delay from when $V_{DD}$ reaches 2.7 V to when the first instruction executes (over the operating temperature range). | 199 | 225 | µs | |
| | STOP mode to RUN mode | 6.79 | 7.27.31 | µs | 2 |
| | LPS mode to LPRUN mode | 240.9 | 551 | µs | 3 |
| | VLPS mode to VLPRUN mode | 1424 | 1459 | µs | 4 |
| | WAIT mode to RUN mode | 0.570 | 0.620 | µs | 5 |
| | LPWAIT mode to LPRUN mode | 237.2 | 554 | µs | 3 |
| | VLPWAIT mode to VLPRUN mode | 1413 | 1500 | µs | 4 |

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is 8 MHz IRC in normal mode.
3. CPU clock = 200 KHz and 8 MHz IRC on standby. Exit by an interrupt on PORTC GPIO.
4. Using 64 KHz external clock; CPU Clock = 32KHz. Exit by an interrupt on PortC GPIO.
5. Clock configuration: CPU and system clocks= 100 MHz. Bus Clock = 50 MHz. .Exit by interrupt on PORTC GPIO

## 7.3.5 Power consumption operating behaviors

**Table 11. Current Consumption (mA)**

| Mode | Maximum Frequency | Conditions | Typical at 3.3 V, 25°C | | Maximum at 3.6 V, 105°C | | Maximum at 3.6V, 125°C | |
|---|---|---|---|---|---|---|---|---|
| | | | $I_{DD}$[1] | $I_{DDA}$ | $I_{DD}$[1] | $I_{DDA}$ | $I_{DD}$[1] | $I_{DDA}$ |
| RUN1 | 100 MHz | • 100 MHz Core<br>• 50 MHz Peripheral clock<br>• Regulators are in full regulation<br>• Relaxation Oscillator on | 38.1 | 9.9 | 53.5 | 13.2 | 53.5 | 13.2 |

*Table continues on the next page...*

calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ is very small.

See Thermal design considerations for more detail on thermal design considerations.

| Board type | Symbol | Description | 32 QFN | 32 LQFP | 48 LQFP | 64 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 96 | 83 | 70 | 64 | °C/W | , |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 33 | 55 | 46 | 46 | °C/W | 1, |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 80 | 70 | 57 | 52 | °C/W | 1,2 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 27 | 49 | 39 | 39 | °C/W | 1,2 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 12 | 31 | 23 | 28 | °C/W | |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 1.8 | 22 | 17 | 15 | °C/W | |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 6 | 5 | 3 | 3 | °C/W | |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

**Table 27. 12-bit ADC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Spurious Free Dynamic Range | SFDR | | 77 | | dB |
| Signal to Noise plus Distortion | SINAD | | 66 | | dB |
| Effective Number of Bits | ENOB | | — | | bits |
| Gain = 1x (Fully Differential/Unipolar) | | | 10.6 | | |
| Gain = 2x (Fully Differential/Unipolar) | | | — | | |
| Gain = 4x (Fully Differential/Unipolar) | | | 10.3 | | |
| Gain = 1x (Single Ended) | | | 10.6 | | |
| Gain = 2x (Single Ended) | | | 10.4 | | |
| Gain = 4x (Single Ended) | | | 10.2 | | |
| Variation across channels[10] | | | 0.1 | | |
| **ADC Inputs** | | | | | |
| Input Leakage Current | $I_{IN}$ | | 1 | | nA |
| Temperature sensor slope | $T_{SLOPE}$ | | 1.7 | | mV/°C |
| Temperature sensor voltage at 25 °C | $V_{TEMP25}$ | | 0.82 | | V |
| **Disturbance** | | | | | |
| Input Injection Current [11] | $I_{INJ}$ | | | +/-3 | mA |
| Channel to Channel Crosstalk[12] | ISOXTLK | | -82 | | dB |
| Memory Crosstalk[13] | MEMXTLK | | -71 | | dB |
| Input Capacitance<br>Sampling Capacitor | $C_{ADI}$ | | 4.8 | | pF |

1. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed
2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V $V_{DDA}$, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

### 8.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

## Table 29. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | — | 25 | 50 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0)[3] | — | 60 | 200 | ns |
| | Analog comparator initialization delay[4] | — | 40 | — | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| | 6-bit DAC reference inputs, Vin1 and Vin2<br>There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range. | $V_{DDA}$ | — | $V_{DD}$ | V |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[5] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Measured with input voltage range limited to 0 to $V_{DD}$
2. Measured with input voltage range limited to $0.7 \le Vin \le V_{DD}-0.8$
3. Input voltage range: $0.1V_{DD} \le Vin \le 0.9V_{DD}$, step = ±100mV, across all temperature. Does not include PCB and PAD delay.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

## Table 32. SPI timing (continued)

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|---|---|---|---|---|
| Clock (SCK) high time | $t_{CH}$ | | — | ns | Figure 13 |
| Master | | | — | ns | Figure 14 |
| Slave | | | | | Figure 15 |
| | | | | | Figure 16 |
| Clock (SCK) low time | $t_{CL}$ | 28 | — | ns | Figure 16 |
| Master | | 28 | — | ns | |
| Slave | | | | | |
| Data set-up time required for inputs | $t_{DS}$ | 20 | — | ns | Figure 13 |
| Master | | 1 | — | ns | Figure 14 |
| Slave | | | | | Figure 15 |
| | | | | | Figure 16 |
| Data hold time required for inputs | $t_{DH}$ | 1 | — | ns | Figure 13 |
| Master | | 3 | — | ns | Figure 14 |
| Slave | | | | | Figure 15 |
| | | | | | Figure 16 |
| Access time (time to data active from high-impedance state) | $t_A$ | 5 | — | ns | Figure 16 |
| Slave | | | | | |
| Disable time (hold time to high-impedance state) | $t_D$ | 5 | — | ns | Figure 16 |
| Slave | | | | | |
| Data valid for outputs | $t_{DV}$ | — | | ns | Figure 13 |
| Master | | — | | ns | Figure 14 |
| Slave (after enable edge) | | | | | Figure 15 |
| | | | | | Figure 16 |
| Data invalid | $t_{DI}$ | 0 | — | ns | Figure 13 |
| Master | | 0 | — | ns | Figure 14 |
| Slave | | | | | Figure 15 |
| | | | | | Figure 16 |
| Rise time | $t_R$ | — | 1 | ns | Figure 13 |
| Master | | — | 1 | ns | Figure 14 |
| Slave | | | | | Figure 15 |
| | | | | | Figure 16 |
| Fall time | $t_F$ | — | 1 | ns | Figure 13 |
| Master | | — | 1 | ns | Figure 14 |
| Slave | | | | | Figure 15 |
| | | | | | Figure 16 |

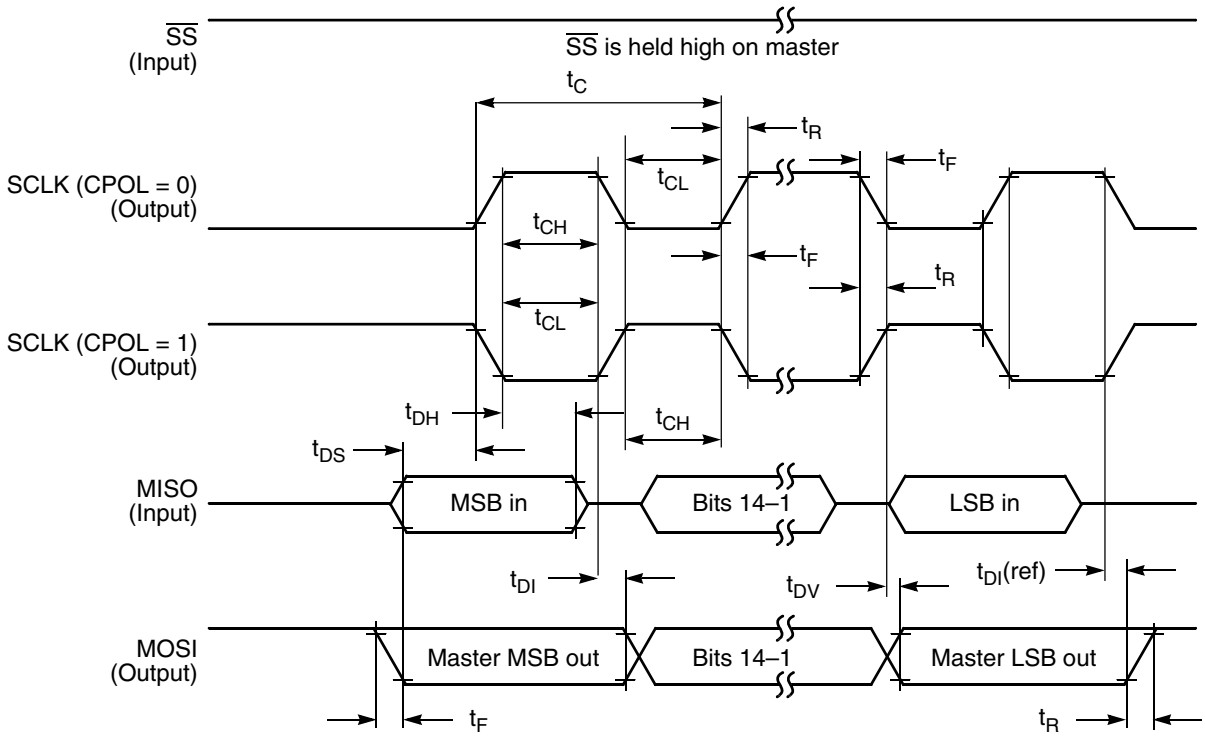



**Figure 13. SPI master timing (CPHA = 0)**

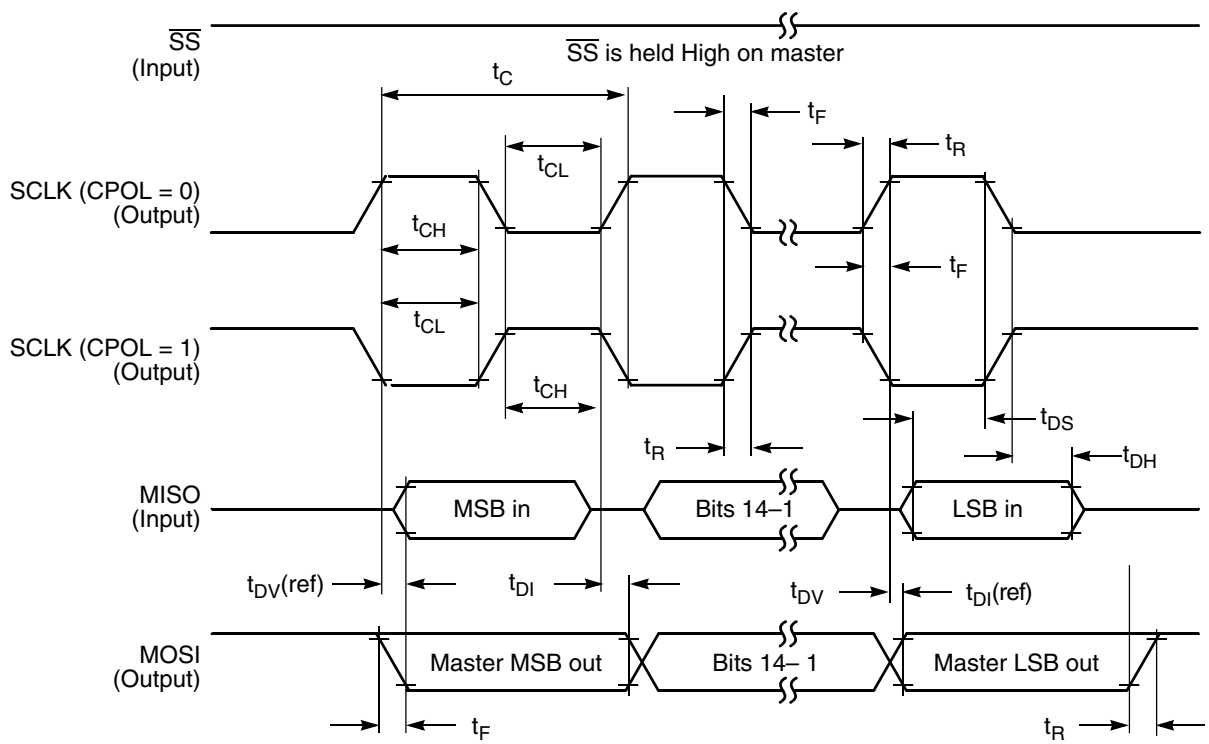



**Figure 14. SPI master timing (CPHA = 1)**

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

**To determine the junction temperature of the device in the application when heat sinks are not used**, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

$T_T$ = Thermocouple temperature on top of package (°C/W)

$\Psi_{JT}$ = hermal characterization parameter (°C/W)

$P_D$ = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

**To determine the junction temperature of the device in the application when heat sinks are used**, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

# 11 Pinout

## 11.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

**NOTE**

- The RESETB pin is a 3.3 V pin only.
- If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.
- Not all CMPD pins are not available on 48 LQFP, 32 LQFP, and 32 QFN packages.
- QSPI signals—including MISO1, MOSI1, SCLK1, and SS0_B—are not available on the 48 LQFP, 32 LQFP, and 32 QFN packages.

| 64 LQFP | 48 LQFP | 32 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | TCK | TCK | GPIOD2 | | | |
| 2 | 2 | 2 | RESETB | RESETB | GPIOD4 | | | |
| 3 | 3 | — | GPIOC0 | GPIOC0 | EXTAL | CLKIN0 | | |
| 4 | 4 | — | GPIOC1 | GPIOC1 | XTAL | | | |
| 5 | 5 | 3 | GPIOC2 | GPIOC2 | TXD0 | XB_OUT11 | XB_IN2 | CLKO0 |
| 6 | — | — | GPIOF8 | GPIOF8 | RXD0 | XB_OUT10 | CMPD_O | PWM_2X |
| 7 | 6 | 4 | GPIOC3 | GPIOC3 | TA0 | CMPA_O | RXD0 | CLKIN1 |
| 8 | 7 | 5 | GPIOC4 | GPIOC4 | TA1 | CMPB_O | XB_IN6 | EWM_OUT_B |
| 9 | — | — | GPIOA7 | GPIOA7 | ANA7&CMPD_IN3 | | | |
| 10 | — | — | GPIOA6 | GPIOA6 | ANA6&CMPD_IN2 | | | |
| 11 | — | — | GPIOA5 | GPIOA5 | ANA5&CMPD_IN1 | | | |
| 12 | 8 | — | GPIOA4 | GPIOA4 | ANA4&CMPD_IN0 | | | |
| 13 | 9 | 6 | GPIOA0 | GPIOA0 | ANA0&CMPA_IN3 | CMPC_O | | |
| 14 | 10 | 7 | GPIOA1 | GPIOA1 | ANA1&CMPA_IN0 | | | |
| 15 | 11 | 8 | GPIOA2 | GPIOA2 | ANA2&VREFHA&CMPA_IN1 | | | |
| 16 | 12 | — | GPIOA3 | GPIOA3 | ANA3&VREFLA&CMPA_IN2 | | | |
| 17 | — | — | GPIOB7 | GPIOB7 | ANB7&CMPB_IN2 | | | |
| 18 | 13 | — | GPIOC5 | GPIOC5 | DACA_O | XB_IN7 | | |
| 19 | — | — | GPIOB6 | GPIOB6 | ANB6&CMPB_IN1 | | | |

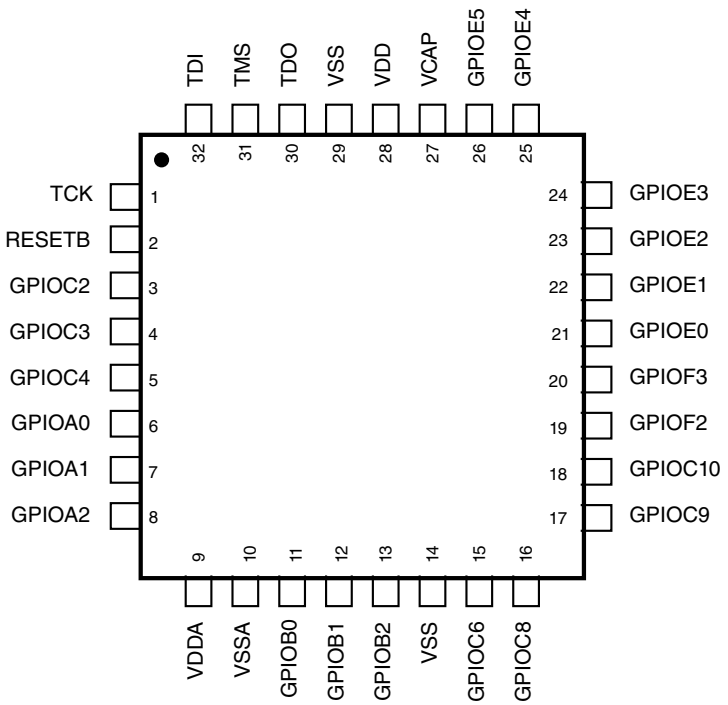



**Figure 25. 32-pin LQFP and QFN**

**NOTE**

The RESETB pin is a 3.3 V pin only.

# 12 Product documentation

The documents listed in Table 36 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

**Table 36. Device documentation**

| Topic | Description | Document Number |
|---|---|---|
| DSP56800E/DSP56800EX Reference Manual | Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set | DSP56800ERM |
| MC56F827xx Reference Manual | Detailed functional description and programming model | MC56F827XXRM |
| MC56F827xx Data Sheet | Electrical and timing specifications, pin descriptions, and package information (this document) | MC56F827XXDS |
| MC56F82xxx Errata | Details any chip issues that might be present | MC56F82xxx_Errata |

# 13 Revision History

The following table summarizes changes to this document since the release of the previous version.

**Table 37. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 10/2013 | First public release |
| 2.1 | 11/2013 | • In Table 2, added DACB_O signal description.<br>• In Obtaining package dimensions, changed 32-QFN's document number from '98ARE10566D' to '98ASA00473D'. |
| 2.2 | 03/2016 - 05/2016 | • Corrected document part number MC56F827XXDS to MC56F827XX.<br>• In "12-bit ADC Electrical Specifications" table, corrected Max Gain Error to 0.990 to 1.010.<br>• In Part identification section, in part number fields table, added the 32QFN package identifier.<br>• In Electrical design considerations" section, added additional section "Power-on Reset design considerations".<br>• Added new section "Power-on Reset design considerations".<br>• In "Peripheral highlights" section, added<br>  • Periodic Interrupt Timer (PIT) Modules<br>  • External Watchdog Monitor (EWM) |
| 3.0 | 09/2016 | • Added products: 56F82746MLF, 56F82733MFM<br>• Removed PDB (Programmable Delay Block) mentions, because PDBs are not present in these devices.<br>• Added V and M temperature options to operating characteristics.<br>• Moved "Signal groups" section under "MC56F827xx signal and pin descriptions" section.<br>• In "Voltage and current operating ratings" section: updated note; in "Absolute Maximum Ratings" table, updated Ambient and Junction Temperature rows, also fixed broken footnotes.<br>• In "Power consumption operating behaviors" section, in "Current Consumption" table: added columns and data for Maximum at 3.6V, 125°C", fixed broken footnotes.<br>• In "Thermal operating requirements" section, updated Die junction temperature and Ambient temperature requirements.<br>• In "Relaxation Oscillator Timing" section, in "Relaxation Oscillator Electrical Specifications" table:<br>  • Added data for "-40°C to 125°C" temperature range.<br>  • For "8 MHz Output Frequency, Standby Mode frequency", 2 corrections were made.<br>  • Fixed broken footnotes. |