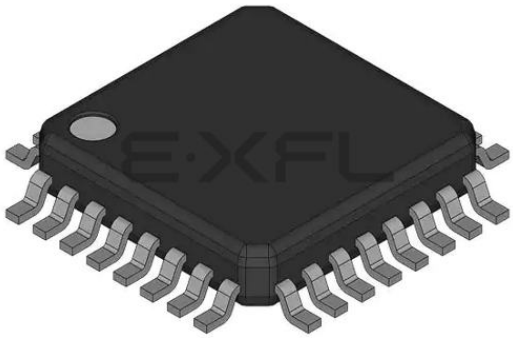

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f82723vlc

Table of Contents

1 Overview

1.1 MC56F827xx Product Family

The following table is the comparsion of features among members of the family.

Table 1. MC56F827xx Family

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Core frequency (MHz)	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50
Flash memory (KB)	64	64	64	64	48	48	48	48	32	32	32	32
RAM (KB)	8	8	8	8	8	8	8	8	6	6	6	6
Interrupt Controller	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Windowed Computer Operating Properly (WCOP)	1	1	1	1	1	1	1	1	1	1	1	1
External Watchdog Monitor (EWM)	1	1	1	1	1	1	1	1	1	1	1	1
Periodic Interrupt Timer (PIT)	2	2	2	2	2	2	2	2	2	2	2	2
Cyclic Redundancy Check (CRC)	1	1	1	1	1	1	1	1	1	1	1	1
Quad Timer (TMR)	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4
12-bit Cyclic ADC channels	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3
PWM Module:												
Input capture channels[2]	12	6	6	6	12	6	6	6	12	6	6	6
High-resolution channels	8	6	6	6	8	6	6	6	8	6	6	6
Standard channels	4	0	0	0	4	0	0	0	4	0	0	0
12-bit DAC	2	2	2	2	2	2	2	2	2	2	2	2
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table continues on the next page...

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode
- Operation ambient temperature:
  V Temperature option:-40 ºC to 105ºC
  M Temperature option:-40 ºC to 125ºC
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1.
GPIOA3	16	12	—	Input/Output	Input, internal pullup enabled	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)				Input		ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A.
GPIOA4	12	8	—	Input/Output	Input, internal pullup enabled	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&CMPD_IN0)				Input		ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D.
GPIOA5	11	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&CMPD_IN1)				Input		ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D.
GPIOA6	10	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&CMPD_IN2)				Input		ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D.
GPIOA7	9	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&CMPD_IN3)				Input		ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D.
GPIOB0	24	17	11	Input/Output	Input, internal pullup enabled	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)				Input		ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0.
GPIOB1	25	18	12	Input/Output	Input, internal pullup enabled	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)				Input		ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. The ADC control register configures this input as ANB1.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
GPIOE4	51	39	25	Input/Output	Input, internal pullup enabled	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)				Input/Output		PWM module A (NanoEdge), submodule 2, output B or input capture B
(XB_IN2)				Input		Crossbar module input 2
GPIOE5	52	40	26	Input/Output	Input, internal pullup enabled	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)				Input/Output		PWM module A (NanoEdge), submodule 2, output A or input capture A
(XB_IN3)				Input		Crossbar module input 3
GPIOE6	53	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)				Input/Output		PWM module A (NanoEdge), submodule 3, output B or input capture B
(XB_IN4)				Input		Crossbar module input 4
GPIOE7	54	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E7: After reset, the default state is GPIOE7.
(PWMA_3A)				Input/Output		PWM module A (NanoEdge), submodule 3, output A or input capture A
(XB_IN5)				Input		Crossbar module input 5
GPIOF0	36	28	—	Input/Output	Input, internal pullup enabled	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)				Input		Crossbar module input 6
(SCLK1)				Input/Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	50	38	—	Input/Output	Input, internal pullup enabled	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)				Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		Crossbar module input 7
(CMPD_O)				Output		Analog comparator D output
GPIOF2	39	—	19	Input/Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)				Input/Open-drain Output		I^2C0 serial clock
(XB_OUT6)				Output		Crossbar module output 6
(MISO1)				Input/Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device

Table continues on the next page...

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 2 C F P T PP N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
2	DSC subfamily	• 2
C	Maximum CPU frequency (MHz)	• 3 = 50 MHz • 7 = 100 MHz
F	Primary program flash memory size	• 1 = 16 KB • 2 = 32 KB • 3 = 48 KB • 4 = 64 KB
P	Pin count	• 3 = 32 • 6 = 48 • 8 = 64
T	Temperature range (°C)	• V = –40 to 105 • M = –40 to 125
PP	Package identifier	• LC = 32LQFP • FM = 32QFN • LF = 48LQFP • LH = 64LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 Example

This is an example part number: MC56F82748VLH

5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

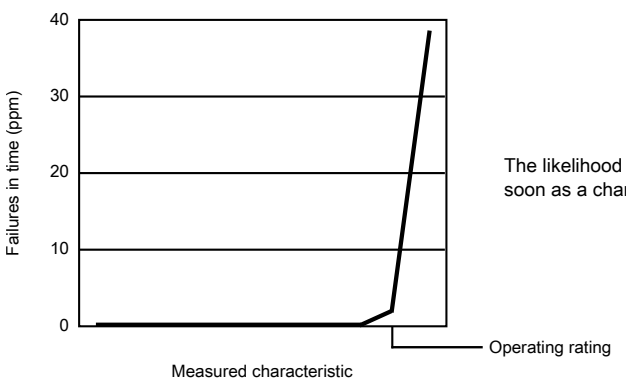
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

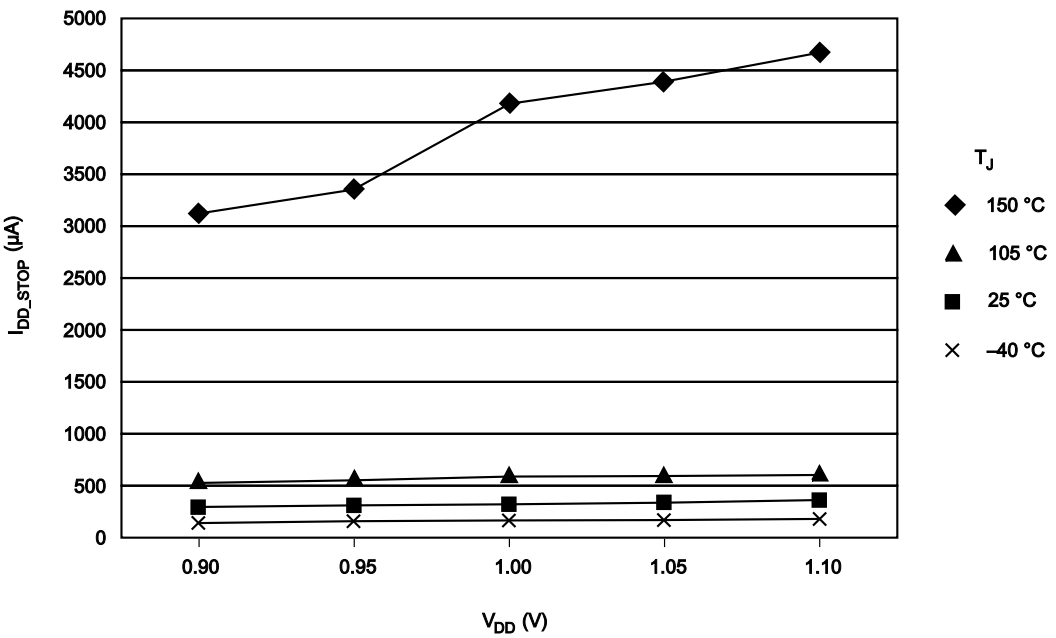
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode						

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.
2. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:2 between the CPU clock and the flash clock when running with 2 MHz external clock input and CPU running at 1 MHz.

7.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

7.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

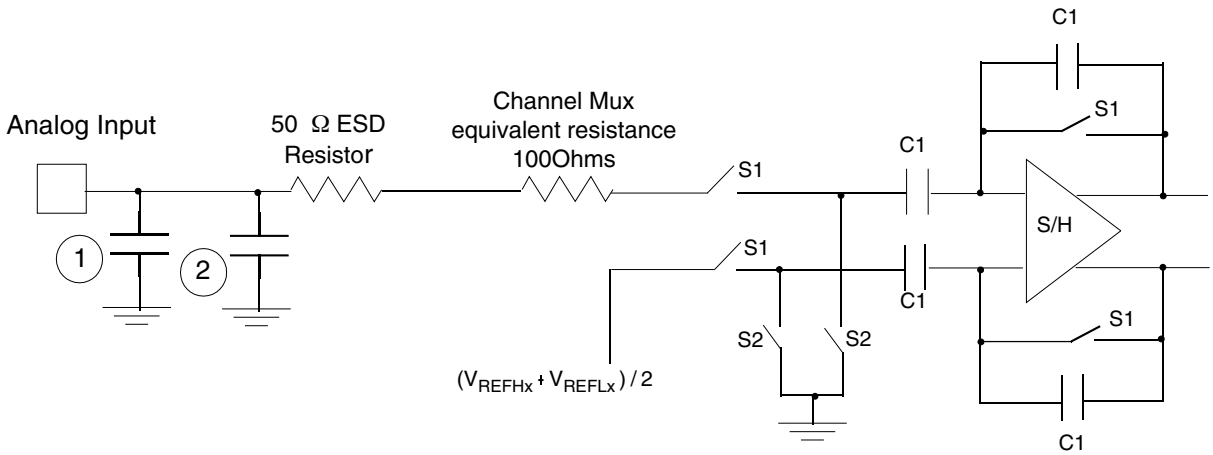
7.4 Switching specifications

7.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{BUS}	Bus clock	—	50	MHz	

$$\frac{1}{(\text{ADC ClockRate}) \times 4.8 \times 10^{-12}} + 100\ ohm + 50\ ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

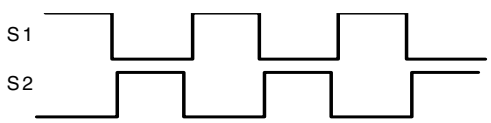


Figure 9. Equivalent circuit for A/D loading

8.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

Table 28. DAC parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pF		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words:	INL	—	+/- 3	+/- 4	LSB[3]

Table continues on the next page...

Table 28. DAC parameters (continued)

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
	410 to 3891 ($19A - $F33) 5% to 95% of full range					
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+ /- 43	mV
Gain error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806 mV

8.5.3 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	300	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	36	—	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis				
	• CR0[HYSTCTR] = 00[1]	—	5	13	mV
	• CR0[HYSTCTR] = 01	—	25	48	mV
	• CR0[HYSTCTR] = 10[2]	—	55	105	mV
	• CR0[HYSTCTR] = 11[2]	—	80	148	mV

Table continues on the next page...

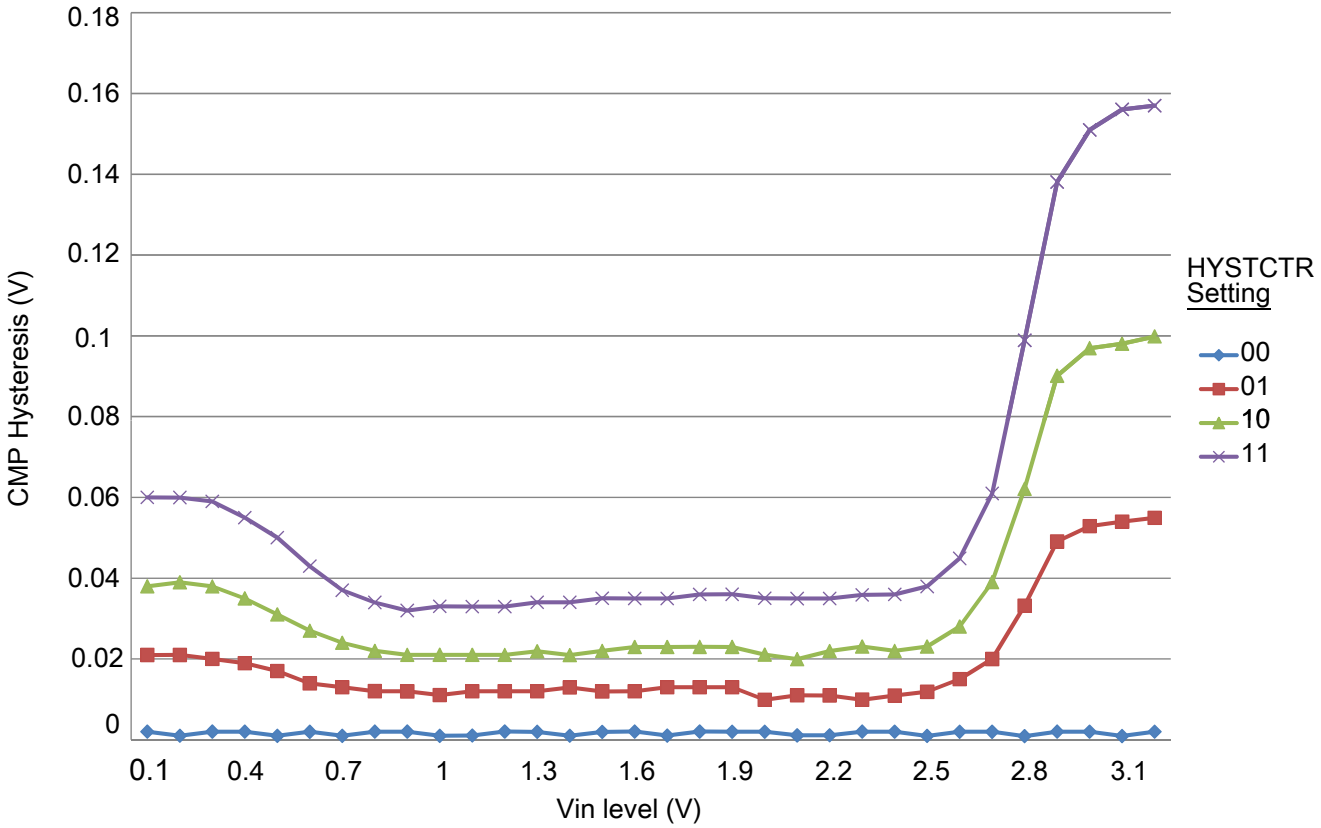


Figure 11. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

8.6 PWMs and timers

8.6.1 Enhanced NanoEdge PWM characteristics

Table 30. NanoEdge PWM timing parameters

Characteristic	Symbol	Min	Typ	Max	Unit
PWM clock frequency			100		MHz
NanoEdge Placement (NEP) Step Size[1, 2]	pwmp		312		ps
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		25		µs

1. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

8.6.2 Quad Timer timing

Parameters listed are guaranteed by design.

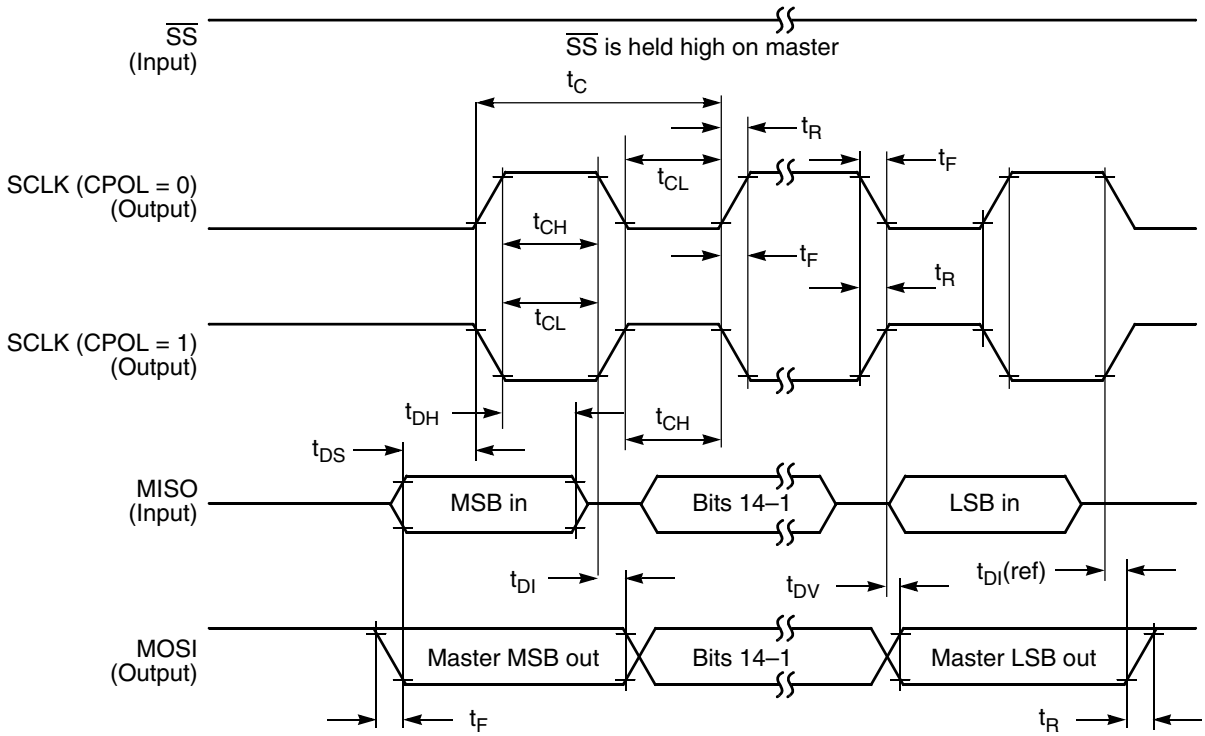


Figure 13. SPI master timing (CPHA = 0)

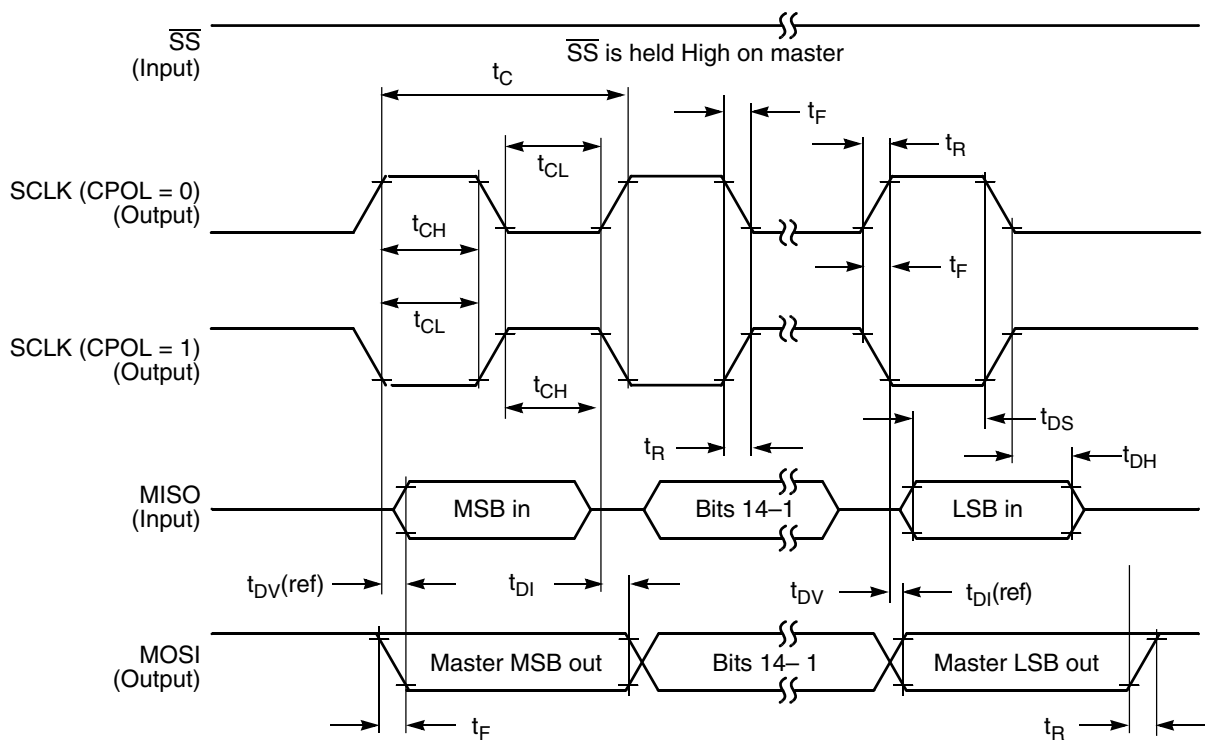


Figure 14. SPI master timing (CPHA = 1)

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

9.3 Power-on Reset design considerations

9.3.1 Improper power-up sequence between VDD/VSS and VDDA/VSSA:

It is recommended that VDD be kept within 100 mV of VDDA at all times, including power ramp-up and ramp-down. Failure to keep VDDA within 100 mV of VDDA may cause a leakage current through the substrate, between the VDD and VDDA pad cells. This leakage current could prevent operation of the device after it powers up. The voltage difference between VDD and VDDA must be limited to below 0.3 V at all times, to avoid permanent damage to the part (See Table 5). Also see Table 6.

9.3.2 Improperly designed protection circuit:

In many circuit designs, it is a general practice to add external clamping diodes on each analog input pin; see diode D1 and D2 in Figure 21, to prevent the surge voltage from damaging the analog input. However, in some cases, these diodes can cause the DSC to fail to start at power-on. For example, in Figure 21, the entire system is directly powered from the power grid; high voltage is fed to 12V DC/DC converter Reg1, then 12V powers DC/DC converter Reg2 and Reg3 to provide 3.3V supply voltage to VDD and VDDA. Due to the startup time delay of DC/DC converters and per-charge the capacitors on 12V and 3.3V rail, VDDA can be charged to a less than 0.5V through a path of R6->R5->R4->R2->D1. If this low voltage duration is more than 1 ms without continuing ramp-up, then it can cause the device to fail to start up.

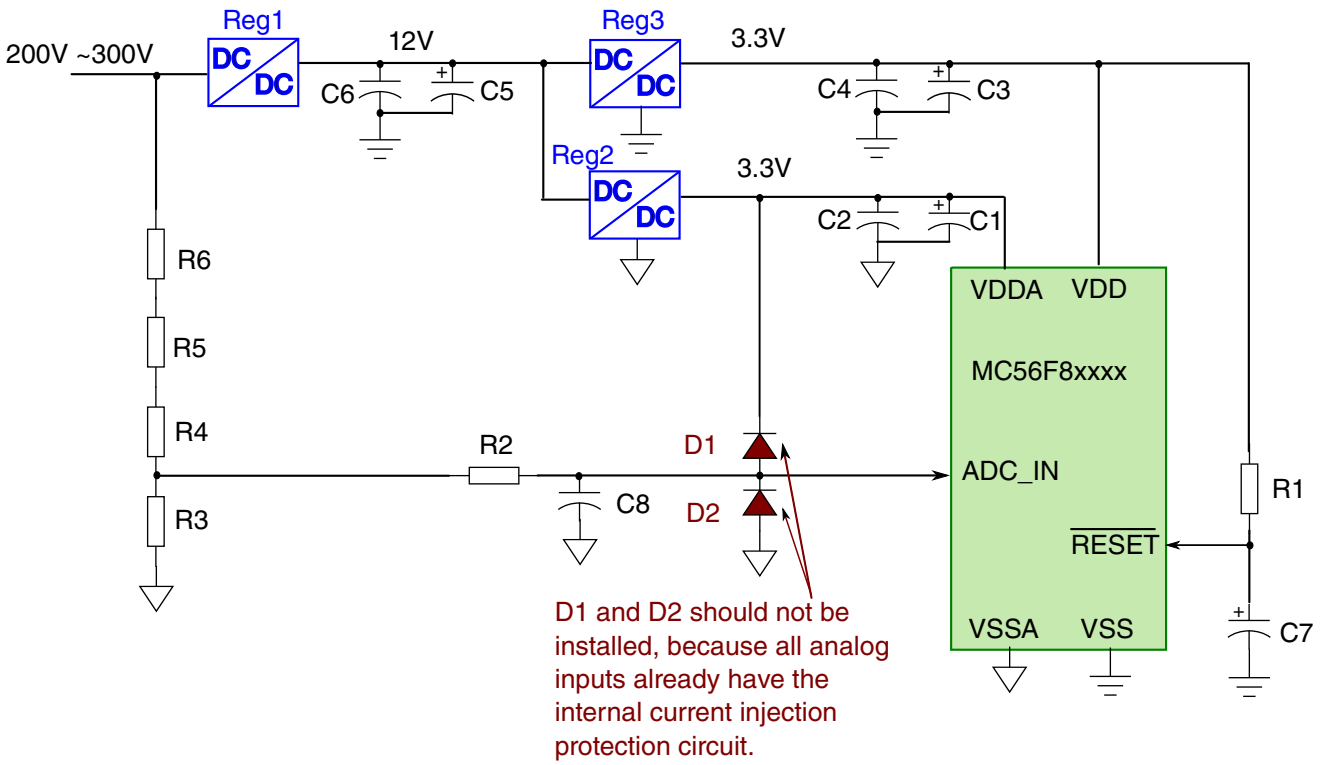


Figure 21. Protection Circuit Example

MC56F8xxxx DSC uses the 5V tolerance I/O. When the pin is configured to digital input, it can accept 5V input. Table 5. When the pin is configured to analog input, the internal integrated current injection protection circuit is enabled. The current injection protection circuit performs the same functions as external clamp diode D1 and D2 in Figure 21. As long as the source or sink current for each analog pin is less than 3 mA, then there is no damage to the device. See Table 27.

This situation could happen if diodes D1 or D2 are used for clamping; therefore in this case, the D1 and D2 clamping diodes are not recommended to be used.

NOTE

In some designs, VDD and VDDA are powered from the same power supply. In this case, above analysis and suggestions are also applicatble.

9.3.3 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.5V to 2.7V. However, the MC56F8xxxx DSC will exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the

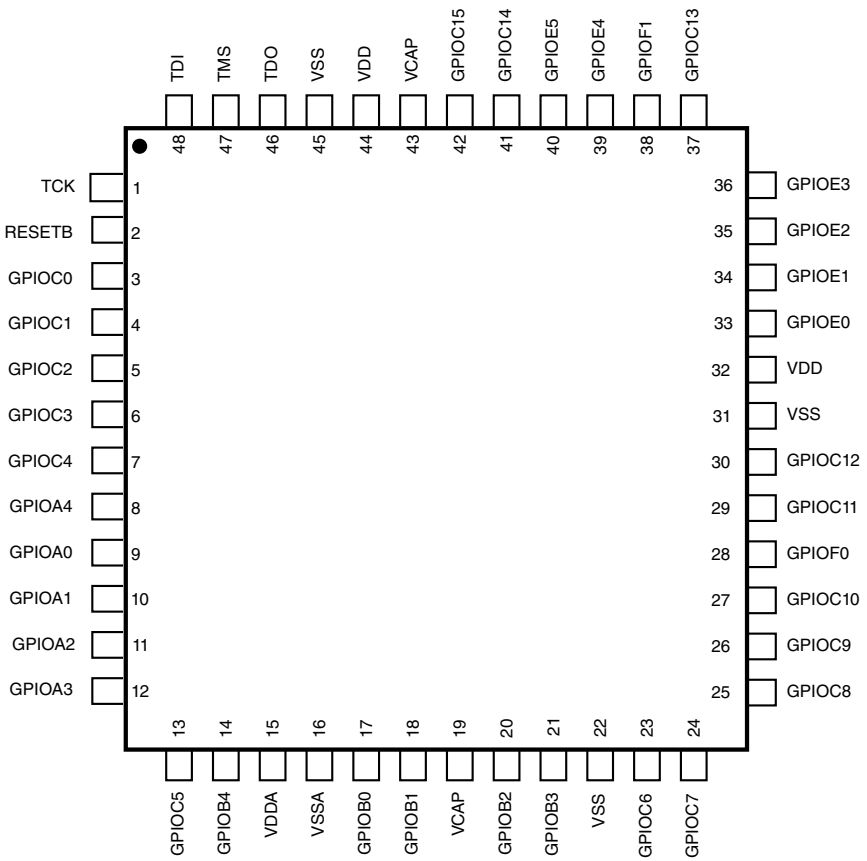


Figure 24. 48-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

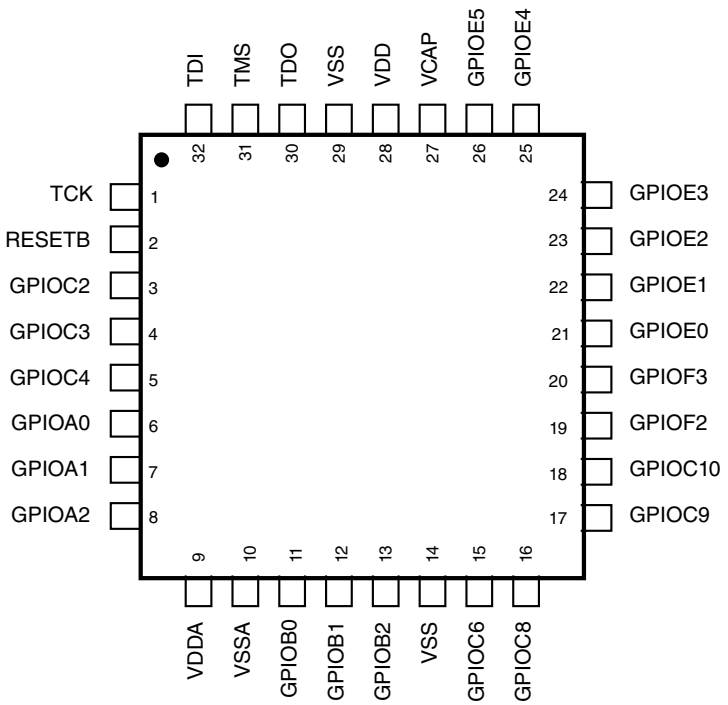


Figure 25. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 36 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 36. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F827xx Reference Manual	Detailed functional description and programming model	MC56F827XXRM
MC56F827xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F827XXDS
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev. No.	Date	Substantial Changes
2	10/2013	First public release
2.1	11/2013	• In Table 2, added DACB_O signal description. • In Obtaining package dimensions, changed 32-QFN's document number from '98ARE10566D' to '98ASA00473D'.

2.2	03/2016 - 05/2016	• Corrected document part number MC56F827XXDS to MC56F827XX.
		• In "12-bit ADC Electrical Specifications" table, corrected Max Gain Error to 0.990 to 1.010.
		• In Part identification section, in part number fields table, added the 32QFN package identifier.
		• In Electrical design considerations" section, added additional section "Power-on Reset design considerations".
		• Added new section "Power-on Reset design considerations".
		• In "Peripheral highlights" section, added
		  • Periodic Interrupt Timer (PIT) Modules
		  • External Watchdog Monitor (EWM)

3.0	09/2016	• Added products: 56F82746MLF, 56F82733MFM
		• Removed PDB (Programmable Delay Block) mentions, because PDBs are not present in these devices.
		• Added V and M temperature options to operating characteristics.
		• Moved "Signal groups" section under "MC56F827xx signal and pin descriptions" section.
		• In "Voltage and current operating ratings" section: updated note; in "Absolute Maximum Ratings" table, updated Ambient and Junction Temperature rows, also fixed broken footnotes.
		• In "Power consumption operating behaviors" section, in "Current Consumption" table: added columns and data for Maximum at 3.6V, 125°C", fixed broken footnotes.
		• In "Thermal operating requirements" section, updated Die junction temperature and Ambient temperature requirements.
		• In "Relaxation Oscillator Timing" section, in "Relaxation Oscillator Electrical Specifications" table:
		  • Added data for "-40°C to 125°C" temperature range.
		  • For "8 MHz Output Frequency, Standby Mode frequency", 2 corrections were made.
		  • Fixed broken footnotes.

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Document Number MC56F827XXDS
Revision 3.0, 09/2016