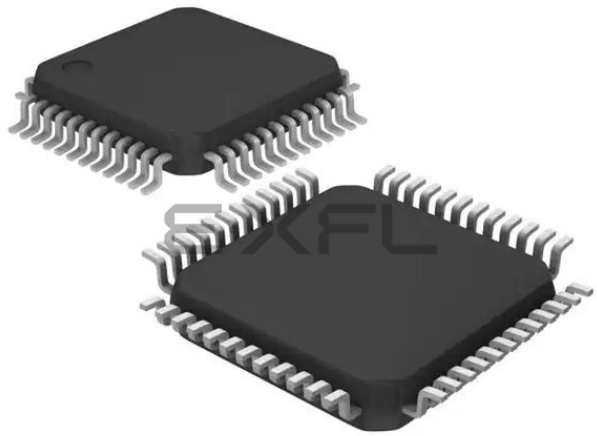

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f82726vlf

- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

1.6.16 Clock sources

1.6.16.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.16.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.6.17 Cyclic Redundancy Check (CRC) Generator

- Hardware CRC generator circuit with 16-bit shift register
- High-speed hardware CRC calculation
- Programmable initial seed value
- CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multibit errors
- Option to transpose input data or output data (CRC result) bitwise, which is required for certain CRC standards

1.6.18 General Purpose I/O (GPIO)

- 5 V tolerance (except RESETB pin)
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set

enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

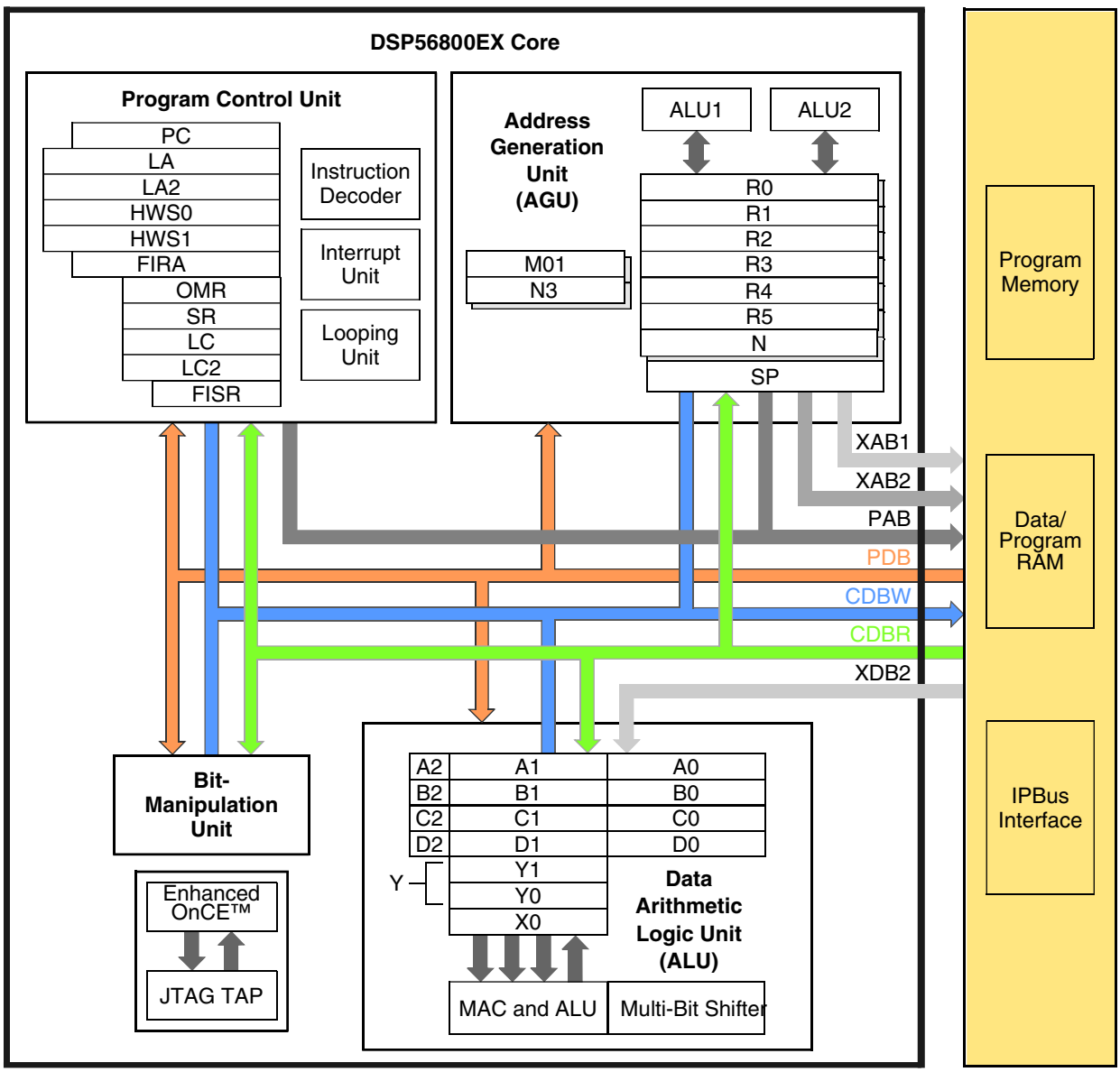

Figure 1. 56800EX basic block diagram

2 MC56F827xx signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIOx_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA outputs, in cases where the fault conditions originate off-chip.

For the MC56F827xx products, which use 64-pin LQFP, 48-pin LQFP and 32-pin packages:

Table 2. Signal descriptions

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
V_{DD}	29	—	—	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
	44	32	—			
	60	44	28			
V_{SS}	30	22	14	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
	43	31	—			
	61	45	29			
V_{DDA}	22	15	9	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	23	16	10	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	26	19	—	On-chip regulator output	On-chip regulator output	Connect a 2.2 µF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation.
	57	43	27			
TDI	64	48	32	Input	Input, internal pullup enabled	Test Data Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)				Input/Output		GPIO Port D0
TDO	62	46	30	Output	Output	Test Data Output — It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO
(GPIOD1)				Input/Output	Output	GPIO Port D1

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
TCK	1	1	1	Input	Input, internal pullup enabled	Test Clock Input — The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK
(GPIOD2)				Input/Output		GPIO Port D2
TMS	63	47	31	Input	Input, internal pullup enabled	Test Mode Select Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to V_{DD} through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to V_{DD}.
(GPIOD3)				Input/Output		GPIO Port D3
$\overline{\text{RESET}}$ or RESETB	2	2	2	Input	Input, internal pullup enabled	Reset — A direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. After reset, the default state is $\overline{\text{RESET}}$. Recommended a capacitor of up to 0.1 µF for filtering noise.
(GPIOD4)				Input/ Opendrain Output		GPIO Port D4 $\overline{\text{RESET}}$ functionality is disabled in this mode and the device can be reset only through POR, COP reset, or software reset.
GPIOA0	13	9	6	Input/Output	Input, internal pullup enabled	GPIO Port A0
(ANA0&CMPA_IN3)				Input		ANA0 is analog input to channel 0 of ADCA; CMPA_IN3 is positive input 3 of analog comparator A. After reset, the default state is GPIOA0.
(CMPC_O)				Output		Analog comparator C output
GPIOA1	14	10	7	Input/Output	Input, internal pullup enabled	GPIO Port A1: After reset, the default state is GPIOA1.
(ANA1&CMPA_IN0)				Input		ANA1 is analog input to channel 1 of ADCA; CMPA_IN0 is negative input 0 of analog comparator A. When used as an analog input, the signal goes to ANA1 and CMPA_IN0. The ADC control register configures this input as ANA1 or CMPA_IN0.
GPIOA2	15	11	8	Input/Output	Input, internal pullup enabled	GPIO Port A2: After reset, the default state is GPIOA2.
(ANA2&VREFHA &CMPA_IN1)				Input		ANA2 is analog input to channel 2 of ADCA; VREFHA is analog reference

Table continues on the next page...

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 2 C F P T PP N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
2	DSC subfamily	• 2
C	Maximum CPU frequency (MHz)	• 3 = 50 MHz • 7 = 100 MHz
F	Primary program flash memory size	• 1 = 16 KB • 2 = 32 KB • 3 = 48 KB • 4 = 64 KB
P	Pin count	• 3 = 32 • 6 = 48 • 8 = 64
T	Temperature range (°C)	• V = –40 to 105 • M = –40 to 125
PP	Package identifier	• LC = 32LQFP • FM = 32QFN • LF = 48LQFP • LH = 64LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 Example

This is an example part number: MC56F82748VLH

6 Ratings

6.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 4. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device.

NOTE

If the voltage difference between VDD and VDDA or VSS and VSSA is too large, then the device can malfunction or be permanently damaged. The restrictions are:

- **At all times, it is recommended that the voltage difference of VDD - VSS be within +/-200 mV of the voltage difference of VDDA - VSSA,**, including power ramp up and ramp down; see additional requirements in Table 6. Failure to do this recommendation may result in a harmful leakage current through the substrate, between the VDD/VSS and VDDA/VSSA pad cells. This harmful leakage current could prevent the device from operating after power up.
- **At all times, to avoid permanent damage to the part, the voltage difference between VDD and VDDA must absolutely be limited to 0.3 V**, See Table 5.
- **At all times, to avoid permanent damage to the part, the voltage difference between VSS and VSSA must absolutely be limited to 0.3 V**, See Table 5.

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V

Table continues on the next page...

Table 9. Reset, stop, wait, and interrupt timing (continued)

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 µF on $\overline{\text{RESET}}$.

NOTE

In Table 9, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 50MHz, T=20 ns. At 4 MHz (used coming out of reset and stop modes), T=250 ns.

Table 10. Power mode transition behavior

Symbol	Description	Min	Max	Unit	Notes[1]
T_{POR}	After a POR event, the amount of delay from when V_{DD} reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
	STOP mode to RUN mode	6.79	7.27.31	µs	2
	LPS mode to LPRUN mode	240.9	551	µs	3
	VLPS mode to VLPRUN mode	1424	1459	µs	4
	WAIT mode to RUN mode	0.570	0.620	µs	5
	LPWAIT mode to LPRUN mode	237.2	554	µs	3
	VLPWAIT mode to VLPRUN mode	1413	1500	µs	4

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is 8 MHz IRC in normal mode.
3. CPU clock = 200 KHz and 8 MHz IRC on standby. Exit by an interrupt on PORTC GPIO.
4. Using 64 KHz external clock; CPU Clock = 32KHz. Exit by an interrupt on PortC GPIO.
5. Clock configuration: CPU and system clocks= 100 MHz. Bus Clock = 50 MHz. .Exit by interrupt on PORTC GPIO

7.3.5 Power consumption operating behaviors

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN1	100 MHz	• 100 MHz Core • 50 MHz Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on	38.1	9.9	53.5	13.2	53.5	13.2

Table continues on the next page...

Table 11. Current Consumption (mA) (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock • ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked • Comparator powered on						
RUN2	50 MHz	• 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock • ADC/DAC (only one 12-bit DAC and all 6-bit DACs) powered on and clocked • Comparator powered on	27.6	9.9	43.5	13.2	43.5	14.0
WAIT	50 MHz	• 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 2X clock • ADC/DAC (single 12-bit DAC, all 6-bit DACs), Comparator powered off	24.0	—	41.3	—	41.3	—
STOP	4 MHz	• 4 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/DAC/Comparator powered off	6.3	—	19.4	—	19.4	—
LPRUN (LsRUN)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • Repeat NOP instructions	2.8	3.1	11.1	4.0	13.0	4.0

Table continues on the next page...

Table 11. Current Consumption (mA) (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12-bit DAC and all 6-bit DACs enabled. • Simple loop with running from platform instruction buffer						
LPWAIT (LsWAIT)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12-bit DAC and all 6-bit DACs enabled.[2] • Processor core in wait mode	2.7	3.1	11.1	4.0	13.0	4.0
LPSTOP (LsSTOP)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off[2] • Processor core in stop mode	1.2	—	9.1	—	12.0	—
VLPRUN	200 kHz	• 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer	0.7	—	7.5	—	10.0	—
VLPWAIT	200 kHz	• 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode	0.7	—	7.5	—	10.0	—
VLPSTOP	200 kHz	• 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby. • Small regulator is disabled. • PLL disabled	0.7	—	7.5	—	10.0	—

8.2 System modules

8.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the MC56F82xxx's core logic. For proper operations, the voltage regulator requires an external 2.2 µF capacitor on each V_{CAP} pin. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 17.

Table 17. Regulator 1.2 V parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600	—	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 18. Bandgap electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

8.3 Clock modules

8.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 19. External clock operation timing requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

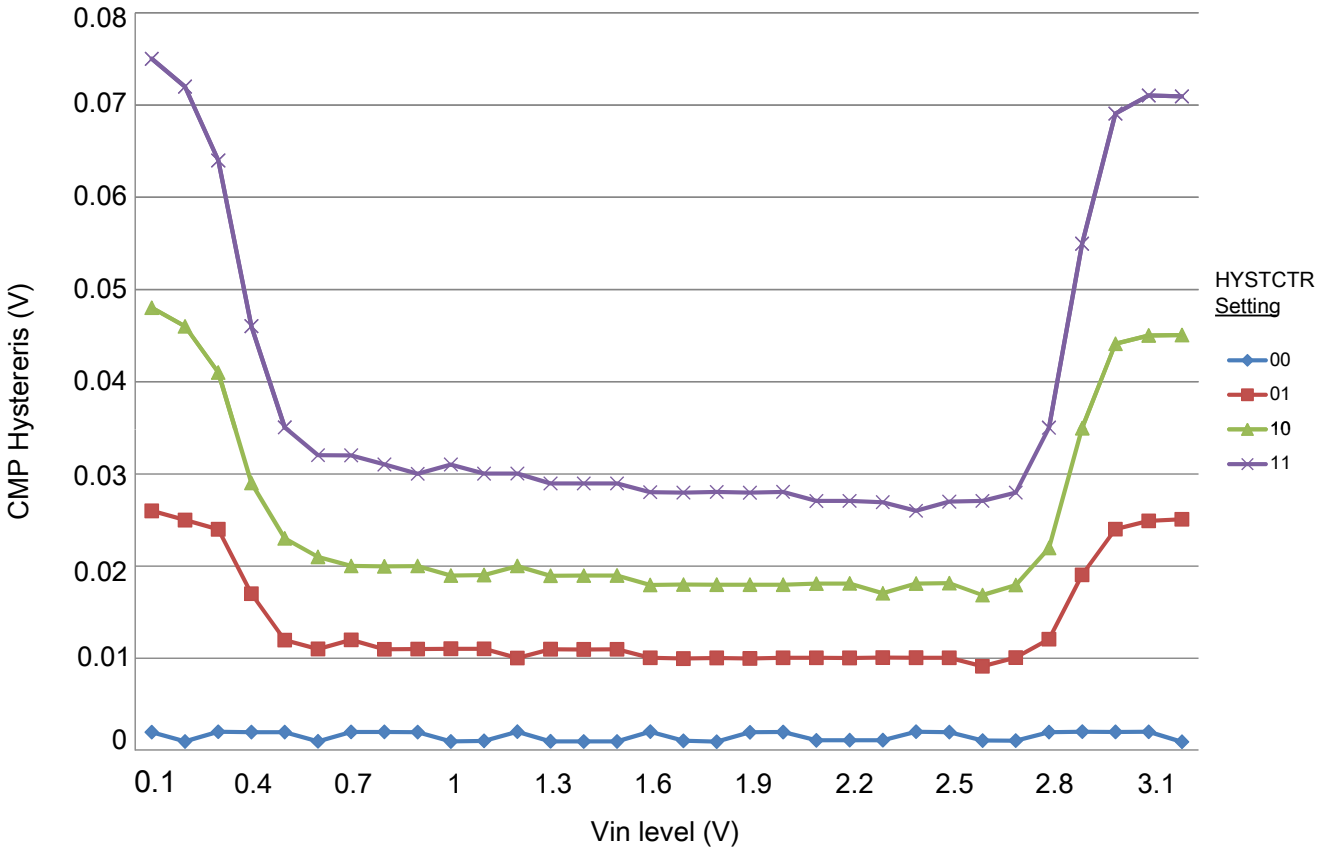

Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

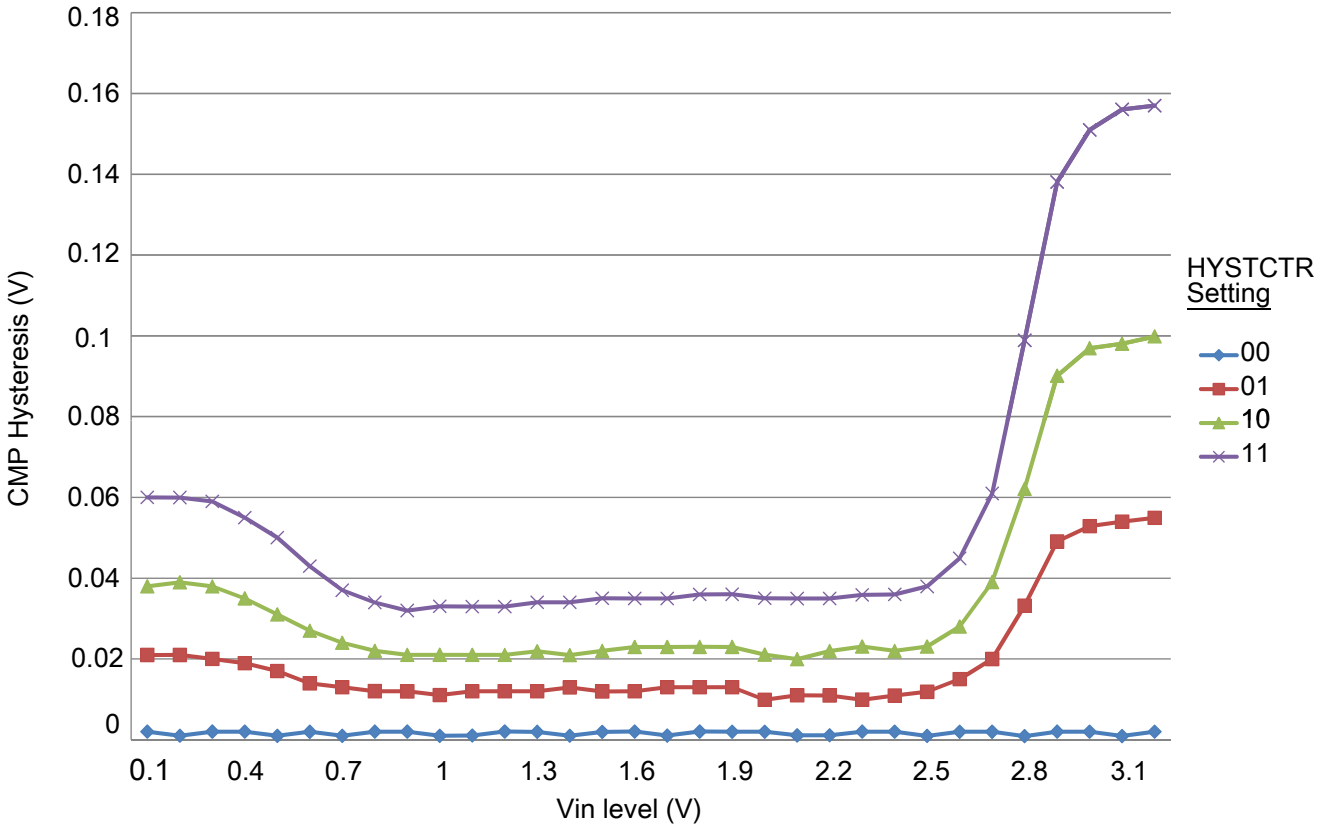

Figure 11. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

8.6 PWMs and timers

8.6.1 Enhanced NanoEdge PWM characteristics

Table 30. NanoEdge PWM timing parameters

Characteristic	Symbol	Min	Typ	Max	Unit
PWM clock frequency			100		MHz
NanoEdge Placement (NEP) Step Size[1, 2]	pwmp		312		ps
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		25		µs

1. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

8.6.2 Quad Timer timing

Parameters listed are guaranteed by design.

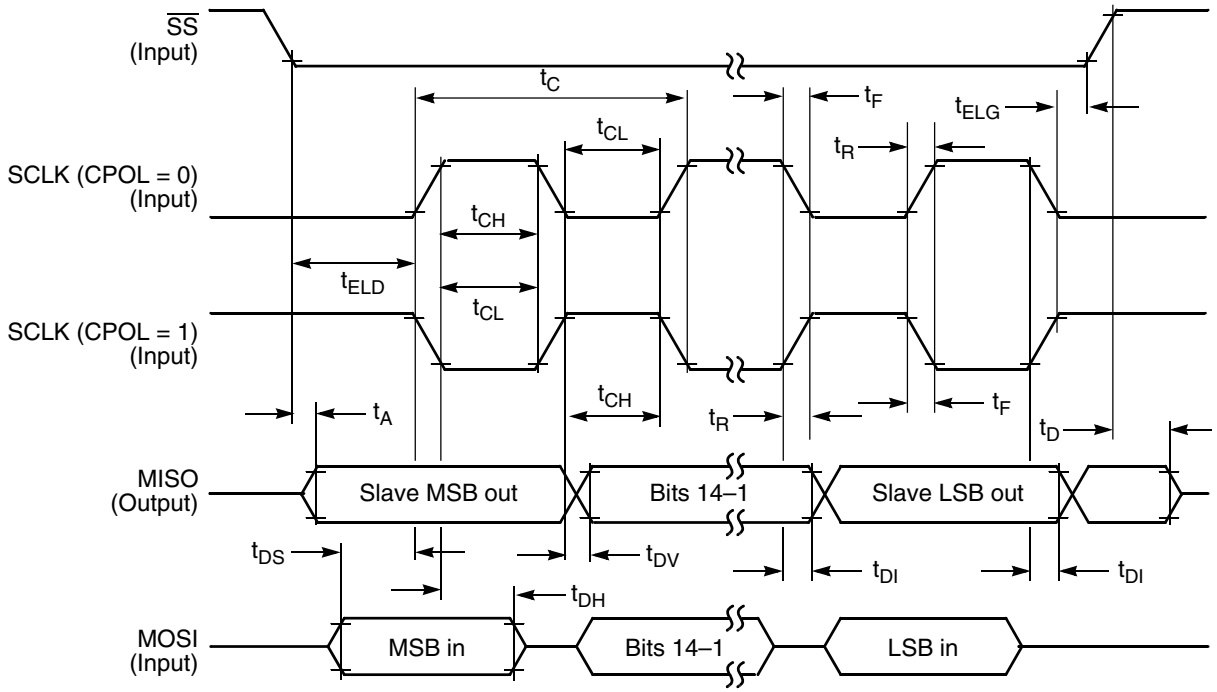

Figure 15. SPI slave timing (CPHA = 0)

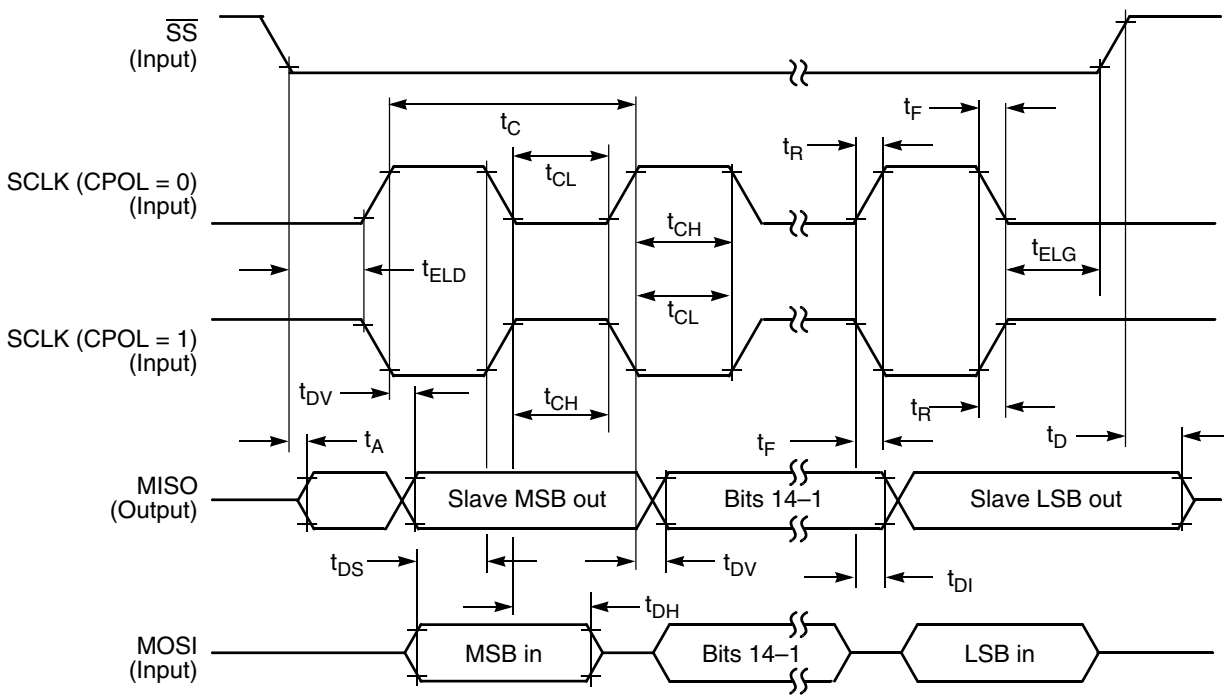

Figure 16. SPI slave timing (CPHA = 1)

8.7.2 Queued Serial Communication Interface (SCI) timing

Parameters listed are guaranteed by design.

Table 33. SCI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbit/s	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 17
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 18
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max.50 MHz depending on part number) or 2x bus clock (max. 100 MHz) for the devices.

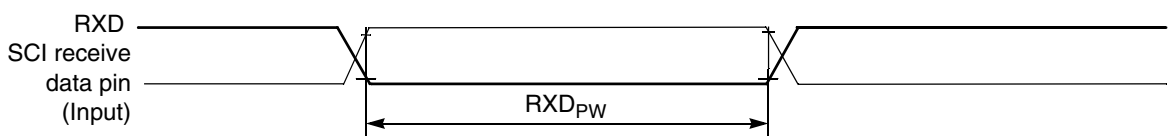

Figure 17. RXD pulse width

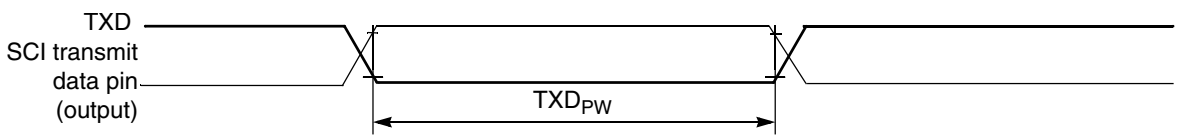

Figure 18. TXD pulse width

8.7.3 Modular/Scalable Controller Area Network (MSCAN)

Table 34. MSCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbit/s
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	1.5	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

high current will be pulled by DSC from the supply, which can cause the supply voltage to drop below the operation voltage; see the captured graph (Figure 22). This can cause the DSC fail to start up.

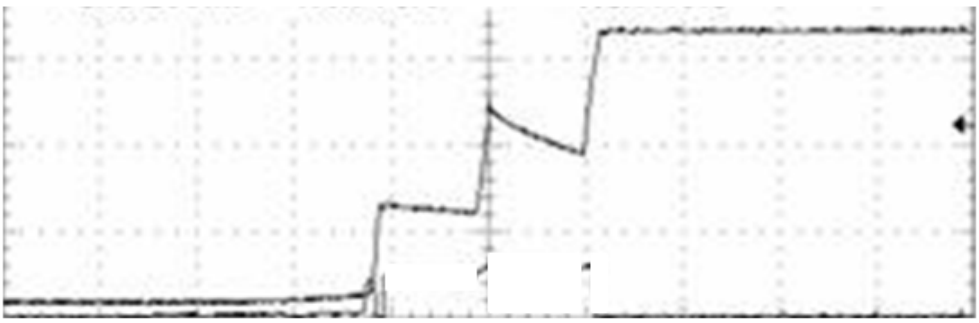

Figure 22. Supply Voltage Drop

A recommended initialization sequence during power-up is:

1. After POR is released, run a few hundred NOP instructions from the internal relaxation oscillator; this gives time for the supply voltage to stabilize.
2. Configure the peripherals (except the ADC) to the desired settings; the ADC should stay in low power mode.
3. Power up the PLL.
4. After the PLL locks, switch the clock from PLL prescale to postscale.
5. Configure the ADC.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
32LQFP	98ASH70029A
32QFN	98ASA00473D
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

64 LQFP	48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
20	—	—	GPIOB5	GPIOB5	ANB5&CMPC_IN2			
21	14	—	GPIOB4	GPIOB4	ANB4&CMPC_IN1			
22	15	9	VDDA	VDDA				
23	16	10	VSSA	VSSA				
24	17	11	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
25	18	12	GPIOB1	GPIOB1	ANB1&CMPB_IN0	DACB_O		
26	19	—	VCAP	VCAP				
27	20	13	GPIOB2	GPIOB2	ANB2&VERFHB&CMPC_IN3			
28	21	—	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
29	—	—	VDD	VDD				
30	22	14	VSS	VSS				
31	23	15	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	SS0_B
32	24	—	GPIOC7	GPIOC7	SS0_B	TXD0	XB_IN8	
33	25	16	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	XB_OUT6
34	26	17	GPIOC9	GPIOC9	SCLK0	XB_IN4	TXD0	XB_OUT8
35	27	18	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	XB_OUT9
36	28	—	GPIOF0	GPIOF0	XB_IN6		SCLK1	
37	29	—	GPIOC11	GPIOC11	CANTX	SCL0	TXD1	
38	30	—	GPIOC12	GPIOC12	CANRX	SDA0	RXD1	
39	—	19	GPIOF2	GPIOF2	SCL0	XB_OUT6	MISO1	
40	—	20	GPIOF3	GPIOF3	SDA0	XB_OUT7	MOSI1	
41	—	—	GPIOF4	GPIOF4	TXD1	XB_OUT8	PWM_0X	PWM_FAULT6
42	—	—	GPIOF5	GPIOF5	RXD1	XB_OUT9	PWM_1X	PWM_FAULT7
43	31	—	VSS	VSS				
44	32	—	VDD	VDD				
45	33	21	GPIOE0	GPIOE0	PWM_0B			
46	34	22	GPIOE1	GPIOE1	PWM_0A			
47	35	23	GPIOE2	GPIOE2	PWM_1B			
48	36	24	GPIOE3	GPIOE3	PWM_1A			
49	37	—	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
50	38	—	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
51	39	25	GPIOE4	GPIOE4	PWM_2B	XB_IN2		
52	40	26	GPIOE5	GPIOE5	PWM_2A	XB_IN3		
53	—	—	GPIOE6	GPIOE6	PWM_3B	XB_IN4		
54	—	—	GPIOE7	GPIOE7	PWM_3A	XB_IN5		
55	41	—	GPIOC14	GPIOC14	SDA0	XB_OUT4	PWM_FAULT4	
56	42	—	GPIOC15	GPIOC15	SCL0	XB_OUT5	PWM_FAULT5	
57	43	27	VCAP	VCAP				
58	—	—	GPIOF6	GPIOF6		PWM_3X		XB_IN2
59	—	—	GPIOF7	GPIOF7		CMPC_O	SS1_B	XB_IN3

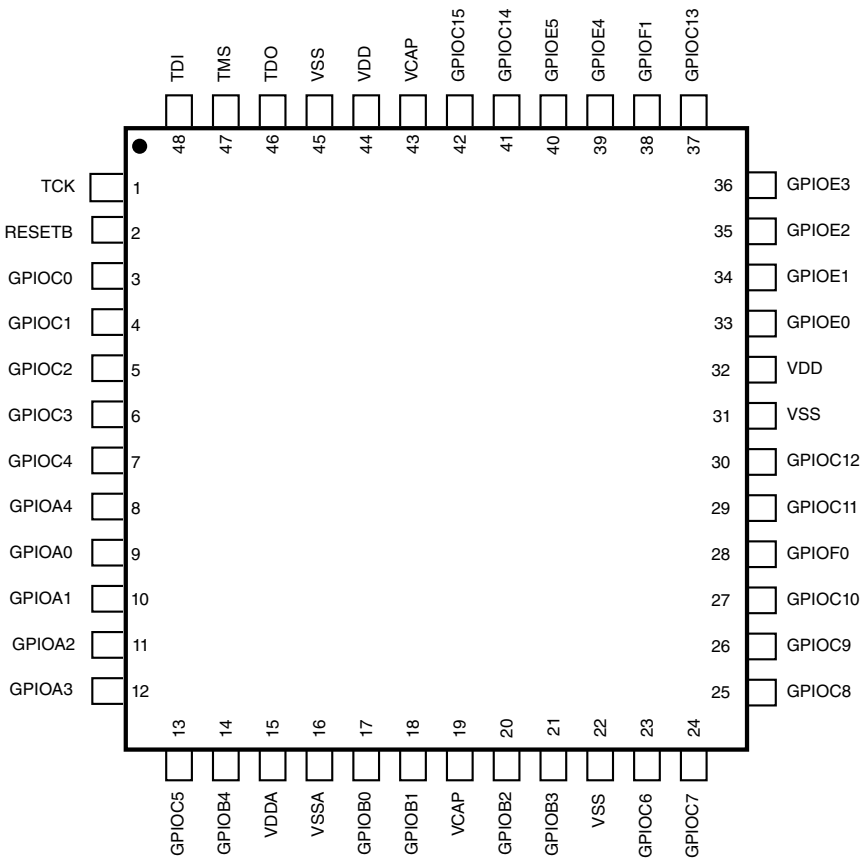

Figure 24. 48-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

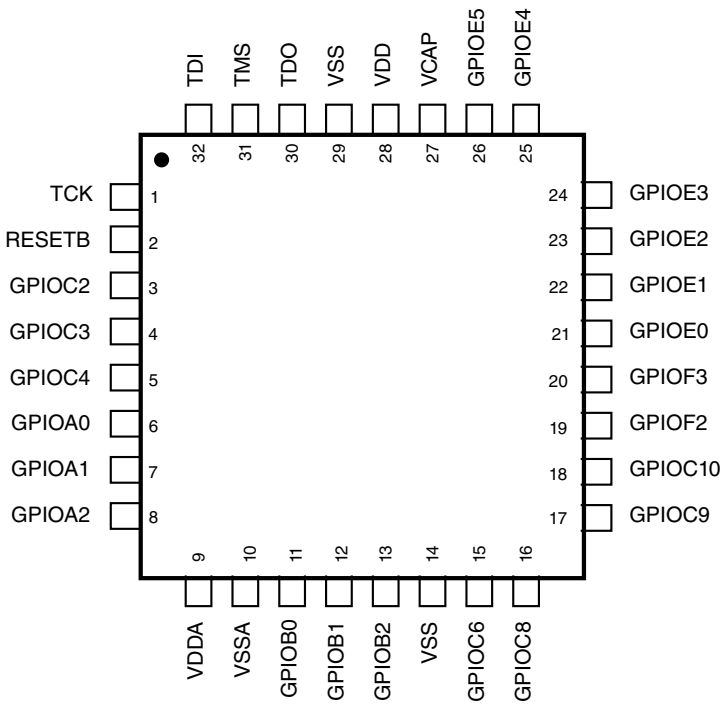

Figure 25. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 36 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 36. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F827xx Reference Manual	Detailed functional description and programming model	MC56F827XXRM
MC56F827xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F827XXDS
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata