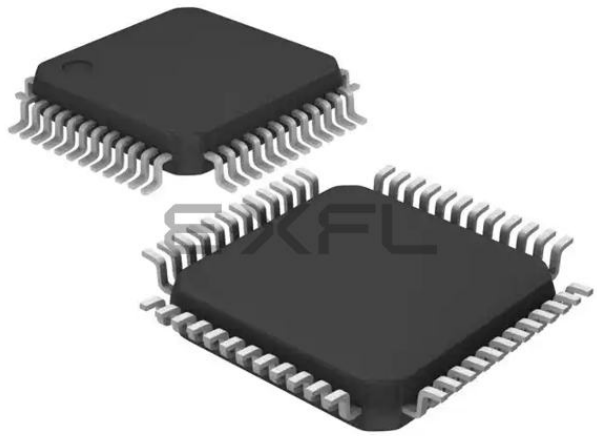

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82726vlfr

1 Overview

1.1 MC56F827xx Product Family

The following table is the comparsion of features among members of the family.

Table 1. MC56F827xx Family

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Core frequency (MHz)	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50	100/50
Flash memory (KB)	64	64	64	64	48	48	48	48	32	32	32	32
RAM (KB)	8	8	8	8	8	8	8	8	6	6	6	6
Interrupt Controller	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Windowed Computer Operating Properly (WCOP)	1	1	1	1	1	1	1	1	1	1	1	1
External Watchdog Monitor (EWM)	1	1	1	1	1	1	1	1	1	1	1	1
Periodic Interrupt Timer (PIT)	2	2	2	2	2	2	2	2	2	2	2	2
Cyclic Redundancy Check (CRC)	1	1	1	1	1	1	1	1	1	1	1	1
Quad Timer (TMR)	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4	1x4
12-bit Cyclic ADC channels	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3	2x8	2x5	2x3	2x3
PWM Module:												
Input capture channels[2]	12	6	6	6	12	6	6	6	12	6	6	6
High-resolution channels	8	6	6	6	8	6	6	6	8	6	6	6
Standard channels	4	0	0	0	4	0	0	0	4	0	0	0
12-bit DAC	2	2	2	2	2	2	2	2	2	2	2	2
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table continues on the next page...

Table 1. MC56F827xx Family (continued)

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Analog Comparators (CMP)	4	4	3	3	4	4	3	3	4	4	3	3
QSCI	2	2	1	1	2	2	1	1	2	2	1	1
QSPI	2	1	1	1	2	1	1	1	2	1	1	1
I2C/SMBus	1	1	1	1	1	1	1	1	1	1	1	1
MSCAN	1	1	0	0	1	1	0	0	1	1	0	0
GPIO	54	39	26	26	54	39	26	26	54	39	26	26
Package pin count	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN
AEC-Q100[3]	Yes	Yes	No	No	Yes	Yes	No	No	Yes	Yes	No	No

1. Temperature options
   V: -40°C to 105°C
   M: -40°C to 125°C
2. Input capture shares the pin with cooresponding PWM channels.
3. Qualification aligned to AEC-Q100

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

1.6.3 Periodic Interrupt Timer (PIT) Modules

- 16-bit counter with programmable count modulo
- PIT0 is master and PIT1 is slave (if synchronizing both PITs)
- The output signals of both PIT0 and PIT1 are internally connected to a peripheral crossbar module
- Can run when the CPU is in Wait/Stop modes. Can also wake up the CPU from Wait/Stop modes.
- In addition to its existing bus clock (up to 50 MHz), 3 alternate clock sources for the counter clock are available:
  - Crystal oscillator output
  - 8 MHz / 400 kHz ROSC (relaxation oscillator output)
  - On-chip low-power 200 kHz oscillator

1.6.4 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, EWM, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.6 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode

- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.13 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC

1.6.14 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.15 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

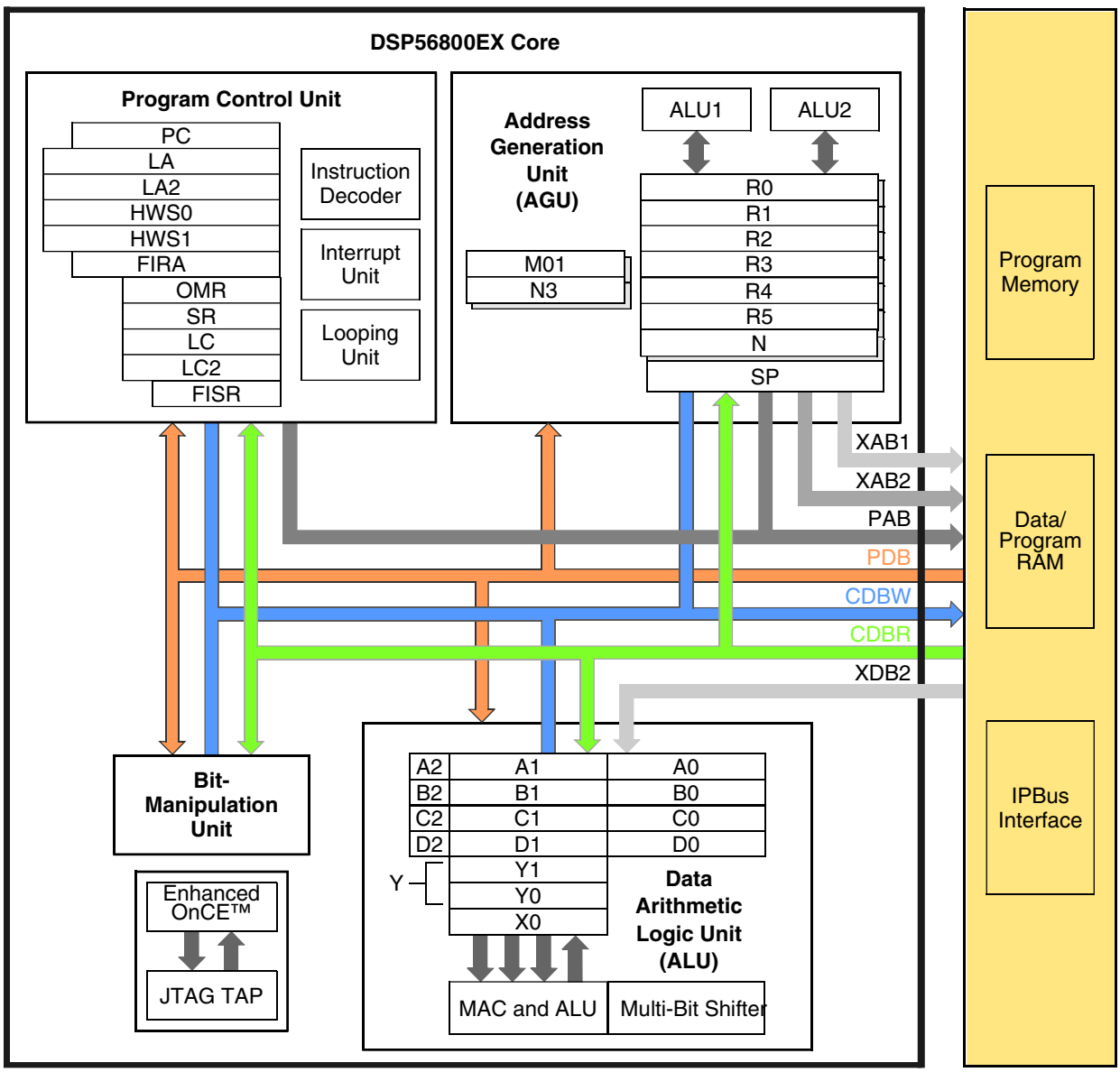


Figure 1. 56800EX basic block diagram

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
GPIOE4	51	39	25	Input/Output	Input, internal pullup enabled	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)				Input/Output		PWM module A (NanoEdge), submodule 2, output B or input capture B
(XB_IN2)				Input		Crossbar module input 2
GPIOE5	52	40	26	Input/Output	Input, internal pullup enabled	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)				Input/Output		PWM module A (NanoEdge), submodule 2, output A or input capture A
(XB_IN3)				Input		Crossbar module input 3
GPIOE6	53	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)				Input/Output		PWM module A (NanoEdge), submodule 3, output B or input capture B
(XB_IN4)				Input		Crossbar module input 4
GPIOE7	54	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E7: After reset, the default state is GPIOE7.
(PWMA_3A)				Input/Output		PWM module A (NanoEdge), submodule 3, output A or input capture A
(XB_IN5)				Input		Crossbar module input 5
GPIOF0	36	28	—	Input/Output	Input, internal pullup enabled	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)				Input		Crossbar module input 6
(SCLK1)				Input/Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	50	38	—	Input/Output	Input, internal pullup enabled	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)				Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		Crossbar module input 7
(CMPD_O)				Output		Analog comparator D output
GPIOF2	39	—	19	Input/Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)				Input/Open-drain Output		I^2C0 serial clock
(XB_OUT6)				Output		Crossbar module output 6
(MISO1)				Input/Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						is placed in the high-impedance state if the slave device is not selected.
GPIOF3	40	—	20	Input/Output	Input, internal pullup enabled	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)				Input/Open-drain Output		I^2C0 serial data line
(XB_OUT7)				Output		Crossbar module output 7
(MOSI1)				Input/Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.
GPIOF4	41	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F4: After reset, the default state is GPIOF4.
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation
(XB_OUT8)				Output		Crossbar module output 8
(PWMA_0X)				Input/Output		PWM module A (NanoEdge), submodule 0, output X or input capture X
(PWMA_FAULT6)				Input		Disable PWMA output 6
GPIOF5	42	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F5: After reset, the default state is GPIOF5.
(RXD1)				Input		SCI1 receive data input
(XB_OUT9)				Output		Crossbar module output 9
(PWMA_1X)				Input/Output		PWM module A (NanoEdge), submodule 1, output X or input capture X
(PWMA_FAULT7)				Input		Disable PWMA output 7
GPIOF6	58	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F6: After reset, the default state is GPIOF6.
(PWMA_3X)				Input/Output		PWM module A (NanoEdge), submodule 3, output X or input capture X
(XB_IN2)				Input		Crossbar module input 2
GPIOF7	59	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F7: After reset, the default state is GPIOF7.
(CMPC_O)				Output		Analog comparator C output
(SS1_B)				Input/Output		In slave mode, SS1_B indicates to the SPI1 module that the current transfer is to be received.
(XB_IN3)				Input		Crossbar module input 3
GPIOF8	6	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F8: After reset, the default state is GPIOF8.
(RXD0)				Input		SCI0 receive data input
(XB_OUT10)				Output		Crossbar module output 10
(CMPD_O)				Output		Analog comparator D output
(PWMA_2X)						PWM module A (NanoEdge), submodule 2, output X or input capture X

5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

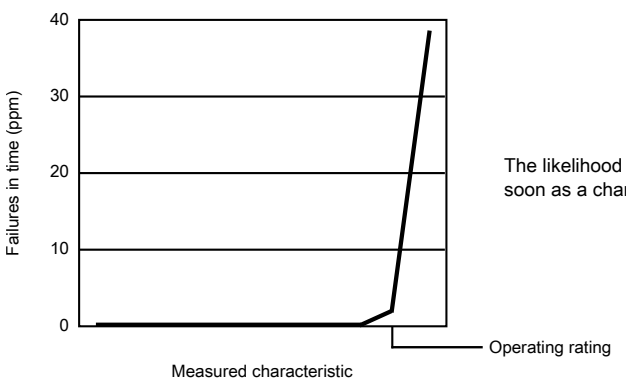
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

This is an example of an operating rating:

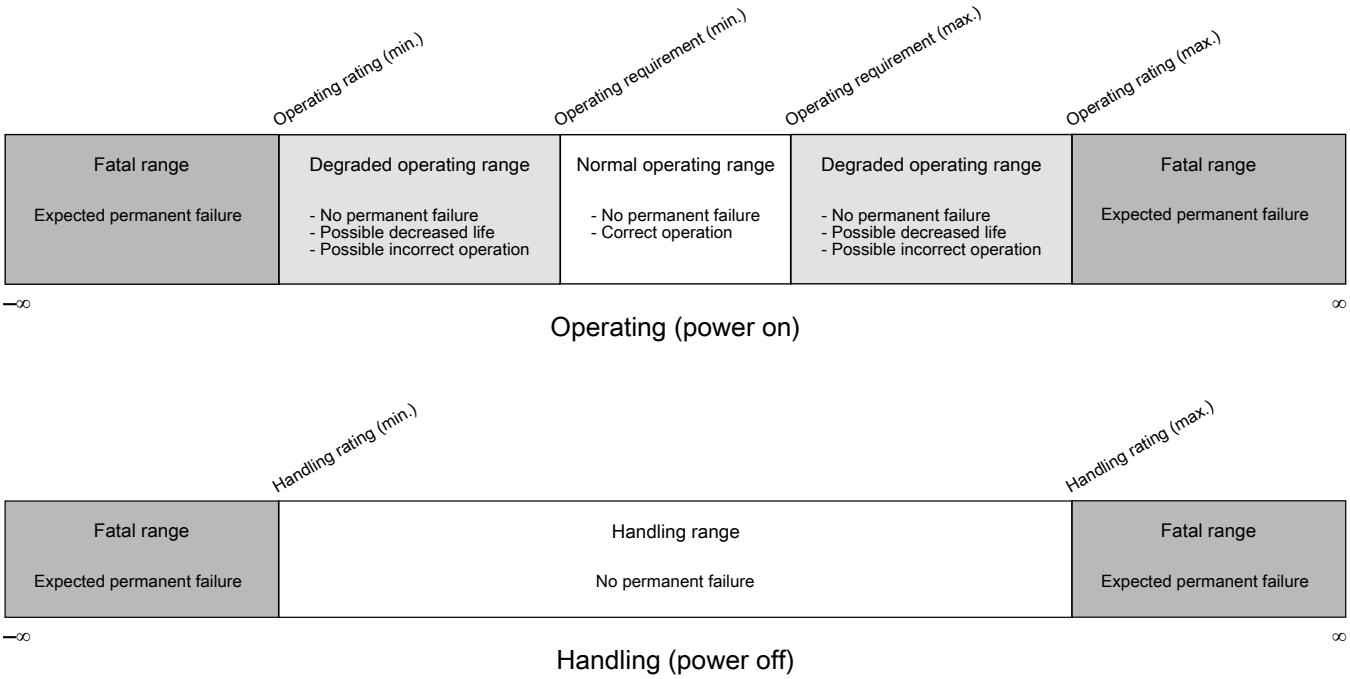
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature	T_A	V temperature	-40	105	°C
		M temperature	-40	125	
Junction Temperature	T_j	V temperature	-40	115	°C
		M temperature	-40	135	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than VDIO_MIN (= V_{SS}–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

7 General

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.) • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[2, 3] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Total IO sink current and total IO source current are limited to 75 mA each
3. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

7.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

2. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions —Forced Convection (Moving Air)* with the board horizontal.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG timing

Table 16. JTAG timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/ 8	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

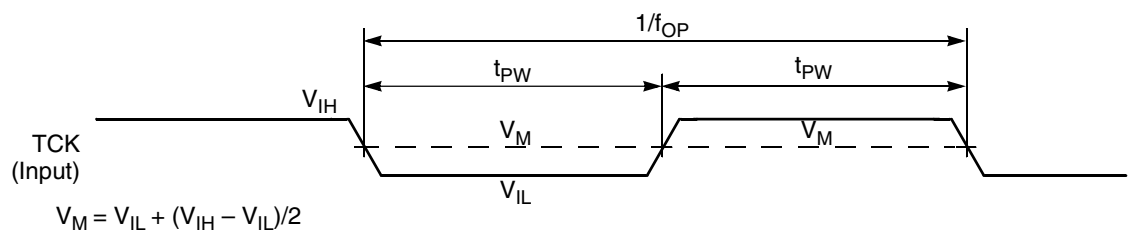


Figure 5. Test clock input timing diagram

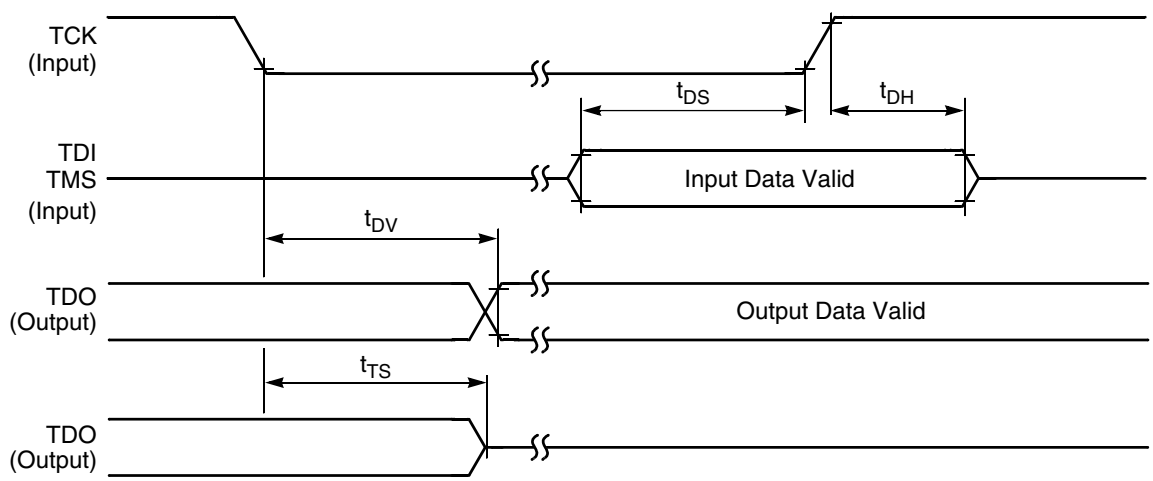


Figure 6. Test access port timing diagram

8.2 System modules

8.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the MC56F82xxx's core logic. For proper operations, the voltage regulator requires an external 2.2 µF capacitor on each V_{CAP} pin. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 17.

Table 17. Regulator 1.2 V parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600	—	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 18. Bandgap electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

8.3 Clock modules

8.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 19. External clock operation timing requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

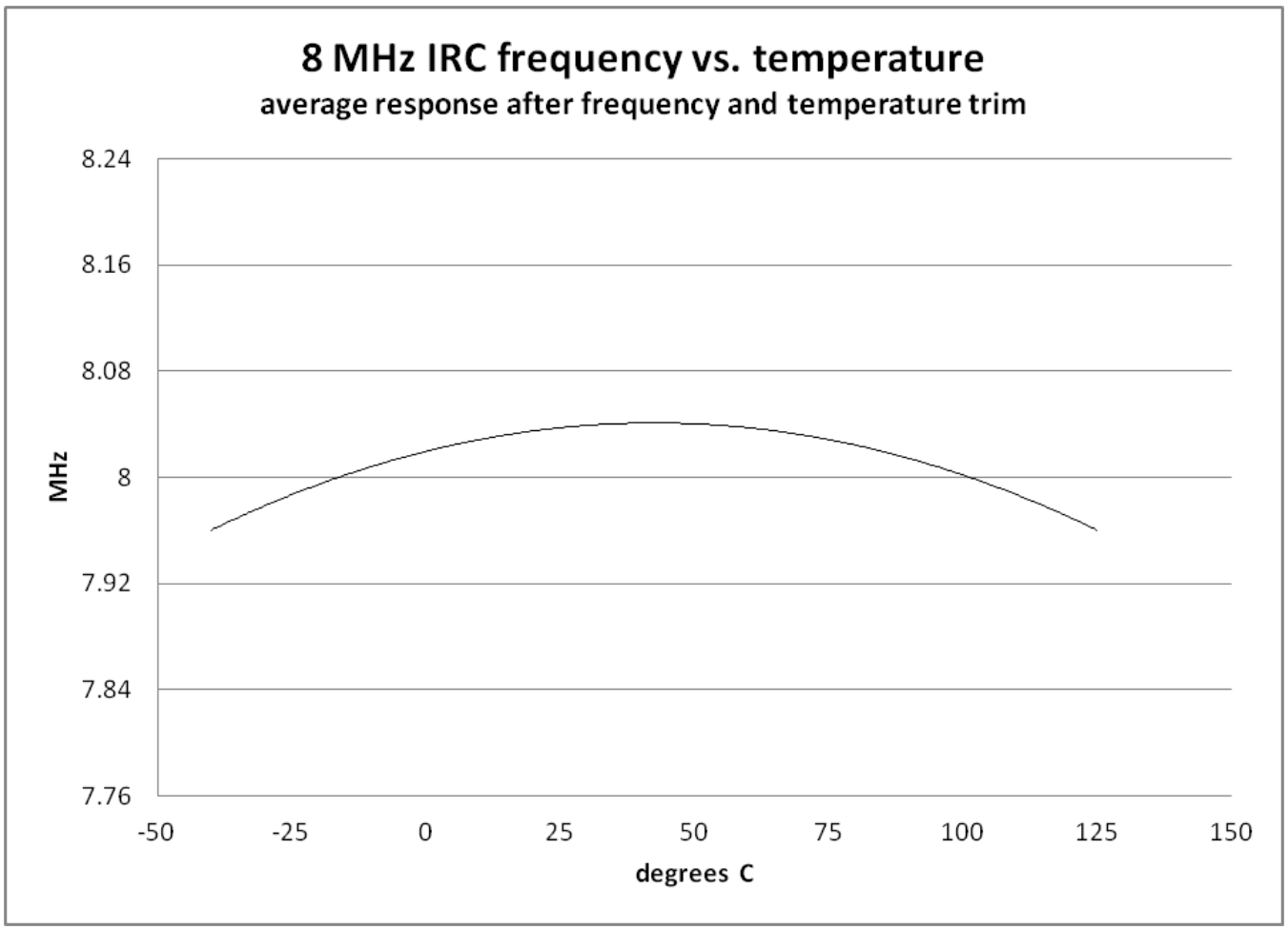


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—

Table continues on the next page...

Table 23. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

8.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

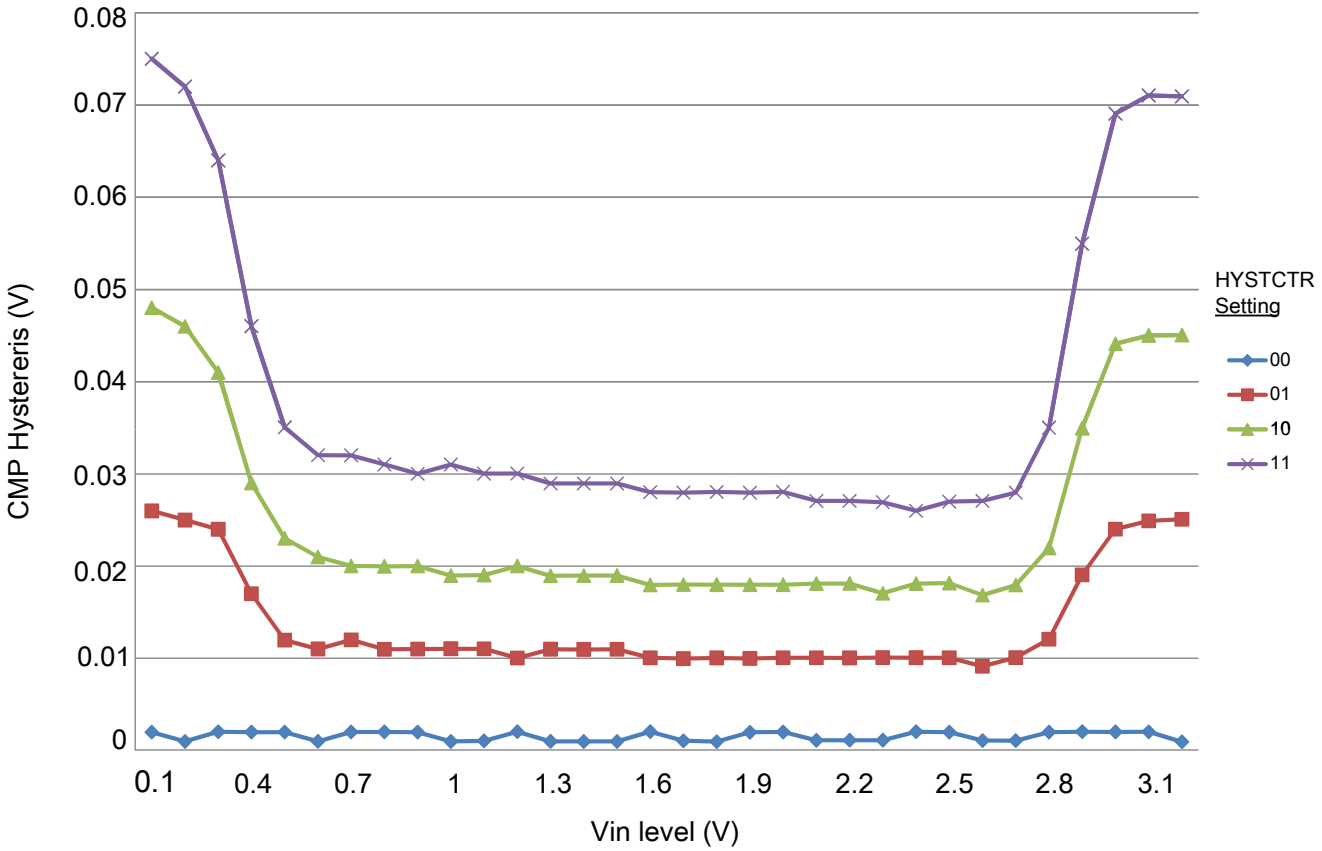


Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

11 Pinout

11.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

- The RESETB pin is a 3.3 V pin only.
- If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.
- Not all CMPD pins are not available on 48 LQFP, 32 LQFP, and 32 QFN packages.
- QSPI signals—including MISO1, MOSI1, SCLK1, and SS0_B—are not available on the 48 LQFP, 32 LQFP, and 32 QFN packages.

64 LQFP	48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	TCK	TCK	GPIOD2			
2	2	2	RESETB	RESETB	GPIOD4			
3	3	—	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	4	—	GPIOC1	GPIOC1	XTAL			
5	5	3	GPIOC2	GPIOC2	TXD0	XB_OUT11	XB_IN2	CLKO0
6	—	—	GPIOF8	GPIOF8	RXD0	XB_OUT10	CMPD_O	PWM_2X
7	6	4	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
8	7	5	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN6	EWM_OUT_B
9	—	—	GPIOA7	GPIOA7	ANA7&CMPD_IN3			
10	—	—	GPIOA6	GPIOA6	ANA6&CMPD_IN2			
11	—	—	GPIOA5	GPIOA5	ANA5&CMPD_IN1			
12	8	—	GPIOA4	GPIOA4	ANA4&CMPD_IN0			
13	9	6	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
14	10	7	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
15	11	8	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
16	12	—	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
17	—	—	GPIOB7	GPIOB7	ANB7&CMPB_IN2			
18	13	—	GPIOC5	GPIOC5	DACA_O	XB_IN7		
19	—	—	GPIOB6	GPIOB6	ANB6&CMPB_IN1			

64 LQFP	48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
60	44	28	VDD	VDD				
61	45	29	VSS	VSS				
62	46	30	TDO	TDO	GPIOD1			
63	47	31	TMS	TMS	GPIOD3			
64	48	32	TDI	TDI	GPIOD0			

11.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

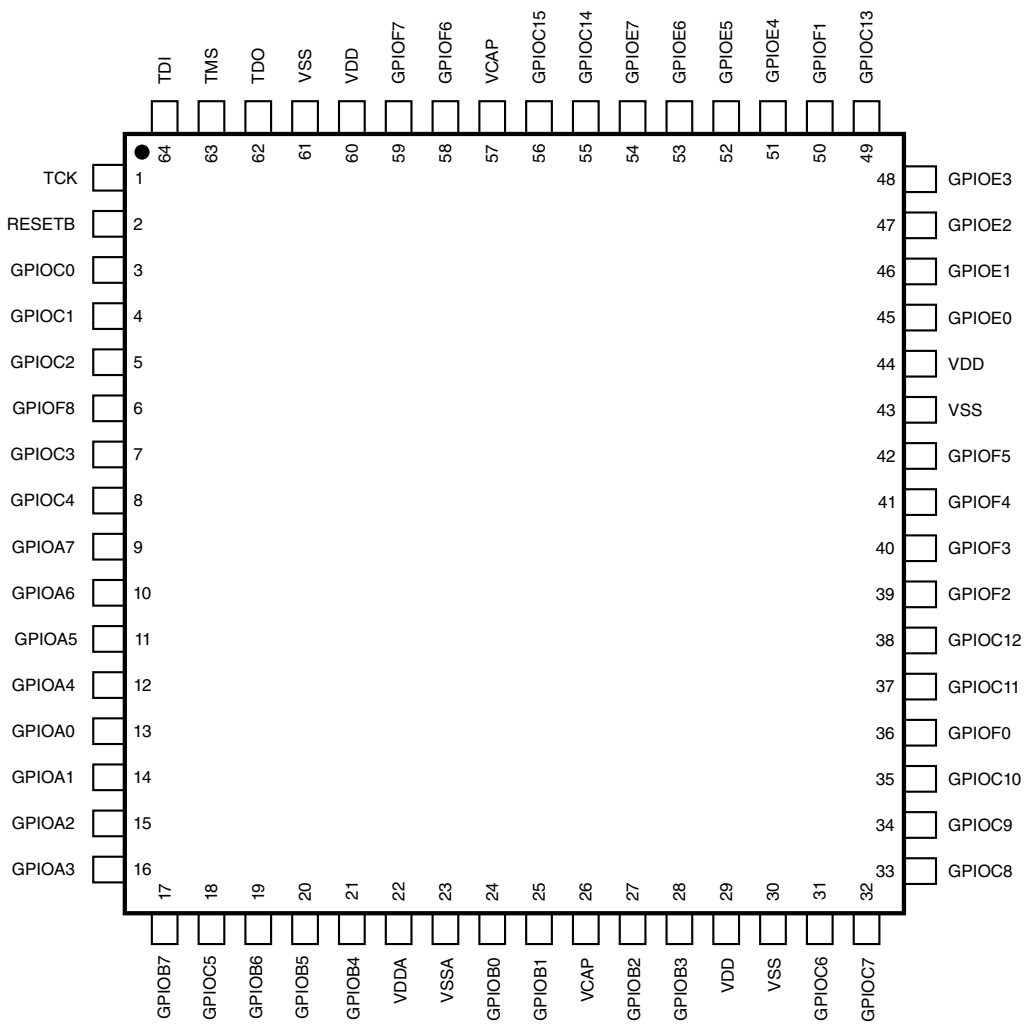


Figure 23. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev. No.	Date	Substantial Changes
2	10/2013	First public release
2.1	11/2013	• In Table 2, added DACB_O signal description. • In Obtaining package dimensions, changed 32-QFN's document number from '98ARE10566D' to '98ASA00473D'.

2.2	03/2016 - 05/2016	• Corrected document part number MC56F827XXDS to MC56F827XX.
		• In "12-bit ADC Electrical Specifications" table, corrected Max Gain Error to 0.990 to 1.010.
		• In Part identification section, in part number fields table, added the 32QFN package identifier.
		• In Electrical design considerations" section, added additional section "Power-on Reset design considerations".
		• Added new section "Power-on Reset design considerations".
		• In "Peripheral highlights" section, added
		  • Periodic Interrupt Timer (PIT) Modules
		  • External Watchdog Monitor (EWM)

3.0	09/2016	• Added products: 56F82746MLF, 56F82733MFM
		• Removed PDB (Programmable Delay Block) mentions, because PDBs are not present in these devices.
		• Added V and M temperature options to operating characteristics.
		• Moved "Signal groups" section under "MC56F827xx signal and pin descriptions" section.
		• In "Voltage and current operating ratings" section: updated note; in "Absolute Maximum Ratings" table, updated Ambient and Junction Temperature rows, also fixed broken footnotes.
		• In "Power consumption operating behaviors" section, in "Current Consumption" table: added columns and data for Maximum at 3.6V, 125°C", fixed broken footnotes.
		• In "Thermal operating requirements" section, updated Die junction temperature and Ambient temperature requirements.
		• In "Relaxation Oscillator Timing" section, in "Relaxation Oscillator Electrical Specifications" table:
		  • Added data for "-40°C to 125°C" temperature range.
		  • For "8 MHz Output Frequency, Standby Mode frequency", 2 corrections were made.
		  • Fixed broken footnotes.