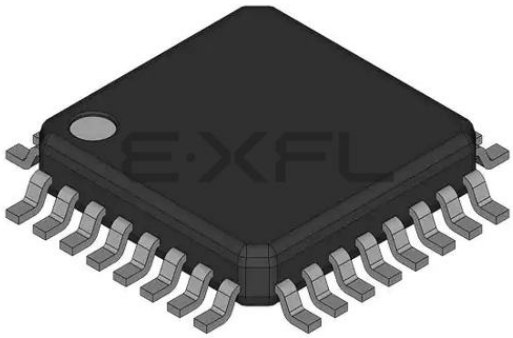

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f82733vlc

Table of Contents

1 Overview....4
1.1 MC56F827xx Product Family....4
1.2 56800EX 32-bit Digital Signal Controller (DSC) core....5
1.3 Operation Parameters....6
1.4 On-Chip Memory and Memory Protection....6
1.5 Interrupt Controller....7
1.6 Peripheral highlights....7
1.7 Block diagrams....13
2 MC56F827xx signal and pin descriptions....16
2.1 Signal groups....25
3 Ordering parts....25
3.1 Determining valid orderable parts....25
4 Part identification....25
4.1 Description....26
4.2 Format....26
4.3 Fields....26
4.4 Example....26
5 Terminology and guidelines....27
5.1 Definition: Operating requirement....27
5.2 Definition: Operating behavior....27
5.3 Definition: Attribute....27
5.4 Definition: Rating....28
5.5 Result of exceeding a rating....28
5.6 Relationship between ratings and operating requirements....28
5.7 Guidelines for ratings and operating requirements....29
5.8 Definition: Typical value....29
5.9 Typical value conditions....30
6 Ratings....31
6.1 Thermal handling ratings....31
6.2 Moisture handling ratings....31
6.3 ESD handling ratings....31
6.4 Voltage and current operating ratings....32
7 General....33
7.1 General characteristics....33
7.2 AC electrical characteristics....34
7.3 Nonswitching electrical specifications....35
7.4 Switching specifications....41
7.5 Thermal specifications....42
8 Peripheral operating requirements and behaviors....44
8.1 Core modules....44
8.2 System modules....45
8.3 Clock modules....45
8.4 Memories and memory interfaces....48
8.5 Analog....50
8.6 PWMs and timers....56
8.7 Communication interfaces....57
9 Design Considerations....63
9.1 Thermal design considerations....63
9.2 Electrical design considerations....65
9.3 Power-on Reset design considerations....66
10 Obtaining package dimensions....68
11 Pinout....69
11.1 Signal Multiplexing and Pin Assignments....69
11.2 Pinout diagrams....71
12 Product documentation....73
13 Revision History....74

Table 1. MC56F827xx Family (continued)

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Analog Comparators (CMP)	4	4	3	3	4	4	3	3	4	4	3	3
QSCI	2	2	1	1	2	2	1	1	2	2	1	1
QSPI	2	1	1	1	2	1	1	1	2	1	1	1
I2C/SMBus	1	1	1	1	1	1	1	1	1	1	1	1
MSCAN	1	1	0	0	1	1	0	0	1	1	0	0
GPIO	54	39	26	26	54	39	26	26	54	39	26	26
Package pin count	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN
AEC-Q100[3]	Yes	Yes	No	No	Yes	Yes	No	No	Yes	Yes	No	No

1. Temperature options
   V: -40°C to 105°C
   M: -40°C to 125°C
2. Input capture shares the pin with cooresponding PWM channels.
3. Qualification aligned to AEC-Q100

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 50 MHz operation in normal mode and 100 MHz operation in fast mode
- Operation ambient temperature:
  V Temperature option:-40 ºC to 105ºC
  M Temperature option:-40 ºC to 125ºC
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory

- Up to 64 KB program/data flash memory
- Up to 8 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.

1.6.3 Periodic Interrupt Timer (PIT) Modules

- 16-bit counter with programmable count modulo
- PIT0 is master and PIT1 is slave (if synchronizing both PITs)
- The output signals of both PIT0 and PIT1 are internally connected to a peripheral crossbar module
- Can run when the CPU is in Wait/Stop modes. Can also wake up the CPU from Wait/Stop modes.
- In addition to its existing bus clock (up to 50 MHz), 3 alternate clock sources for the counter clock are available:
  - Crystal oscillator output
  - 8 MHz / 400 kHz ROSC (relaxation oscillator output)
  - On-chip low-power 200 kHz oscillator

1.6.4 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, EWM, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.6 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
    - External crystal oscillator/external clock source

2 MC56F827xx signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIOx_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA outputs, in cases where the fault conditions originate off-chip.

For the MC56F827xx products, which use 64-pin LQFP, 48-pin LQFP and 32-pin packages:

Table 2. Signal descriptions

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
V_{DD}	29	—	—	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
	44	32	—			
	60	44	28			
V_{SS}	30	22	14	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
	43	31	—			
	61	45	29			
V_{DDA}	22	15	9	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	23	16	10	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	26	19	—	On-chip regulator output	On-chip regulator output	Connect a 2.2 µF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation.
	57	43	27			
TDI	64	48	32	Input	Input, internal pullup enabled	Test Data Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)				Input/Output		GPIO Port D0
TDO	62	46	30	Output	Output	Test Data Output — It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO
(GPIOD1)				Input/Output	Output	GPIO Port D1

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						is placed in the high-impedance state if the slave device is not selected.
GPIOF3	40	—	20	Input/Output	Input, internal pullup enabled	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)				Input/Open-drain Output		I^2C0 serial data line
(XB_OUT7)				Output		Crossbar module output 7
(MOSI1)				Input/Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.
GPIOF4	41	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F4: After reset, the default state is GPIOF4.
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation
(XB_OUT8)				Output		Crossbar module output 8
(PWMA_0X)				Input/Output		PWM module A (NanoEdge), submodule 0, output X or input capture X
(PWMA_FAULT6)				Input		Disable PWMA output 6
GPIOF5	42	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F5: After reset, the default state is GPIOF5.
(RXD1)				Input		SCI1 receive data input
(XB_OUT9)				Output		Crossbar module output 9
(PWMA_1X)				Input/Output		PWM module A (NanoEdge), submodule 1, output X or input capture X
(PWMA_FAULT7)				Input		Disable PWMA output 7
GPIOF6	58	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F6: After reset, the default state is GPIOF6.
(PWMA_3X)				Input/Output		PWM module A (NanoEdge), submodule 3, output X or input capture X
(XB_IN2)				Input		Crossbar module input 2
GPIOF7	59	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F7: After reset, the default state is GPIOF7.
(CMPC_O)				Output		Analog comparator C output
(SS1_B)				Input/Output		In slave mode, SS1_B indicates to the SPI1 module that the current transfer is to be received.
(XB_IN3)				Input		Crossbar module input 3
GPIOF8	6	—	—	Input/Output	Input, internal pullup enabled	GPIO Port F8: After reset, the default state is GPIOF8.
(RXD0)				Input		SCI0 receive data input
(XB_OUT10)				Output		Crossbar module output 10
(CMPD_O)				Output		Analog comparator D output
(PWMA_2X)						PWM module A (NanoEdge), submodule 2, output X or input capture X

5 Terminology and guidelines

5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

5.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

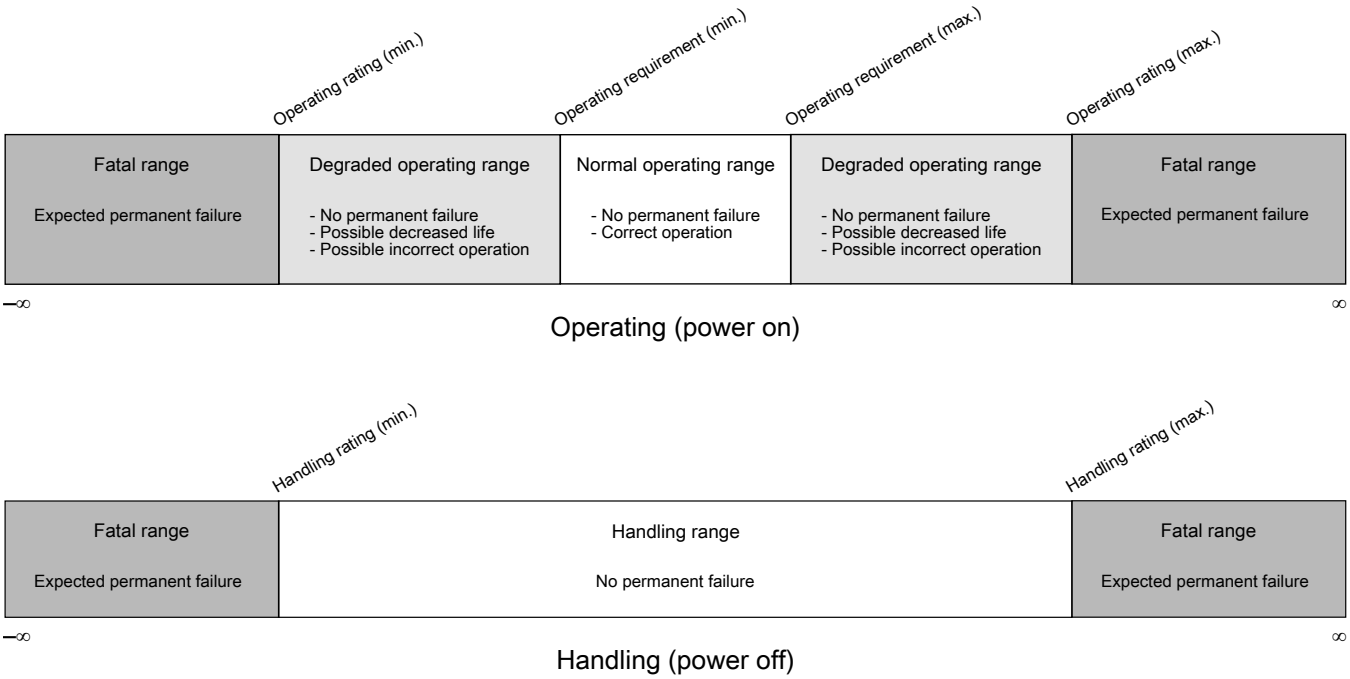
This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

5.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

7.4.2 General switching timing

Table 14. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	2
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	3

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. 75 pF load
3. 15 pF load

7.5 Thermal specifications

7.5.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description		Min	Max	Unit
T_J	Die junction temperature	V	–40	115	°C
		M	–40	135	°C
T_A	Ambient temperature	V	–40	105	°C
		M	–40	125	°C

7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power

Table 22. Relaxation Oscillator Electrical Specifications (continued)

Characteristic		Symbol	Min	Typ	Max	Unit
	-40°C to 105°C		7.76	8	8.24	MHz
	-40°C to 125°C		7.60	8	8.32	MHz
Standby Mode (IRC trimmed @ 8 MHz)	-40°C to 105°C		248	405	562	kHz
	-40°C to 125°C		198	405	702	kHz
8 MHz Frequency Variation over 25°C						
RUN Mode	0°C to 105°C			+/-1.5	+/-2	%
	-40°C to 105°C			+/-1.5	+/-3	%
	-40°C to 125°C			+/-1.5	-5 to +4	%
200 kHz Output Frequency[1]						
RUN Mode	-40°C to 105°C		194	200	206	kHz
	-40°C to 125°C		192	200	208	kHz
200 kHz Output Frequency Variation over 25°C						
RUN Mode	0°C to 85°C			+/-1.5	+/-2	%
	-40°C to 105°C			+/-1.5	+/-3	%
	-40°C to 125°C			+/-1.5	+/-4	%
Stabilization Time	8 MHz output[2]	tstab		0.12		µs
	200 kHz output[3]			10		µs
Output Duty Cycle			48	50	52	%

1. Frequency after factory trim
2. Standby to run mode transition
3. Power down to run mode transition

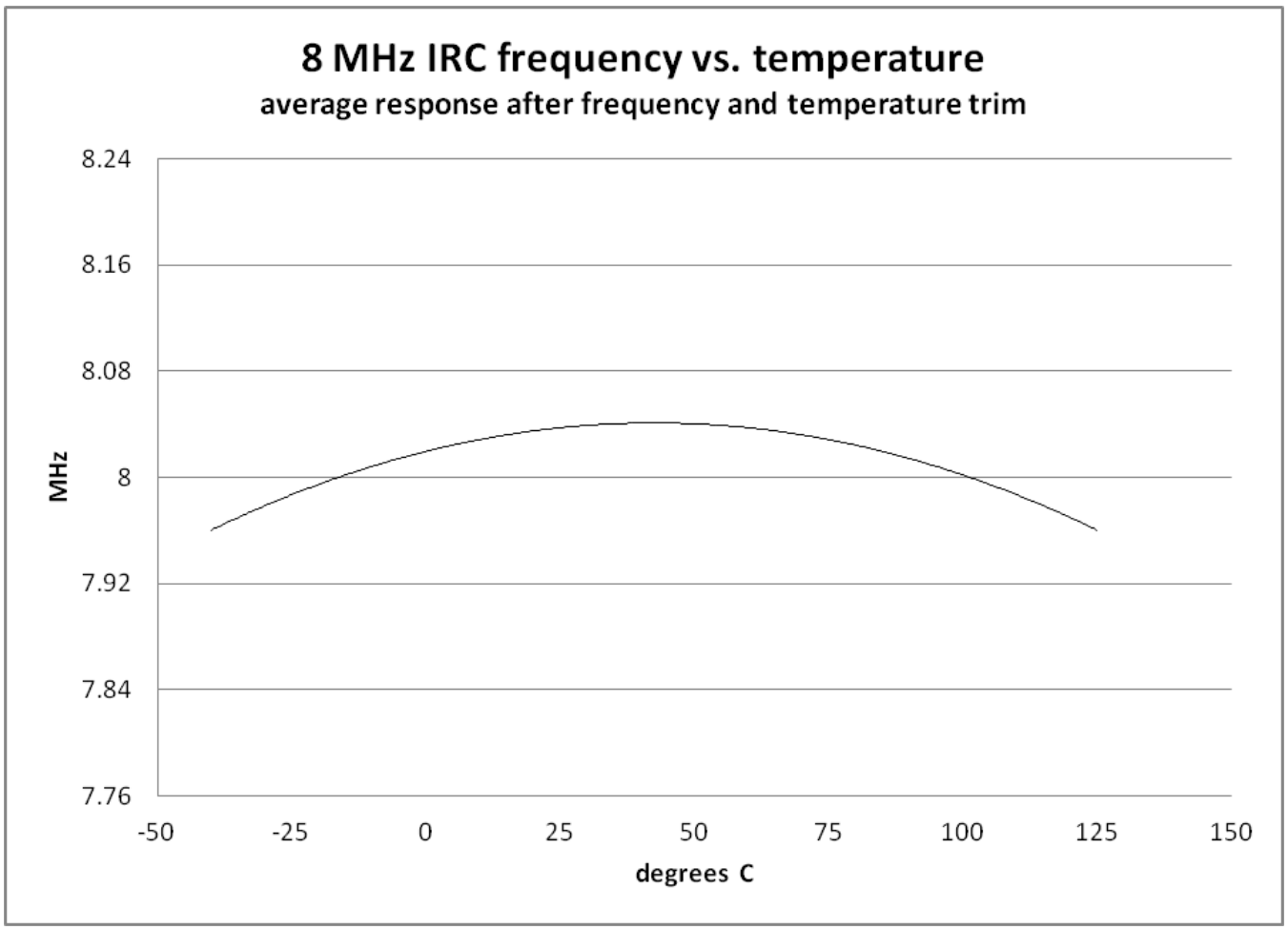


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—

Table continues on the next page...

Table 27. 12-bit ADC Electrical Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Spurious Free Dynamic Range	SFDR		77		dB
Signal to Noise plus Distortion	SINAD		66		dB
Effective Number of Bits	ENOB		—		bits
Gain = 1x (Fully Differential/Unipolar)			10.6		
Gain = 2x (Fully Differential/Unipolar)			—		
Gain = 4x (Fully Differential/Unipolar)			10.3		
Gain = 1x (Single Ended)			10.6		
Gain = 2x (Single Ended)			10.4		
Gain = 4x (Single Ended)			10.2		
Variation across channels[10]			0.1		
ADC Inputs					
Input Leakage Current	I_{IN}		1		nA
Temperature sensor slope	T_{SLOPE}		1.7		mV/°C
Temperature sensor voltage at 25 °C	V_{TEMP25}		0.82		V
Disturbance					
Input Injection Current [11]	I_{INJ}			+/-3	mA
Channel to Channel Crosstalk[12]	ISOXTLK		-82		dB
Memory Crosstalk[13]	MEMXTLK		-71		dB
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

1. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed
2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA}, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

8.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	—	25	50	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)[3]	—	60	200	ns
	Analog comparator initialization delay[4]	—	40	—	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
	6-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	V_{DDA}	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Measured with input voltage range limited to 0 to V_{DD}
2. Measured with input voltage range limited to $0.7 \le Vin \le V_{DD}-0.8$
3. Input voltage range: $0.1V_{DD} \le Vin \le 0.9V_{DD}$, step = ±100mV, across all temperature. Does not include PCB and PAD delay.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

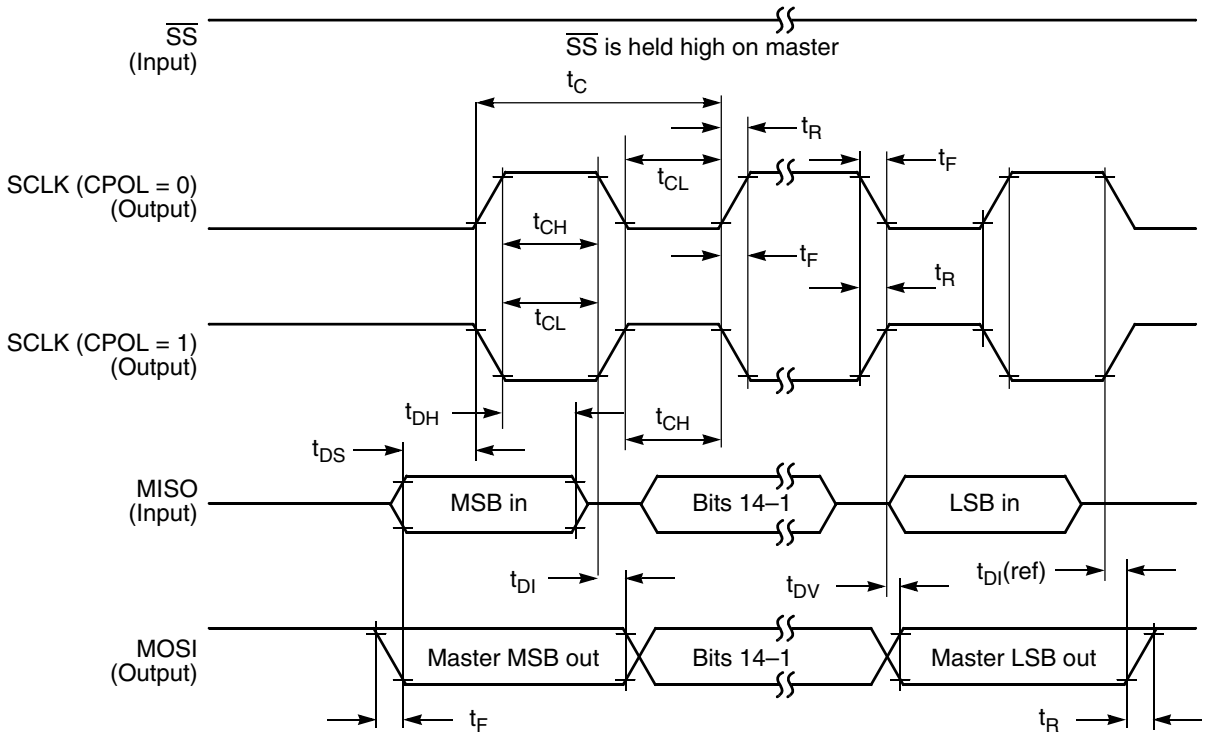


Figure 13. SPI master timing (CPHA = 0)

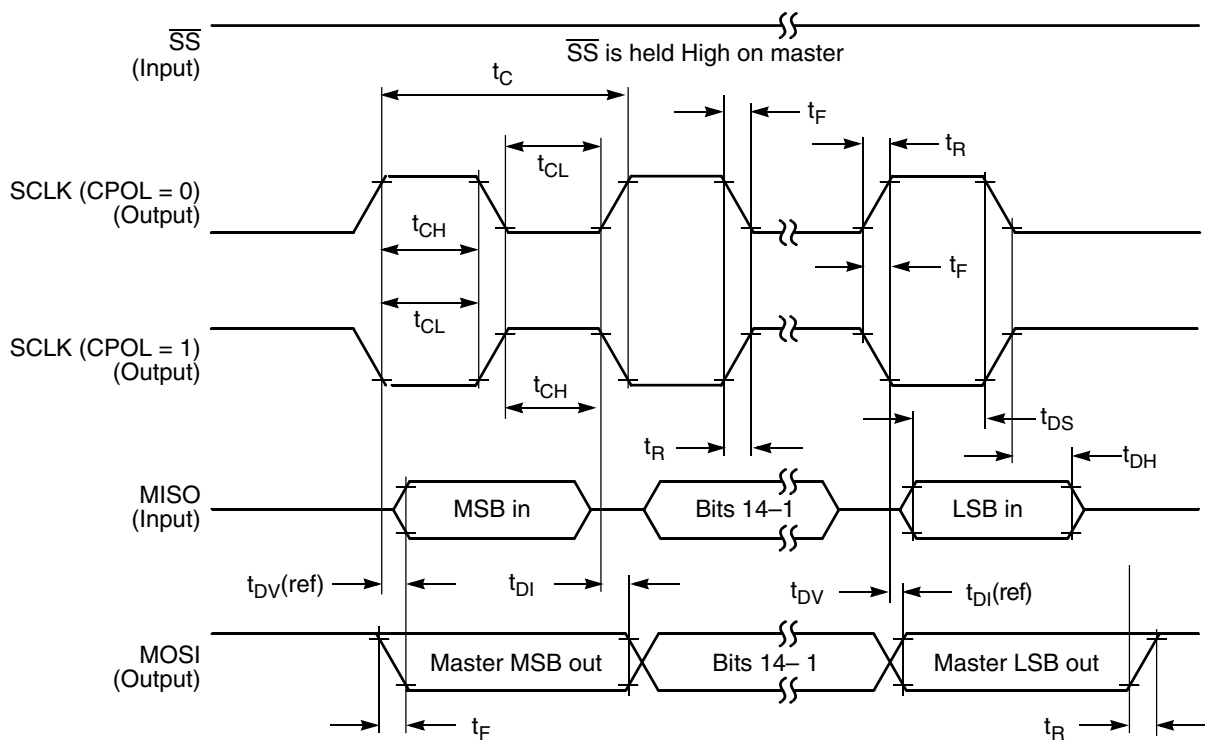


Figure 14. SPI master timing (CPHA = 1)

9.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA}. Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.

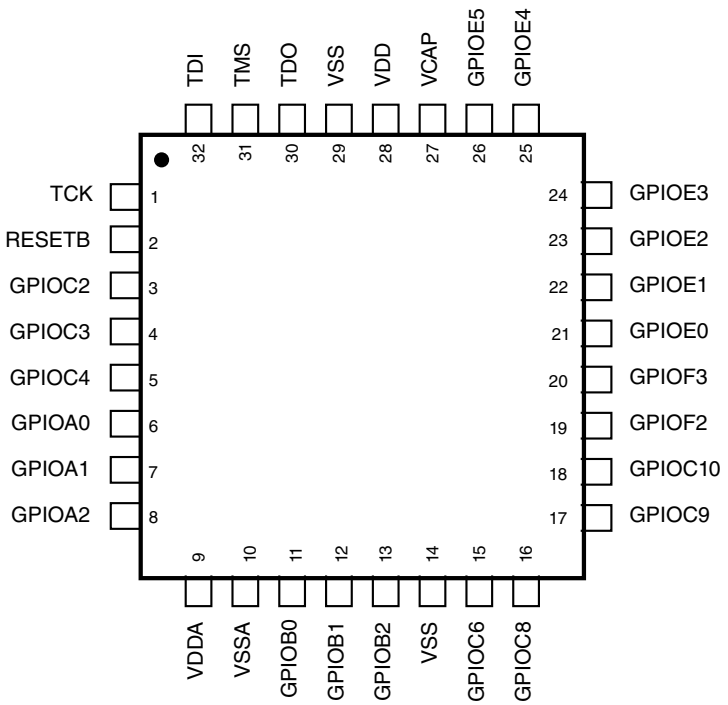


Figure 25. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 36 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 36. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F827xx Reference Manual	Detailed functional description and programming model	MC56F827XXRM
MC56F827xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F827XXDS
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev. No.	Date	Substantial Changes
2	10/2013	First public release
2.1	11/2013	• In Table 2, added DACB_O signal description. • In Obtaining package dimensions, changed 32-QFN's document number from '98ARE10566D' to '98ASA00473D'.

2.2	03/2016 - 05/2016	• Corrected document part number MC56F827XXDS to MC56F827XX.
		• In "12-bit ADC Electrical Specifications" table, corrected Max Gain Error to 0.990 to 1.010.
		• In Part identification section, in part number fields table, added the 32QFN package identifier.
		• In Electrical design considerations" section, added additional section "Power-on Reset design considerations".
		• Added new section "Power-on Reset design considerations".
		• In "Peripheral highlights" section, added
		  • Periodic Interrupt Timer (PIT) Modules
		  • External Watchdog Monitor (EWM)

3.0	09/2016	• Added products: 56F82746MLF, 56F82733MFM
		• Removed PDB (Programmable Delay Block) mentions, because PDBs are not present in these devices.
		• Added V and M temperature options to operating characteristics.
		• Moved "Signal groups" section under "MC56F827xx signal and pin descriptions" section.
		• In "Voltage and current operating ratings" section: updated note; in "Absolute Maximum Ratings" table, updated Ambient and Junction Temperature rows, also fixed broken footnotes.
		• In "Power consumption operating behaviors" section, in "Current Consumption" table: added columns and data for Maximum at 3.6V, 125°C", fixed broken footnotes.
		• In "Thermal operating requirements" section, updated Die junction temperature and Ambient temperature requirements.
		• In "Relaxation Oscillator Timing" section, in "Relaxation Oscillator Electrical Specifications" table:
		  • Added data for "-40°C to 125°C" temperature range.
		  • For "8 MHz Output Frequency, Standby Mode frequency", 2 corrections were made.
		  • Fixed broken footnotes.

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Document Number MC56F827XXDS
Revision 3.0, 09/2016