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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	54
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82738vlh

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging
- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except for RESETB pin which is a 3.3 V pin only)
  - Operation ambient temperature: V temperature option: -40°C to 105°C
  - Operation ambient temperature: M temperature option: -40°C to 125°C
- 64-pin LQFP, 48-pin LQFP, 32-pin QFN, and 32-pin LQFP packages

  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.13 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC

1.6.14 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.15 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

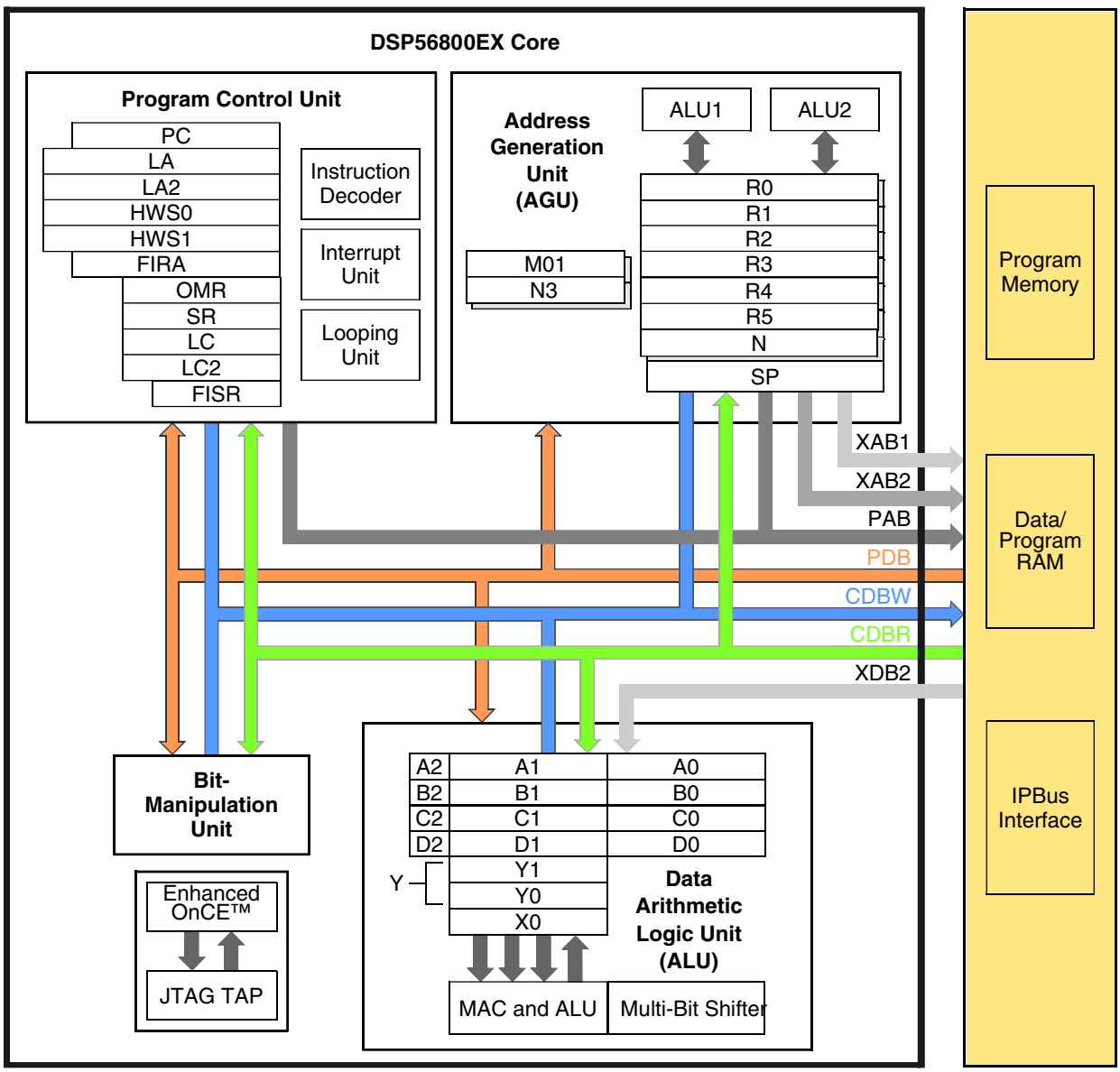


Figure 1. 56800EX basic block diagram

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
TCK	1	1	1	Input	Input, internal pullup enabled	Test Clock Input — The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK
(GPIOD2)				Input/Output		GPIO Port D2
TMS	63	47	31	Input	Input, internal pullup enabled	Test Mode Select Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to V_{DD} through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to V_{DD}.
(GPIOD3)				Input/Output		GPIO Port D3
$\overline{\text{RESET}}$ or RESETB	2	2	2	Input	Input, internal pullup enabled	Reset — A direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. After reset, the default state is $\overline{\text{RESET}}$. Recommended a capacitor of up to 0.1 µF for filtering noise.
(GPIOD4)				Input/ Opendrain Output		GPIO Port D4 $\overline{\text{RESET}}$ functionality is disabled in this mode and the device can be reset only through POR, COP reset, or software reset.
GPIOA0	13	9	6	Input/Output	Input, internal pullup enabled	GPIO Port A0
(ANA0&CMPA_IN3)				Input		ANA0 is analog input to channel 0 of ADCA; CMPA_IN3 is positive input 3 of analog comparator A. After reset, the default state is GPIOA0.
(CMPC_O)				Output		Analog comparator C output
GPIOA1	14	10	7	Input/Output	Input, internal pullup enabled	GPIO Port A1: After reset, the default state is GPIOA1.
(ANA1&CMPA_IN0)				Input		ANA1 is analog input to channel 1 of ADCA; CMPA_IN0 is negative input 0 of analog comparator A. When used as an analog input, the signal goes to ANA1 and CMPA_IN0. The ADC control register configures this input as ANA1 or CMPA_IN0.
GPIOA2	15	11	8	Input/Output	Input, internal pullup enabled	GPIO Port A2: After reset, the default state is GPIOA2.
(ANA2&VREFHA &CMPA_IN1)				Input		ANA2 is analog input to channel 2 of ADCA; VREFHA is analog reference

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
						high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1.
GPIOA3	16	12	—	Input/Output	Input, internal pullup enabled	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)				Input		ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A.
GPIOA4	12	8	—	Input/Output	Input, internal pullup enabled	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&CMPD_IN0)				Input		ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D.
GPIOA5	11	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&CMPD_IN1)				Input		ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D.
GPIOA6	10	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&CMPD_IN2)				Input		ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D.
GPIOA7	9	—	—	Input/Output	Input, internal pullup enabled	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&CMPD_IN3)				Input		ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D.
GPIOB0	24	17	11	Input/Output	Input, internal pullup enabled	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)				Input		ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0.
GPIOB1	25	18	12	Input/Output	Input, internal pullup enabled	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)				Input		ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. The ADC control register configures this input as ANB1.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
GPIOE4	51	39	25	Input/Output	Input, internal pullup enabled	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)				Input/Output		PWM module A (NanoEdge), submodule 2, output B or input capture B
(XB_IN2)				Input		Crossbar module input 2
GPIOE5	52	40	26	Input/Output	Input, internal pullup enabled	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)				Input/Output		PWM module A (NanoEdge), submodule 2, output A or input capture A
(XB_IN3)				Input		Crossbar module input 3
GPIOE6	53	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)				Input/Output		PWM module A (NanoEdge), submodule 3, output B or input capture B
(XB_IN4)				Input		Crossbar module input 4
GPIOE7	54	—	—	Input/Output	Input, internal pullup enabled	GPIO Port E7: After reset, the default state is GPIOE7.
(PWMA_3A)				Input/Output		PWM module A (NanoEdge), submodule 3, output A or input capture A
(XB_IN5)				Input		Crossbar module input 5
GPIOF0	36	28	—	Input/Output	Input, internal pullup enabled	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)				Input		Crossbar module input 6
(SCLK1)				Input/Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	50	38	—	Input/Output	Input, internal pullup enabled	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)				Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		Crossbar module input 7
(CMPD_O)				Output		Analog comparator D output
GPIOF2	39	—	19	Input/Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)				Input/Open-drain Output		I^2C0 serial clock
(XB_OUT6)				Output		Crossbar module output 6
(MISO1)				Input/Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device

Table continues on the next page...

5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

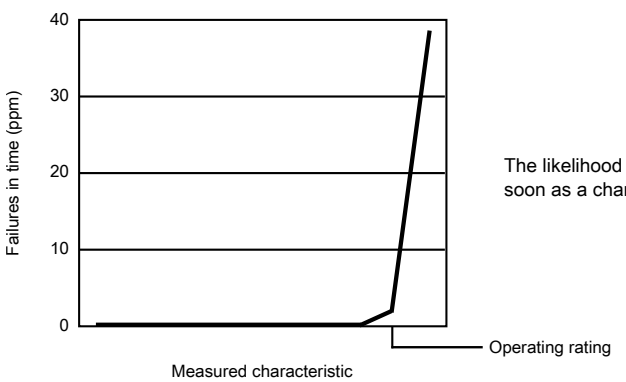
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature	T_A	V temperature	-40	105	°C
		M temperature	-40	125	
Junction Temperature	T_j	V temperature	-40	115	°C
		M temperature	-40	135	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than VDIO_MIN (= V_{SS}–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

7 General

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.) • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[2, 3] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Total IO sink current and total IO source current are limited to 75 mA each
3. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

7.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode						

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.
2. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:2 between the CPU clock and the flash clock when running with 2 MHz external clock input and CPU running at 1 MHz.

7.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

7.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

7.4 Switching specifications

7.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{BUS}	Bus clock	—	50	MHz	

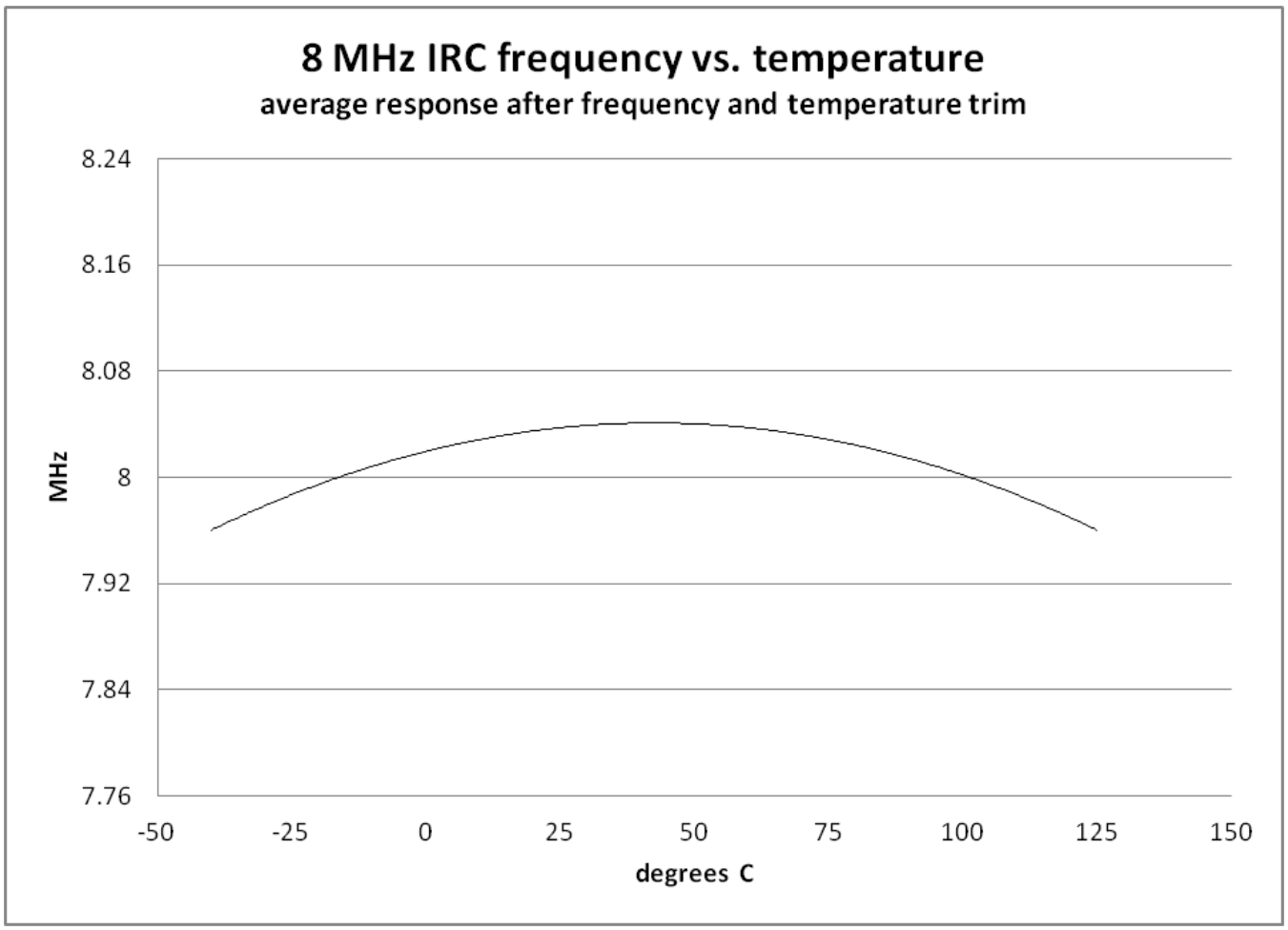


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—

Table continues on the next page...

Table 23. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

8.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

8.5 Analog

8.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 27. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	VDDA	3	3.3	3.6	V
VREFH (in external reference mode)	Vrefhx	VDDA-0.6		VDDA	V
ADC Conversion Clock[2]	f_{ADCCLK}	0.1		10	MHz
Conversion Range[3] Fully Differential Single Ended/Unipolar	R_{AD}	 – (V_{REFH} – V_{REFL}) V_{REFL}		 V_{REFH} – V_{REFL} V_{REFH}	V
Input Voltage Range (per input)[4] External Reference Internal Reference	V_{ADIN}	V_{REFL} 0		V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time[5]	t_{ADC}		8		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block)	I_{ADRUN}		1.8		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.1		µA
V_{REFH} Current (in external mode)	I_{VREFH}		190	225	µA
Accuracy (DC or Absolute)					
Integral non-Linearity[6]	INL		+/- 1.5	+/- 2.2	LSB[7]
Differential non-Linearity[6]	DNL		+/- 0.5	+/- 0.8	LSB[7]
Monotonicity		GUARANTEED			
Offset[8] Fully Differential Single Ended/Unipolar	V_{OFFSET}		 +/- 8 +/- 12		mV
Gain Error	E_{GAIN}		0.996 to1.004	0.990 to 1.010	
AC Specifications[9]					
Signal to Noise Ratio	SNR		66		dB
Total Harmonic Distortion	THD		75		dB

Table continues on the next page...

Table 27. 12-bit ADC Electrical Specifications (continued)

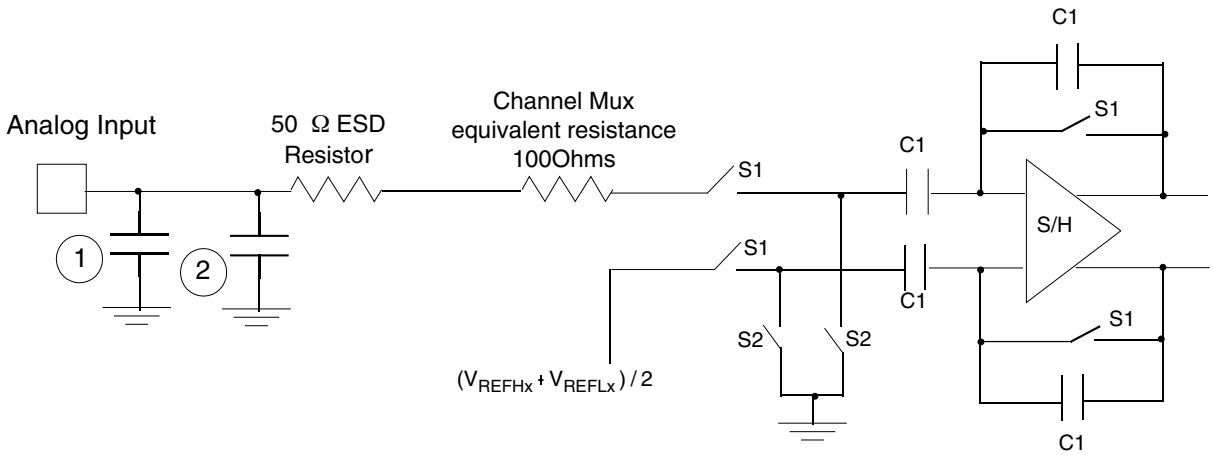
Characteristic	Symbol	Min	Typ	Max	Unit
Spurious Free Dynamic Range	SFDR		77		dB
Signal to Noise plus Distortion	SINAD		66		dB
Effective Number of Bits	ENOB		—		bits
Gain = 1x (Fully Differential/Unipolar)			10.6		
Gain = 2x (Fully Differential/Unipolar)			—		
Gain = 4x (Fully Differential/Unipolar)			10.3		
Gain = 1x (Single Ended)			10.6		
Gain = 2x (Single Ended)			10.4		
Gain = 4x (Single Ended)			10.2		
Variation across channels[10]			0.1		
ADC Inputs					
Input Leakage Current	I_{IN}		1		nA
Temperature sensor slope	T_{SLOPE}		1.7		mV/°C
Temperature sensor voltage at 25 °C	V_{TEMP25}		0.82		V
Disturbance					
Input Injection Current [11]	I_{INJ}			+/-3	mA
Channel to Channel Crosstalk[12]	ISOXTLK		-82		dB
Memory Crosstalk[13]	MEMXTLK		-71		dB
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

1. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed
2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA}, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

8.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 4.8 \times 10^{-12}} + 100\ ohm + 50\ ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

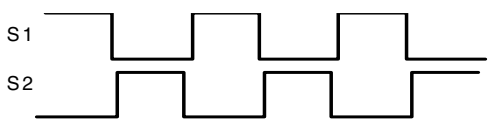


Figure 9. Equivalent circuit for A/D loading

8.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

Table 28. DAC parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pF		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words:	INL	—	+/- 3	+/- 4	LSB[3]

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	—	25	50	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)[3]	—	60	200	ns
	Analog comparator initialization delay[4]	—	40	—	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
	6-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	V_{DDA}	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Measured with input voltage range limited to 0 to V_{DD}
2. Measured with input voltage range limited to $0.7 \le Vin \le V_{DD}-0.8$
3. Input voltage range: $0.1V_{DD} \le Vin \le 0.9V_{DD}$, step = ±100mV, across all temperature. Does not include PCB and PAD delay.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

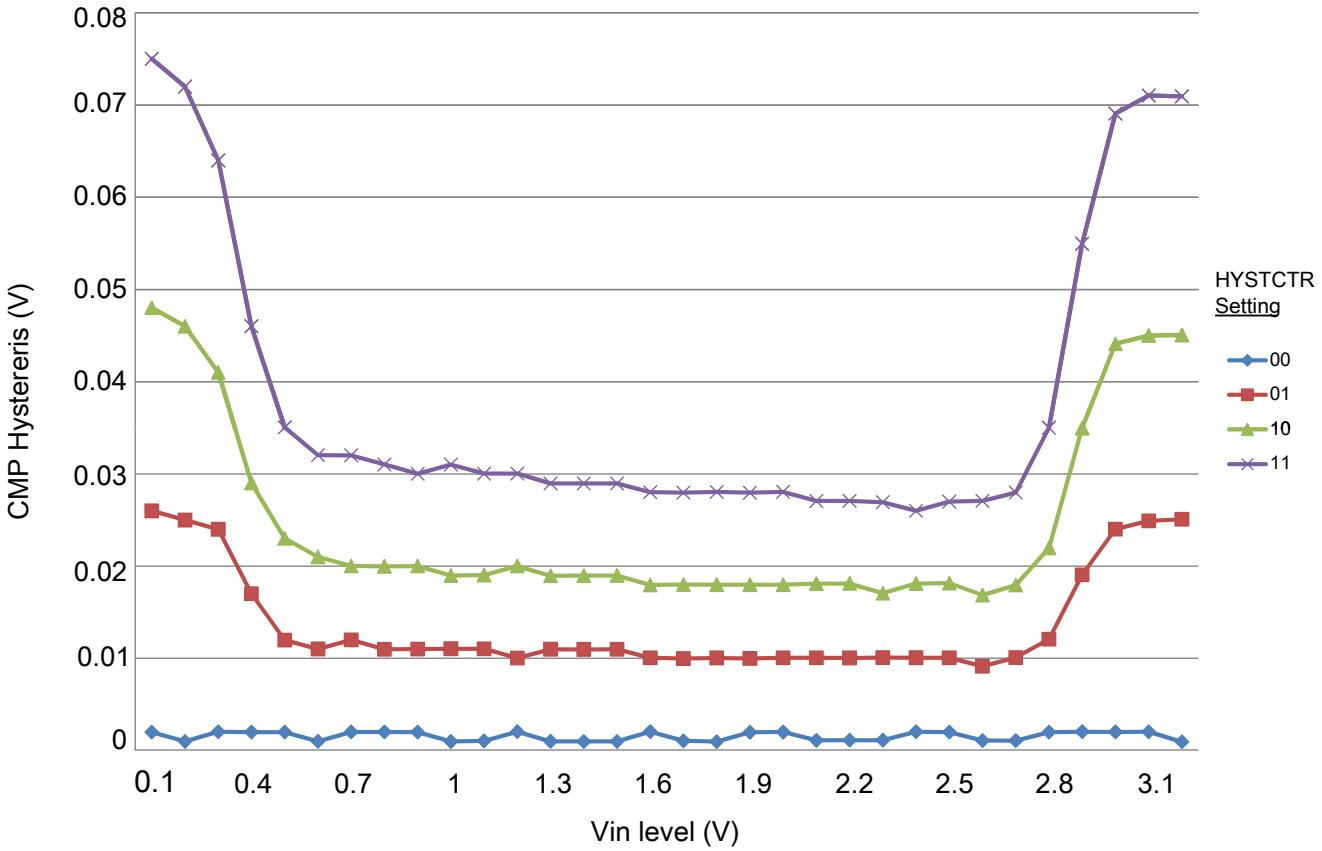


Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

Table 31. Timer timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 12
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 12
Timer output period	P_{OUT}	2T-2	—	ns	Figure 12
Timer output high/low period	P_{OUTHL}	1T-2	—	ns	Figure 12

1. T = clock cycle. For 100 MHz operation, T = 10 ns.

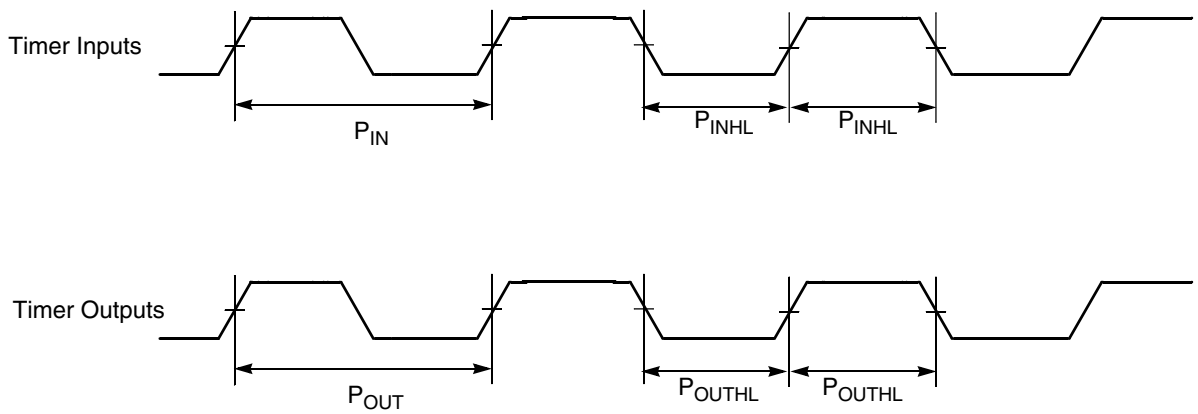


Figure 12. Timer timing

8.7 Communication interfaces

8.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 32. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	60 60	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Enable lead time Master Slave	t_{ELD}	— 20	— —	ns ns	Figure 16
Enable lag time Master Slave	t_{ELG}	— 20	— —	ns ns	Figure 16

Table continues on the next page...

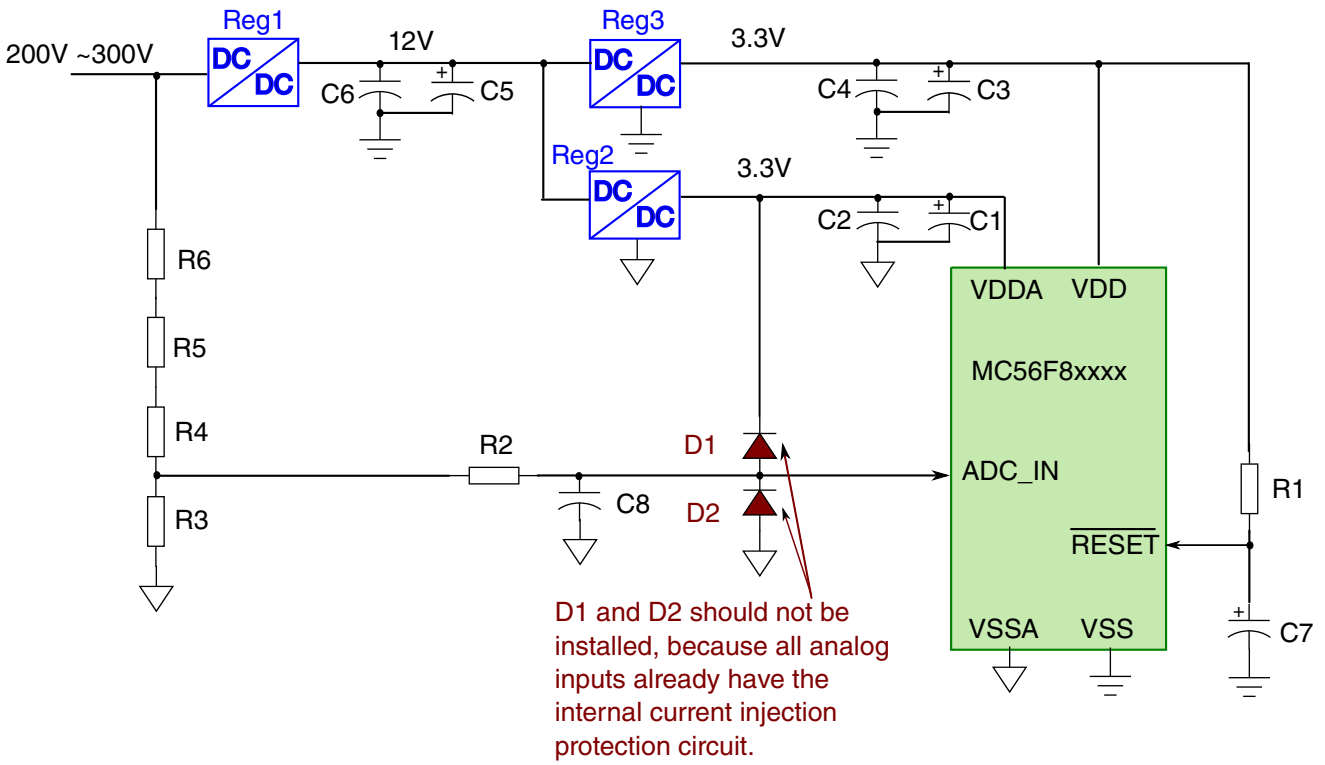


Figure 21. Protection Circuit Example

MC56F8xxxx DSC uses the 5V tolerance I/O. When the pin is configured to digital input, it can accept 5V input. Table 5. When the pin is configured to analog input, the internal integrated current injection protection circuit is enabled. The current injection protection circuit performs the same functions as external clamp diode D1 and D2 in Figure 21. As long as the source or sink current for each analog pin is less than 3 mA, then there is no damage to the device. See Table 27.

This situation could happen if diodes D1 or D2 are used for clamping; therefore in this case, the D1 and D2 clamping diodes are not recommended to be used.

NOTE

In some designs, VDD and VDDA are powered from the same power supply. In this case, above analysis and suggestions are also applicatble.

9.3.3 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.5V to 2.7V. However, the MC56F8xxxx DSC will exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the

high current will be pulled by DSC from the supply, which can cause the supply voltage to drop below the operation voltage; see the captured graph (Figure 22). This can cause the DSC fail to start up.

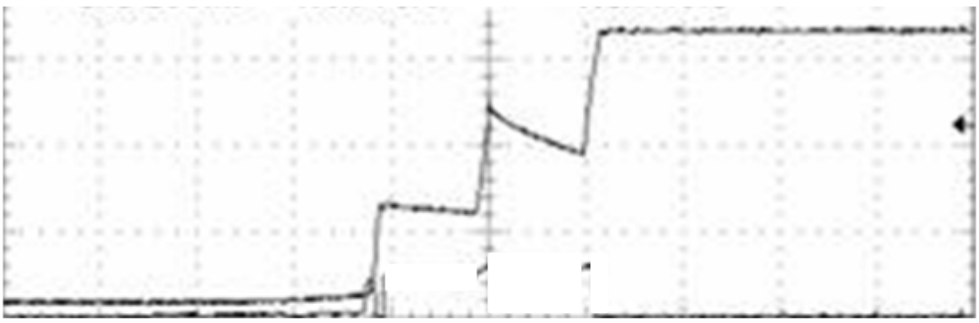


Figure 22. Supply Voltage Drop

A recommended initialization sequence during power-up is:

1. After POR is released, run a few hundred NOP instructions from the internal relaxation oscillator; this gives time for the supply voltage to stabilize.
2. Configure the peripherals (except the ADC) to the desired settings; the ADC should stay in low power mode.
3. Power up the PLL.
4. After the PLL locks, switch the clock from PLL prescale to postscale.
5. Configure the ADC.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
32LQFP	98ASH70029A
32QFN	98ASA00473D
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W