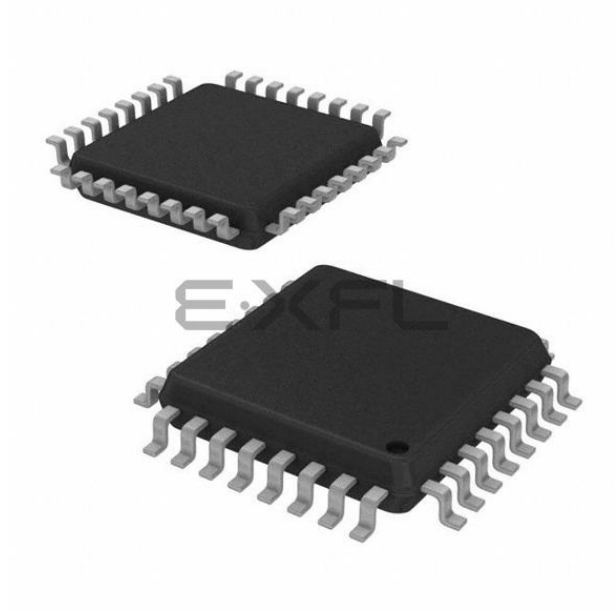

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82743vlc

Table 1. MC56F827xx Family (continued)

Feature	MC56F82											
Part Number[1]	748V LH	746V LF 746M LF	743V LC	743V FM	738V LH	736V LF	733V LC	733V FM 733M FM	728V LH	726V LF	723V LC	723V FM
Analog Comparators (CMP)	4	4	3	3	4	4	3	3	4	4	3	3
QSCI	2	2	1	1	2	2	1	1	2	2	1	1
QSPI	2	1	1	1	2	1	1	1	2	1	1	1
I2C/SMBus	1	1	1	1	1	1	1	1	1	1	1	1
MSCAN	1	1	0	0	1	1	0	0	1	1	0	0
GPIO	54	39	26	26	54	39	26	26	54	39	26	26
Package pin count	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN	64 LQFP	48 LQFP	32 LQFP	32 QFN
AEC-Q100[3]	Yes	Yes	No	No	Yes	Yes	No	No	Yes	Yes	No	No

1. Temperature options
   V: -40°C to 105°C
   M: -40°C to 125°C
2. Input capture shares the pin with cooresponding PWM channels.
3. Qualification aligned to AEC-Q100

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Up to 64 KB program/data flash memory
- Up to 8 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
    - External crystal oscillator/external clock source

  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.13 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC

1.6.14 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.15 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
DACB_O				Analog Output		12-bit digital-to-analog output
GPIOB2	27	20	13	Input/Output	Input, internal pullup enabled	GPIO Port B2: After reset, the default state is GPIOB2.
(ANB2&VERFHB &CMPC_IN3)				Input		ANB2 is analog input to channel 2 of ADCB; VREFHB is analog reference high of ADCB; CMPC_IN3 is positive input 3 of analog comparator C. When used as an analog input, the signal goes to both ANB2 and CMPC_IN3.
GPIOB3	28	21	—	Input/Output	Input, internal pullup enabled	GPIO Port B3: After reset, the default state is GPIOB3.
(ANB3&VREFLB& CMPC_IN0)				Input		ANB3 is analog input to channel 3 of ADCB; VREFLB is analog reference low of ADCB; CMPC_IN0 is negative input 0 of analog comparator C.
GPIOB4	21	14	—	Input/Output	Input, internal pullup enabled	GPIO Port B4: After reset, the default state is GPIOB4.
(ANB4&CMPC_IN 1)				Input		ANB4 is analog input to channel 4 of ADCB; CMPC_IN1 is negative input 1 of analog comparator C.
GPIOB5	20	—	—	Input/Output	Input, internal pullup enabled	GPIO Port B5: After reset, the default state is GPIOB5.
(ANB5&CMPC_IN 2)				Input		ANB5 is analog input to channel 5 of ADCB; CMPC_IN2 is negative input 2 of analog comparator C.
GPIOB6	19	—	—	Input/Output	Input, internal pullup enabled	GPIO Port B6: After reset, the default state is GPIOB6.
(ANB6&CMPB_IN 1)				Input		ANB6 is analog input to channel 6 of ADCB; CMPB_IN1 is negative input 1 of analog comparator B.
GPIOB7	17	—	—	Input/Output	Input, internal pullup enabled	GPIO Port B7: After reset, the default state is GPIOB7.
(ANB7&CMPB_IN 2)				Input		ANB7 is analog input to channel 7 of ADCB; CMPB_IN2 is negative input 2 of analog comparator B.
GPIOC0	3	3	—	Input/Output	Input, internal pullup enabled	GPIO Port C0: After reset, the default state is GPIOC0.
(EXTAL)				Analog Input		The external crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator.
(CLKIN0)				Input		External clock input 0[1]
GPIOC1	4	4	—	Input/Output	Input, internal pullup enabled	GPIO Port C1: After reset, the default state is GPIOC1.
(XTAL)				Input		The external crystal oscillator output (XTAL) connects the internal crystal

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
($\overline{SS0\_B}$)				Input/Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received.
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single wire operation
(XB_IN8)				Input		Crossbar module input 8
GPIOC8	33	25	16	Input/Output	Input, internal pullup enabled	GPIO Port C8: After reset, the default state is GPIOC8.
(MISO0)				Input/Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)				Input		SCI0 receive data input
(XB_IN9)				Input		Crossbar module input 9
(XB_OUT6)				Output		Crossbar module output 6
GPIOC9	34	26	17	Input/Output	Input, internal pullup enabled	GPIO Port C9: After reset, the default state is GPIOC9.
(SCLK0)				Input/Output		SPI0 serial clock. In master mode, SCLK0 pin is an output, clocking slaved listeners. In slave mode, SCLK0 pin is the data clock input.
(XB_IN4)				Input		Crossbar module input 4
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single wire operation
(XB_OUT8)				Output		Crossbar module output 8
GPIOC10	35	27	18	Input/Output	Input, internal pullup enabled	GPIO Port C10: After reset, the default state is GPIOC10.
(MOSI0)				Input/Output		Master out/slave in for SPI0 — In master mode, MOSI0 pin is the data output. In slave mode, MOSI0 pin is the data input.
(XB_IN5)				Input		Crossbar module input 4
(MISO0)				Input/Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(XB_OUT9)				Output		Crossbar module output 9
GPIOC11	37	29	—	Input/Output	Input, internal pullup enabled	GPIO Port C11: After reset, the default state is GPIOC11.
(CANTX)				Open-drain Output		CAN transmit data output
(SCL0)				Input/Open-drain Output		I^2C0 serial clock

Table continues on the next page...

5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

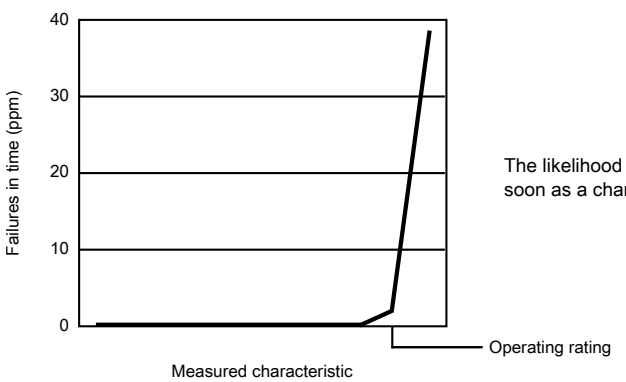
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

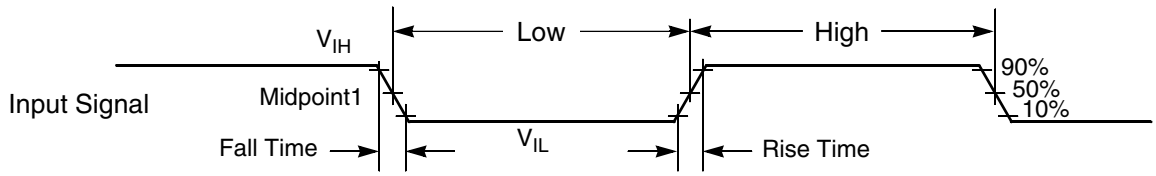
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3. Input signal measurement references

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

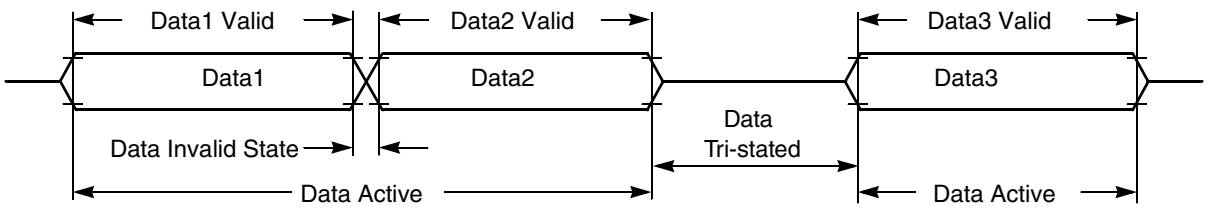


Figure 4. Signal states

7.3 Nonswitching electrical specifications

7.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA}-0.6		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V

Table continues on the next page...

Table 8. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Group 1	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
		Pin Group 2					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	—	50	kΩ	—
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	—	50	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ || C_{LD} = 400 pF
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

7.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 9. Reset, stop, wait, and interrupt timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—

Table continues on the next page...

Table 9. Reset, stop, wait, and interrupt timing (continued)

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 µF on $\overline{\text{RESET}}$.

NOTE

In Table 9, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 50MHz, T=20 ns. At 4 MHz (used coming out of reset and stop modes), T=250 ns.

Table 10. Power mode transition behavior

Symbol	Description	Min	Max	Unit	Notes[1]
T_{POR}	After a POR event, the amount of delay from when V_{DD} reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
	STOP mode to RUN mode	6.79	7.27.31	µs	2
	LPS mode to LPRUN mode	240.9	551	µs	3
	VLPS mode to VLPRUN mode	1424	1459	µs	4
	WAIT mode to RUN mode	0.570	0.620	µs	5
	LPWAIT mode to LPRUN mode	237.2	554	µs	3
	VLPWAIT mode to VLPRUN mode	1413	1500	µs	4

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is 8 MHz IRC in normal mode.
3. CPU clock = 200 KHz and 8 MHz IRC on standby. Exit by an interrupt on PORTC GPIO.
4. Using 64 KHz external clock; CPU Clock = 32KHz. Exit by an interrupt on PortC GPIO.
5. Clock configuration: CPU and system clocks= 100 MHz. Bus Clock = 50 MHz. .Exit by interrupt on PORTC GPIO

7.3.5 Power consumption operating behaviors

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN1	100 MHz	• 100 MHz Core • 50 MHz Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on	38.1	9.9	53.5	13.2	53.5	13.2

Table continues on the next page...

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C		Maximum at 3.6V, 125°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode						

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.
2. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:2 between the CPU clock and the flash clock when running with 2 MHz external clock input and CPU running at 1 MHz.

7.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

7.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

7.4 Switching specifications

7.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{BUS}	Bus clock	—	50	MHz	

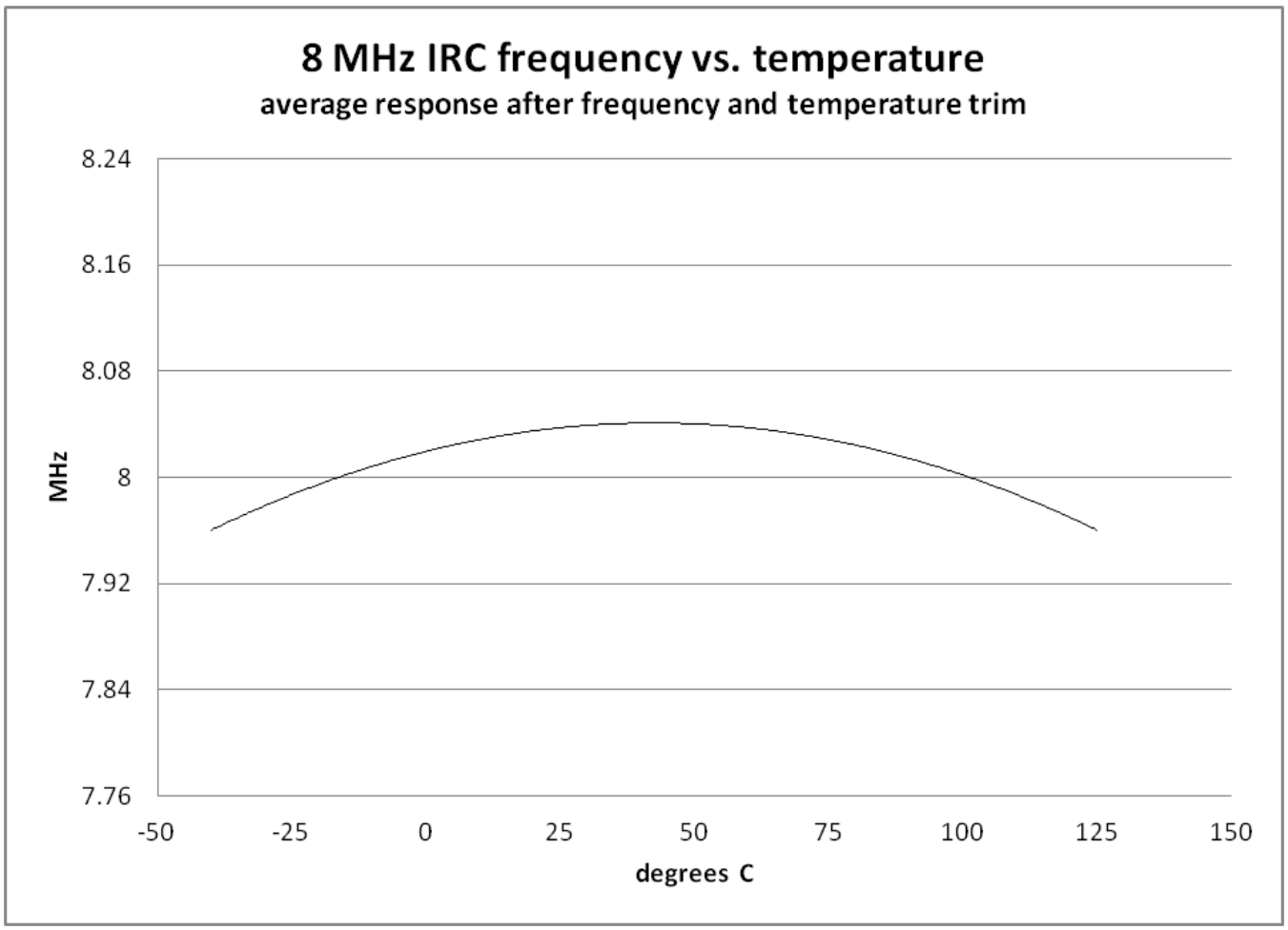


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—

Table continues on the next page...

Table 23. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

8.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

8.5 Analog

8.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 27. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	VDDA	3	3.3	3.6	V
VREFH (in external reference mode)	Vrefhx	VDDA-0.6		VDDA	V
ADC Conversion Clock[2]	f_{ADCCLK}	0.1		10	MHz
Conversion Range[3] Fully Differential Single Ended/Unipolar	R_{AD}	 – (V_{REFH} – V_{REFL}) V_{REFL}		 V_{REFH} – V_{REFL} V_{REFH}	V
Input Voltage Range (per input)[4] External Reference Internal Reference	V_{ADIN}	V_{REFL} 0		V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time[5]	t_{ADC}		8		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block)	I_{ADRUN}		1.8		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.1		µA
V_{REFH} Current (in external mode)	I_{VREFH}		190	225	µA
Accuracy (DC or Absolute)					
Integral non-Linearity[6]	INL		+/- 1.5	+/- 2.2	LSB[7]
Differential non-Linearity[6]	DNL		+/- 0.5	+/- 0.8	LSB[7]
Monotonicity		GUARANTEED			
Offset[8] Fully Differential Single Ended/Unipolar	V_{OFFSET}		 +/- 8 +/- 12		mV
Gain Error	E_{GAIN}		0.996 to1.004	0.990 to 1.010	
AC Specifications[9]					
Signal to Noise Ratio	SNR		66		dB
Total Harmonic Distortion	THD		75		dB

Table continues on the next page...

Table 32. SPI timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Clock (SCK) high time	t_{CH}		—	ns	Figure 13
Master			—	ns	Figure 14
Slave					Figure 15
					Figure 16
Clock (SCK) low time	t_{CL}	28	—	ns	Figure 16
Master		28	—	ns	
Slave					
Data set-up time required for inputs	t_{DS}	20	—	ns	Figure 13
Master		1	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Data hold time required for inputs	t_{DH}	1	—	ns	Figure 13
Master		3	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Access time (time to data active from high-impedance state)	t_A	5	—	ns	Figure 16
Slave					
Disable time (hold time to high-impedance state)	t_D	5	—	ns	Figure 16
Slave					
Data valid for outputs	t_{DV}	—		ns	Figure 13
Master		—		ns	Figure 14
Slave (after enable edge)					Figure 15
					Figure 16
Data invalid	t_{DI}	0	—	ns	Figure 13
Master		0	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Rise time	t_R	—	1	ns	Figure 13
Master		—	1	ns	Figure 14
Slave					Figure 15
					Figure 16
Fall time	t_F	—	1	ns	Figure 13
Master		—	1	ns	Figure 14
Slave					Figure 15
					Figure 16

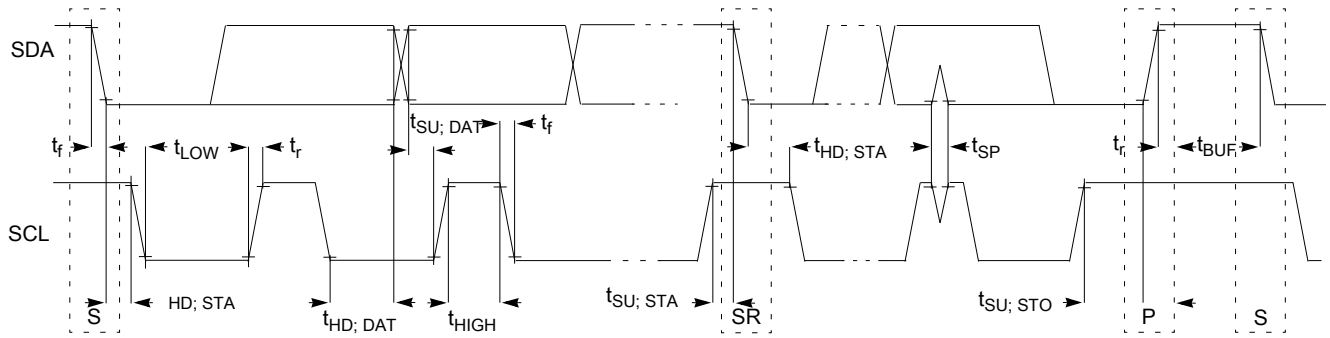


Figure 20. Timing definition for fast and standard mode devices on the I^2C bus

9 Design Considerations

9.1 Thermal design considerations

An estimate of the chip junction temperature (TJ) can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which TJ value is closer to the application depends on the power dissipated by other components on the board.

- The TJ value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The TJ value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

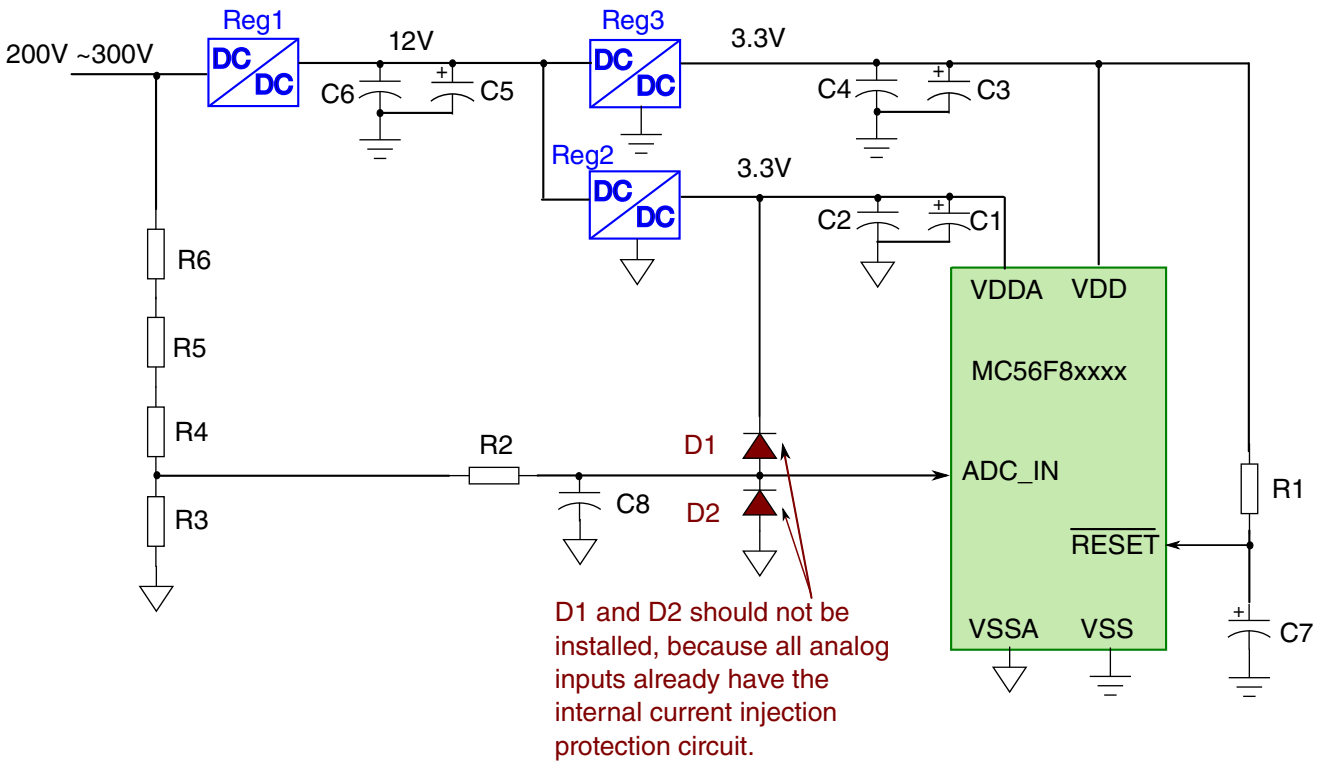


Figure 21. Protection Circuit Example

MC56F8xxxx DSC uses the 5V tolerance I/O. When the pin is configured to digital input, it can accept 5V input. Table 5. When the pin is configured to analog input, the internal integrated current injection protection circuit is enabled. The current injection protection circuit performs the same functions as external clamp diode D1 and D2 in Figure 21. As long as the source or sink current for each analog pin is less than 3 mA, then there is no damage to the device. See Table 27.

This situation could happen if diodes D1 or D2 are used for clamping; therefore in this case, the D1 and D2 clamping diodes are not recommended to be used.

NOTE

In some designs, VDD and VDDA are powered from the same power supply. In this case, above analysis and suggestions are also applicatble.

9.3.3 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.5V to 2.7V. However, the MC56F8xxxx DSC will exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the

11 Pinout

11.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

- The RESETB pin is a 3.3 V pin only.
- If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.
- Not all CMPD pins are not available on 48 LQFP, 32 LQFP, and 32 QFN packages.
- QSPI signals—including MISO1, MOSI1, SCLK1, and SS0_B—are not available on the 48 LQFP, 32 LQFP, and 32 QFN packages.

64 LQFP	48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	TCK	TCK	GPIOD2			
2	2	2	RESETB	RESETB	GPIOD4			
3	3	—	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	4	—	GPIOC1	GPIOC1	XTAL			
5	5	3	GPIOC2	GPIOC2	TXD0	XB_OUT11	XB_IN2	CLKO0
6	—	—	GPIOF8	GPIOF8	RXD0	XB_OUT10	CMPD_O	PWM_2X
7	6	4	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
8	7	5	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN6	EWM_OUT_B
9	—	—	GPIOA7	GPIOA7	ANA7&CMPD_IN3			
10	—	—	GPIOA6	GPIOA6	ANA6&CMPD_IN2			
11	—	—	GPIOA5	GPIOA5	ANA5&CMPD_IN1			
12	8	—	GPIOA4	GPIOA4	ANA4&CMPD_IN0			
13	9	6	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
14	10	7	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
15	11	8	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
16	12	—	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
17	—	—	GPIOB7	GPIOB7	ANB7&CMPB_IN2			
18	13	—	GPIOC5	GPIOC5	DACA_O	XB_IN7		
19	—	—	GPIOB6	GPIOB6	ANB6&CMPB_IN1			

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev. No.	Date	Substantial Changes
2	10/2013	First public release
2.1	11/2013	• In Table 2, added DACB_O signal description. • In Obtaining package dimensions, changed 32-QFN's document number from '98ARE10566D' to '98ASA00473D'.

2.2	03/2016 - 05/2016	• Corrected document part number MC56F827XXDS to MC56F827XX.
		• In "12-bit ADC Electrical Specifications" table, corrected Max Gain Error to 0.990 to 1.010.
		• In Part identification section, in part number fields table, added the 32QFN package identifier.
		• In Electrical design considerations" section, added additional section "Power-on Reset design considerations".
		• Added new section "Power-on Reset design considerations".
		• In "Peripheral highlights" section, added
		  • Periodic Interrupt Timer (PIT) Modules
		  • External Watchdog Monitor (EWM)

3.0	09/2016	• Added products: 56F82746MLF, 56F82733MFM
		• Removed PDB (Programmable Delay Block) mentions, because PDBs are not present in these devices.
		• Added V and M temperature options to operating characteristics.
		• Moved "Signal groups" section under "MC56F827xx signal and pin descriptions" section.
		• In "Voltage and current operating ratings" section: updated note; in "Absolute Maximum Ratings" table, updated Ambient and Junction Temperature rows, also fixed broken footnotes.
		• In "Power consumption operating behaviors" section, in "Current Consumption" table: added columns and data for Maximum at 3.6V, 125°C", fixed broken footnotes.
		• In "Thermal operating requirements" section, updated Die junction temperature and Ambient temperature requirements.
		• In "Relaxation Oscillator Timing" section, in "Relaxation Oscillator Electrical Specifications" table:
		  • Added data for "-40°C to 125°C" temperature range.
		  • For "8 MHz Output Frequency, Standby Mode frequency", 2 corrections were made.
		  • Fixed broken footnotes.