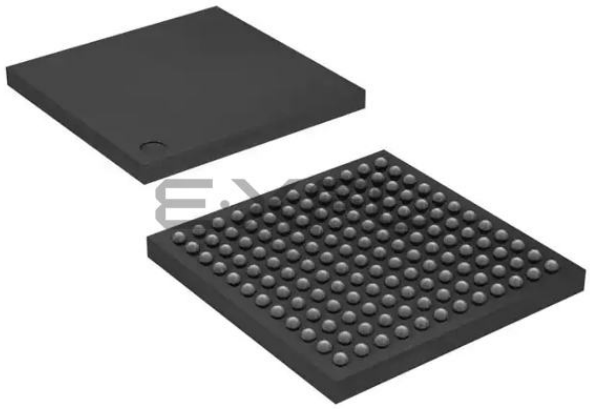

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 100 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 58x16b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-MAPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60fn1m0vmd12r |

- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB high-/full-/low-speed On-the-Go controller with ULPI interface
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect (USBDCD)
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital Host Controller (SDHC)
  - Two I2S modules

## Table 4. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Output high voltage — low drive strength | | | — | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2mA | $V_{DD}$ – 0.5 | — | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6mA | $V_{DD}$ – 0.5 | — | | V | |
| $I_{OHT}$ | Output high current total for all ports | — | — | 100 | mA | |
| $I_{OHT\_io60}$ | Output high current total for fast digital ports | — | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | — | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 10 mA | — | | — | 0.5 | V |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 5 mA | — | | | 0.5 | V |
| | Output low voltage — low drive strength | | | — | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2 mA | — | | — | 0.5 | V |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 1 mA | — | | | 0.5 | V |
| $I_{OLT}$ | Output low current total for all ports | — | — | 100 | mA | |
| $I_{OLT\_io60}$ | Output low current total for fast digital ports | — | — | 100 | mA | |
| $I_{INA}$ | Input leakage current, analog pins and digital pins configured as analog inputs | | | | | 1, 2 |
| | • $V_{SS}$ ≤ $V_{IN}$ ≤ $V_{DD}$ | | | | | |
| | • All pins except EXTAL32, XTAL32, EXTAL, XTAL | — | 0.002 | 0.5 | µA | |
| | • EXTAL (PTA18) and XTAL (PTA19) | — | 0.004 | 1.5 | µA | |
| | • EXTAL32, XTAL32 | — | 0.075 | 10 | µA | |
| $I_{IND}$ | Input leakage current, digital pins | | | | | 2, 3 |
| | • $V_{SS}$ ≤ $V_{IN}$ ≤ $V_{IL}$ | | | | | |
| | • All digital pins | — | 0.002 | 0.5 | µA | |
| | • $V_{IN}$ = $V_{DD}$ | | | | | |
| | • All digital pins except PTD7 | — | 0.002 | 0.5 | µA | |
| | • PTD7 | — | 0.004 | 1 | µA | |
| $I_{IND}$ | Input leakage current, digital pins | | | | | 2, 3, 4 |
| | • $V_{IL}$ < $V_{IN}$ < $V_{DD}$ | | | | | |
| | • $V_{DD}$ = 3.6 V | — | 18 | 26 | µA | |
| | • $V_{DD}$ = 3.0 V | — | 12 | 19 | µA | |
| | • $V_{DD}$ = 2.5 V | — | 8 | 13 | µA | |
| | • $V_{DD}$ = 1.7 V | — | 3 | 6 | µA | |
| $I_{IND}$ | Input leakage current, digital pins | | | | | 2, 3 |
| | • $V_{DD}$ < $V_{IN}$ < 5.5 V | — | 1 | 50 | µA | |
| $Z_{IND}$ | Input impedance examples, digital pins | | | | | 2, 5 |
| | | — | — | 48 | kΩ | |

*Table continues on the next page...*

**Table 4. Voltage and current operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • $V_{DD}$ = 3.6 V<br>• $V_{DD}$ = 3.0 V<br>• $V_{DD}$ = 2.5 V<br>• $V_{DD}$ = 1.7 V | —<br>—<br>— | —<br>—<br>— | 55<br>57<br>85 | kΩ<br>kΩ<br>kΩ | |
| $R_{PU}$ | Internal pullup resistors | 20 | — | 50 | kΩ | 6 |
| $R_{PD}$ | Internal pulldown resistors | 20 | — | 50 | kΩ | 7 |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
3. Internal pull-up/pull-down resistors disabled.
4. Characterized, not tested in production.
5. Examples calculated using $V_{IL}$ relation, $V_{DD}$, and max $I_{IND}$: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below $V_{IL}$ due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V. See Figure 2.
6. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$
7. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{DD}$

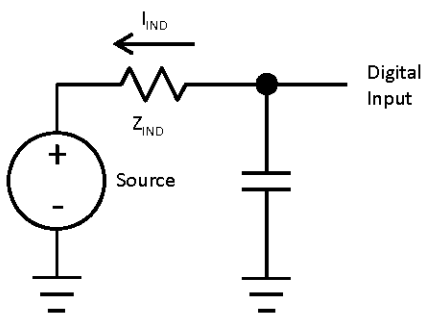


**Figure 2. 5 V Tolerant Input IIND Parameter**

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

5. 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
6. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode at greater than 100 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

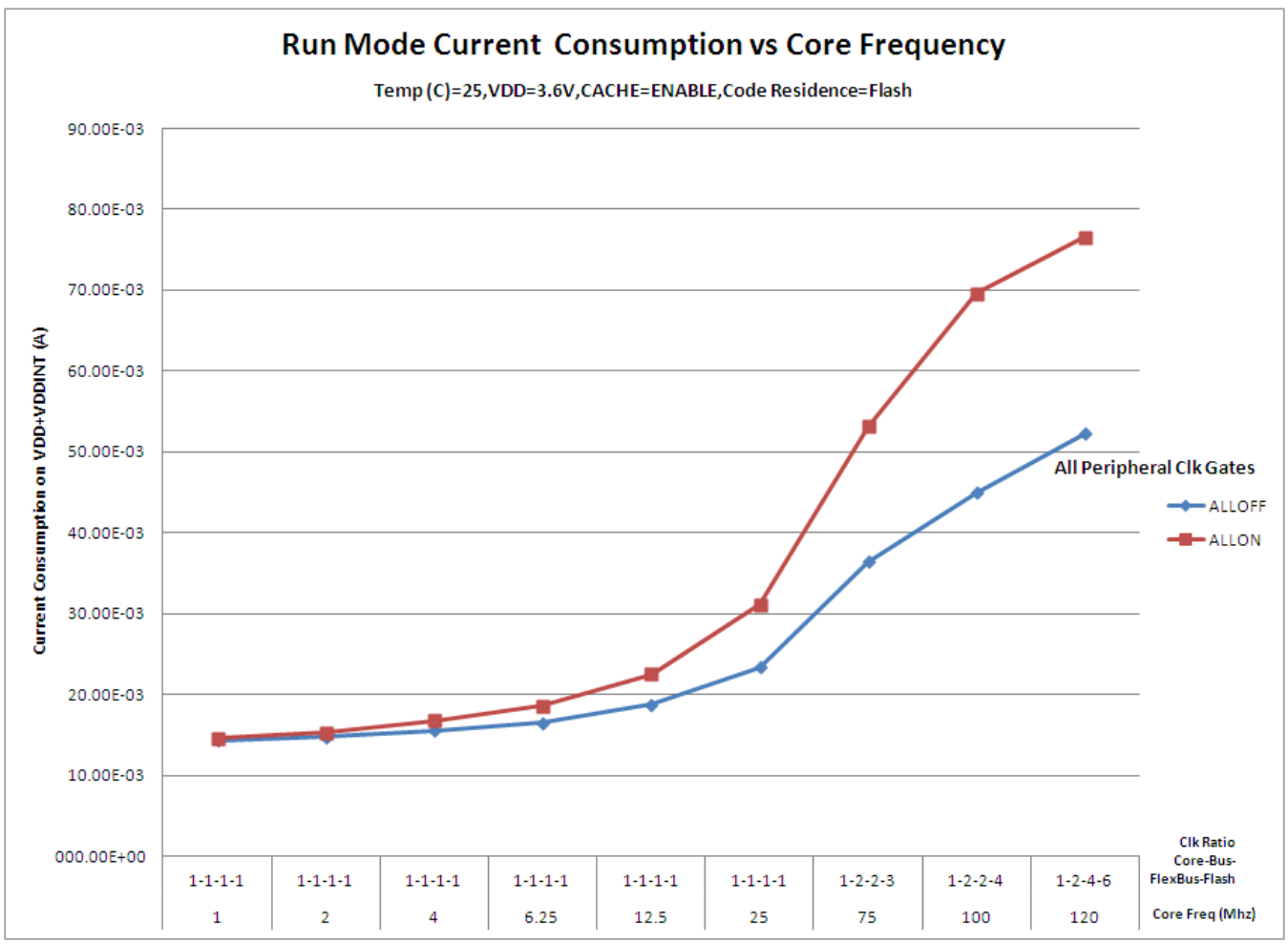


**Figure 3. Run mode supply current vs. core frequency**

**Table 9. Device clock specifications (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $f_{BUS}$ | Bus clock | — | 4 | MHz | |
| FB_CLK | FlexBus clock | — | 4 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 0.5 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 4 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

**Table 10. General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path | 100 | — | ns | 3 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 16 | — | ns | 3 |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns | 3 |
| | Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion | 2 | — | Bus clock cycles | |
| | Port rise and fall time (high drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br><br>—<br>—<br><br>—<br>— | <br><br><br>14<br>8<br><br>36<br>24 | <br><br><br>ns<br>ns<br><br>ns<br>ns | 4 |
| | Port rise and fall time (low drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br><br>—<br>—<br><br>—<br>— | <br><br><br>14<br>8<br><br>36<br>24 | <br><br><br>ns<br>ns<br><br>ns<br>ns | 5 |

*Table continues on the next page...*

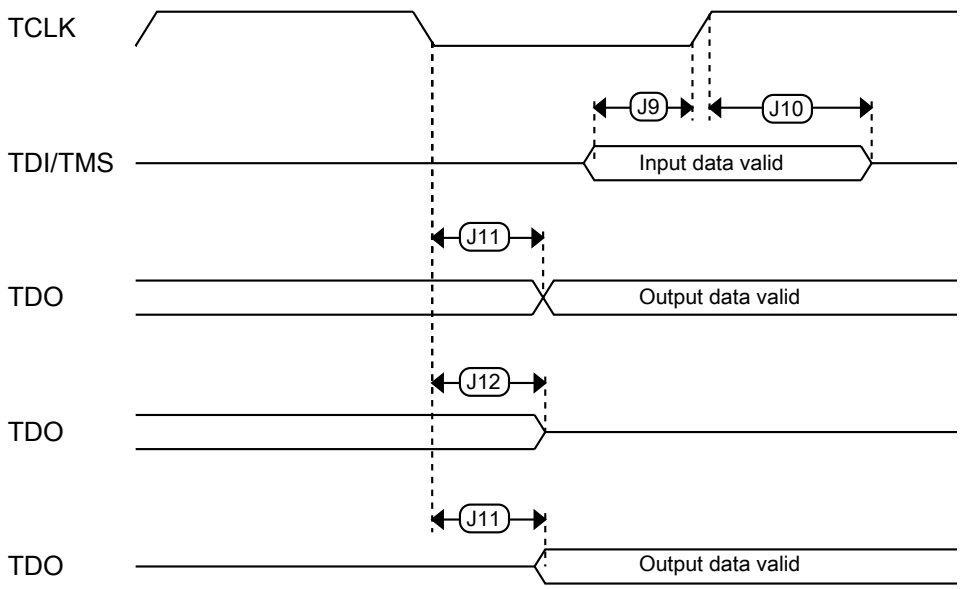


**Figure 9. Test Access Port timing**

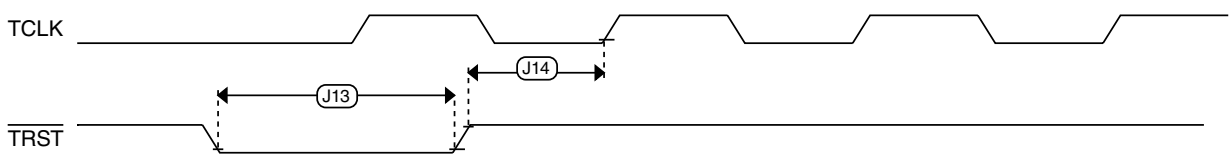


**Figure 10. $\overline{\text{TRST}}$ timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

**Table 15. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | | — | ± 0.2 | ± 0.5 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 4.5 | — | $\%f_{dco}$ | 1 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 4 | — | MHz | |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) 640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 2, 3 |
| | | Mid range (DRS=01) 1280 × $f_{fll\_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) 1920 × $f_{fll\_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) 2560 × $f_{fll\_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00) 732 × $f_{fll\_ref}$ | — | 23.99 | — | MHz | 4, 5 |
| | | Mid range (DRS=01) 1464 × $f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) 2197 × $f_{fll\_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) 2929 × $f_{fll\_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc\_fll}$ | FLL period jitter | | — | 180 | — | ps | |

*Table continues on the next page...*

### 6.4.1.3 Flash high voltage current behaviors

**Table 22. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 3.5 | 7.5 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 6.4.1.4 Reliability specifications

**Table 23. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Program Flash | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | Data Flash | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | FlexRAM as EEPROM | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | |
| $n_{nvmcycee}$ | Cycling endurance for EEPROM backup | 20 K | 50 K | — | cycles | 2 |
| | Write endurance | | | | | 3 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 70 K | 175 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 630 K | 1.6 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 2.5 M | 6.4 M | — | writes | |
| $n_{nvmwree2k}$ | • EEPROM backup to FlexRAM ratio = 2,048 | 10 M | 25 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ $T_j$ ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup per subsystem. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

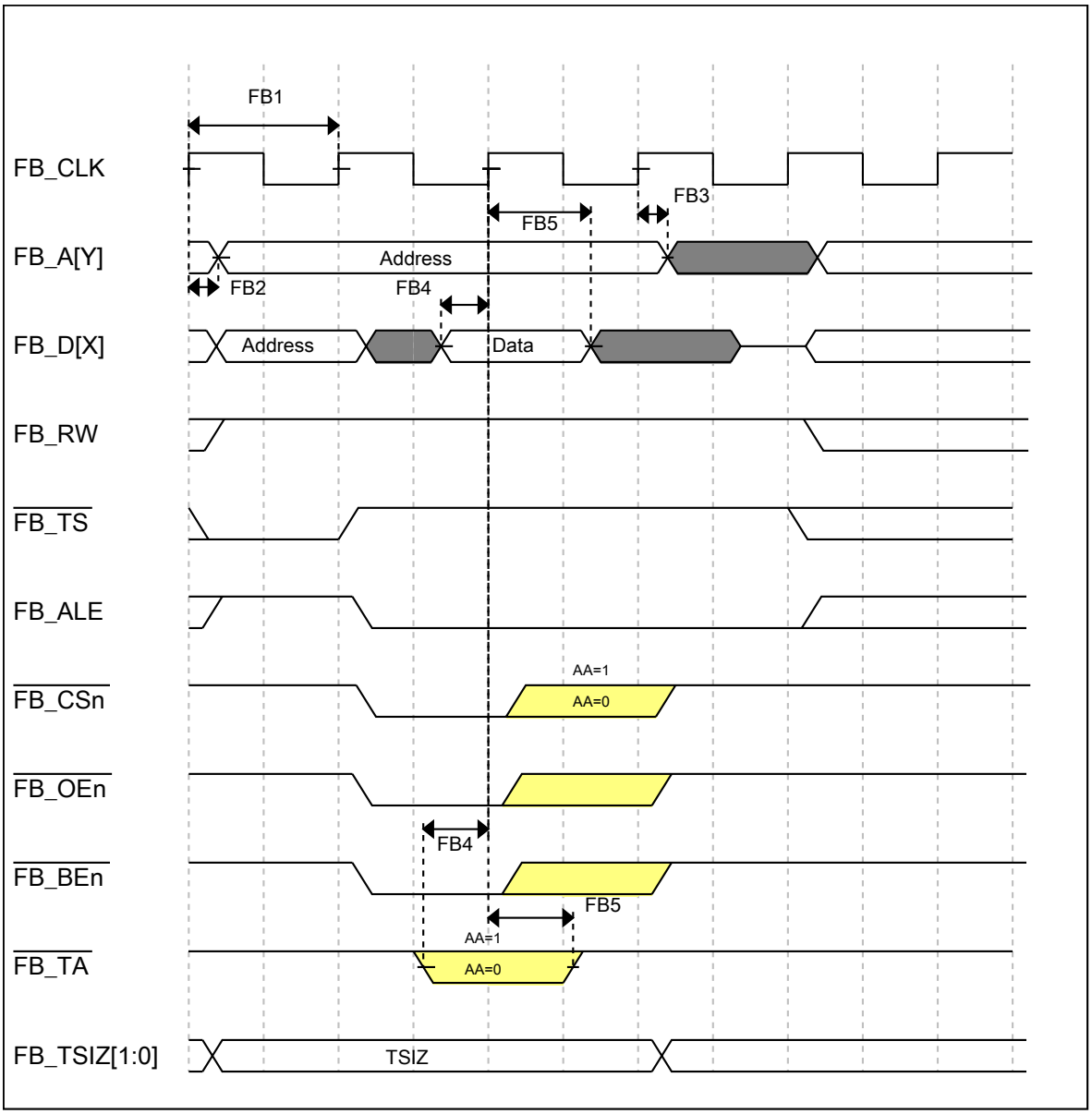


**Figure 18. FlexBus read timing diagram**

## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 28 and Table 29 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 30 and Table 31.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 28. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 × VREFH<br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-bit / 10-bit / 12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input series resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance (external) | 13-bit / 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging | 37.037 | — | 461.467 | ksps | 5 |

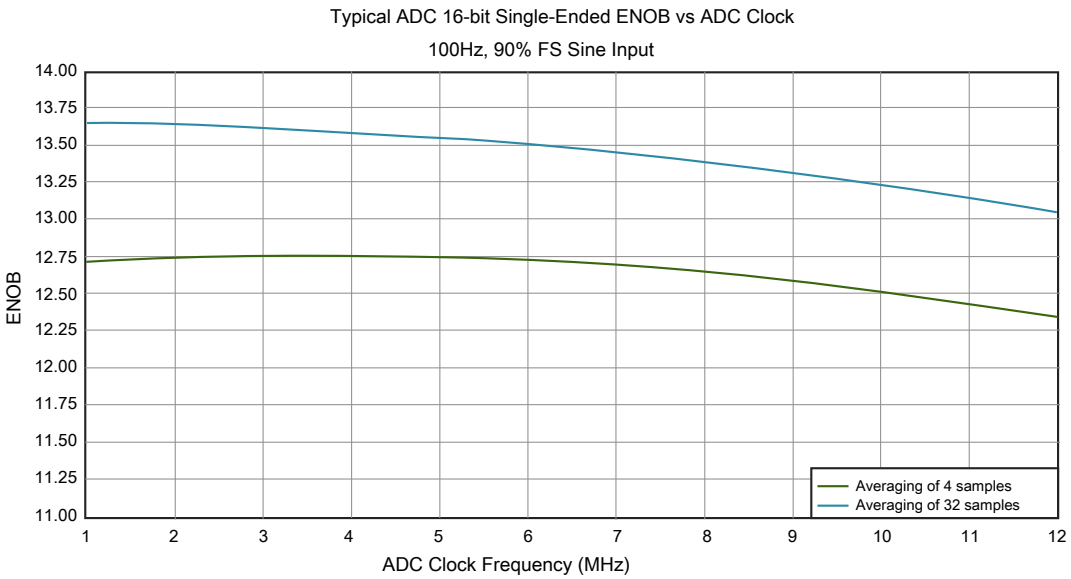


**Figure 22. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 30. 16-bit ADC with PGA operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8 | — | 128 | — | kΩ | IN+ to IN-[4] |
| | | Gain = 16, 32 | — | 64 | — | | |
| | | Gain = 64 | — | 32 | — | | |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_S$ | ADC sampling time | | 1.25 | — | — | μs | 6 |
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 18.484 | — | 450 | Ksps | 7 |
| | | 16 bit modes | 37.037 | — | 250 | Ksps | 8 |

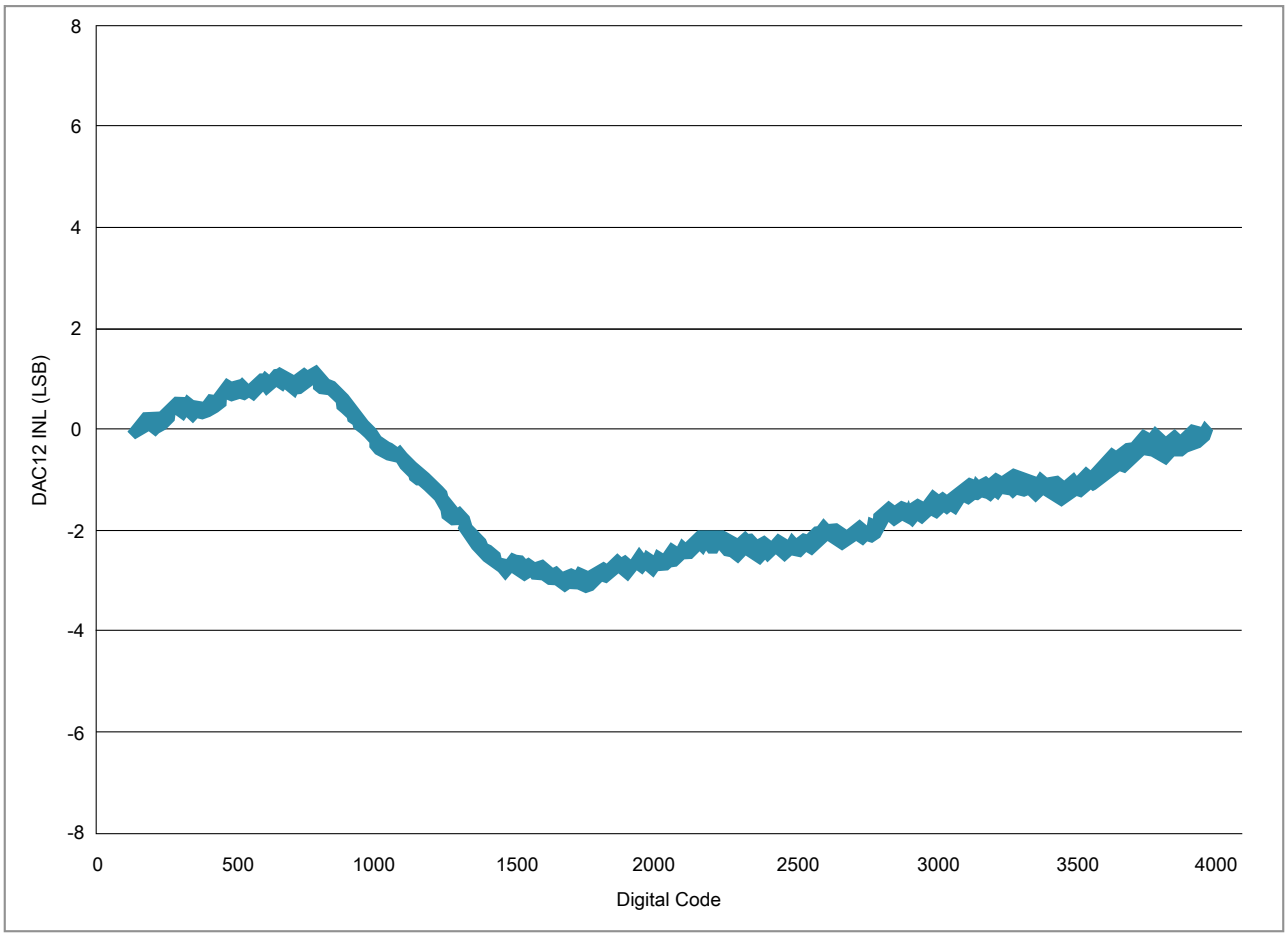


**Figure 25. Typical INL error vs. digital code**

### 6.8.5 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

**Table 43. ULPI timing specifications**

| Num | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | USB_CLKIN operating frequency | — | 60 | — | MHz |
| | USB_CLKIN duty cycle | — | 50 | — | % |
| U1 | USB_CLKIN clock period | — | 16.67 | — | ns |
| U2 | Input setup (control and data) | 5 | — | — | ns |
| U3 | Input hold (control and data) | 1 | — | — | ns |
| U4 | Output valid (control and data) | — | — | 9.5 | ns |
| U5 | Output hold (control and data) | 1 | — | — | ns |

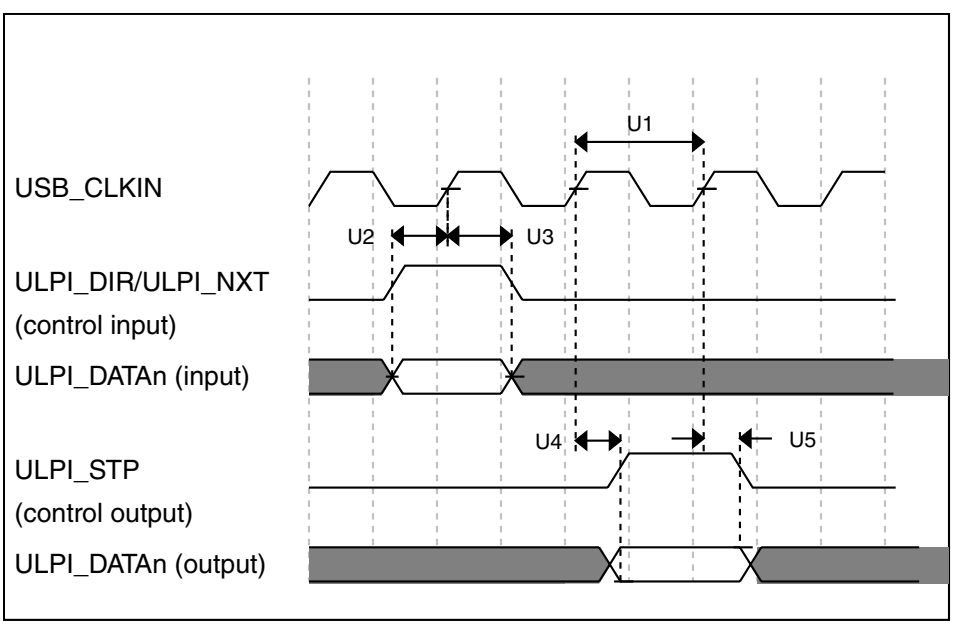


**Figure 29. ULPI timing diagram**

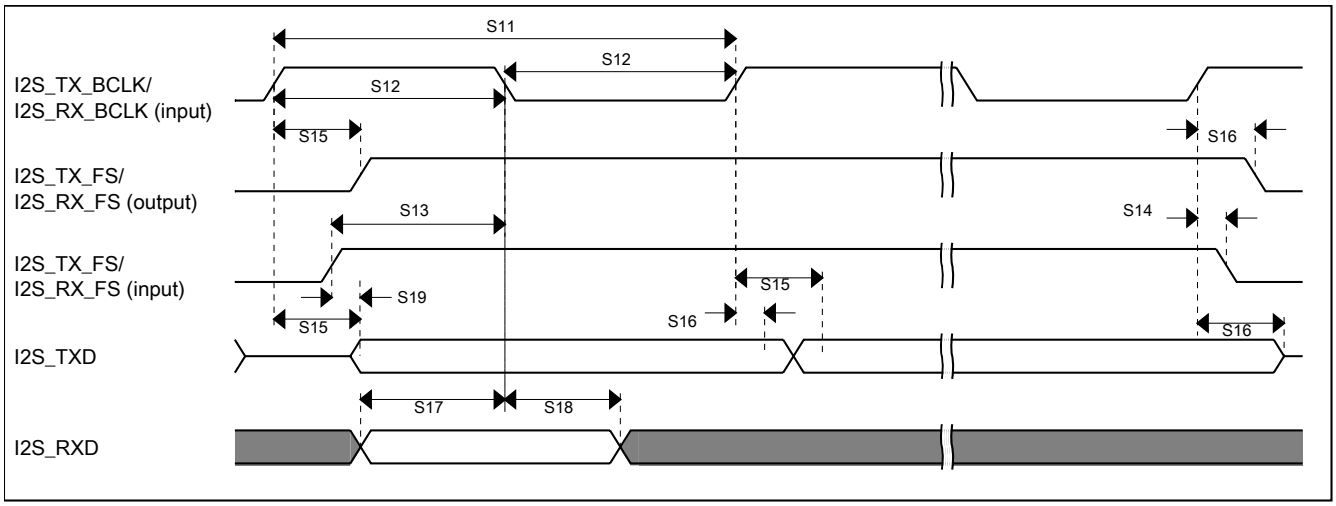


**Figure 39. I2S/SAI timing — slave modes**

### 6.8.12.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | -1.6 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 45 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

**Table 58. Pins with active pull control after reset**

| Pin | Active pull direction after reset |
|---|---|
| PTA0 | pulldown |
| PTA1 | pullup |
| PTA3 | pullup |
| PTA4 | pullup |
| RESET_b | pullup |

## 8.2 K60 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | L5 | RTC_ WAKEUP_B | RTC_ WAKEUP_B | RTC_ WAKEUP_B | | | | | | | | |
| — | M5 | NC | NC | NC | | | | | | | | |
| — | A10 | NC | NC | NC | | | | | | | | |
| — | B10 | NC | NC | NC | | | | | | | | |
| — | C10 | NC | NC | NC | | | | | | | | |
| 1 | D3 | PTE0 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | SDHC0_D1 | | I2C1_SDA | RTC_ CLKOUT | |
| 2 | D2 | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | SDHC0_D0 | | I2C1_SCL | SPI1_SIN | |
| 3 | D1 | PTE2/ LLWU_P1 | ADC1_SE6a | ADC1_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_ CTS_b | SDHC0_ DCLK | | | | |
| 4 | E4 | PTE3 | ADC1_SE7a | ADC1_SE7a | PTE3 | SPI1_SIN | UART1_ RTS_b | SDHC0_CMD | | | SPI1_SOUT | |
| 5 | E5 | VDD | VDD | VDD | | | | | | | | |
| 6 | F6 | VSS | VSS | VSS | | | | | | | | |
| 7 | E3 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | SDHC0_D3 | | | | |
| 8 | E2 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | SDHC0_D2 | | FTM3_CH0 | | |
| 9 | E1 | PTE6 | DISABLED | | PTE6 | SPI1_PCS3 | UART3_ CTS_b | I2S0_MCLK | | FTM3_CH1 | USB_SOF_ OUT | |
| 10 | F4 | PTE7 | DISABLED | | PTE7 | | UART3_ RTS_b | I2S0_RXD0 | | FTM3_CH2 | | |
| 11 | F3 | PTE8 | ADC2_SE16 | ADC2_SE16 | PTE8 | I2S0_RXD1 | UART5_TX | I2S0_RX_FS | | FTM3_CH3 | | |
| 12 | F2 | PTE9 | ADC2_SE17 | ADC2_SE17 | PTE9 | I2S0_TXD1 | UART5_RX | I2S0_RX_ BCLK | | FTM3_CH4 | | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 13 | F1 | PTE10 | DISABLED | | PTE10 | | UART5_ CTS_b | I2S0_TXD0 | | FTM3_CH5 | | |
| 14 | G4 | PTE11 | ADC3_SE16 | ADC3_SE16 | PTE11 | | UART5_ RTS_b | I2S0_TX_FS | | FTM3_CH6 | | |
| 15 | G3 | PTE12 | ADC3_SE17 | ADC3_SE17 | PTE12 | | | I2S0_TX_ BCLK | | FTM3_CH7 | | |
| 16 | E6 | VDD | VDD | VDD | | | | | | | | |
| 17 | F7 | VSS | VSS | VSS | | | | | | | | |
| 18 | H3 | VSS | VSS | VSS | | | | | | | | |
| 19 | H1 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |
| 20 | H2 | USB0_DM | USB0_DM | USB0_DM | | | | | | | | |
| 21 | G1 | VOUT33 | VOUT33 | VOUT33 | | | | | | | | |
| 22 | G2 | VREGIN | VREGIN | VREGIN | | | | | | | | |
| 23 | J1 | PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1 | PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1 | PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1 | | | | | | | | |
| 24 | J2 | PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1 | PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1 | PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1 | | | | | | | | |
| 25 | K1 | PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1 | PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1 | PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1 | | | | | | | | |
| 26 | K2 | PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1 | PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1 | PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1 | | | | | | | | |
| 27 | L1 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| 28 | L2 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| 29 | M1 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | | | | | | | | |
| 30 | M2 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | | | | | | | | |
| 31 | H5 | VDDA | VDDA | VDDA | | | | | | | | |
| 32 | G5 | VREFH | VREFH | VREFH | | | | | | | | |
| 33 | G6 | VREFL | VREFL | VREFL | | | | | | | | |
| 34 | H6 | VSSA | VSSA | VSSA | | | | | | | | |
| 35 | K3 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | ADC1_SE16/ CMP2_IN2/ ADC0_SE22 | | | | | | | | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 83 | G12 | PTB2 | ADC0_SE12/ TSI0_CH7 | ADC0_SE12/ TSI0_CH7 | PTB2 | I2C0_SCL | UART0_ RTS_b | ENET0_ 1588_TMR0 | | FTM0_FLT3 | | |
| 84 | G11 | PTB3 | ADC0_SE13/ TSI0_CH8 | ADC0_SE13/ TSI0_CH8 | PTB3 | I2C0_SDA | UART0_ CTS_b/ UART0_ COL_b | ENET0_ 1588_TMR1 | | FTM0_FLT0 | | |
| 85 | G10 | PTB4 | ADC1_SE10 | ADC1_SE10 | PTB4 | | | ENET0_ 1588_TMR2 | | FTM1_FLT0 | | |
| 86 | G9 | PTB5 | ADC1_SE11 | ADC1_SE11 | PTB5 | | | ENET0_ 1588_TMR3 | | FTM2_FLT0 | | |
| 87 | F12 | PTB6 | ADC1_SE12 | ADC1_SE12 | PTB6 | | | | FB_AD23 | | | |
| 88 | F11 | PTB7 | ADC1_SE13 | ADC1_SE13 | PTB7 | | | | FB_AD22 | | | |
| 89 | F10 | PTB8 | DISABLED | | PTB8 | | UART3_ RTS_b | | FB_AD21 | | | |
| 90 | F9 | PTB9 | DISABLED | | PTB9 | SPI1_PCS1 | UART3_ CTS_b | | FB_AD20 | | | |
| 91 | E12 | PTB10 | ADC1_SE14 | ADC1_SE14 | PTB10 | SPI1_PCS0 | UART3_RX | I2S1_TX_ BCLK | FB_AD19 | FTM0_FLT1 | | |
| 92 | E11 | PTB11 | ADC1_SE15 | ADC1_SE15 | PTB11 | SPI1_SCK | UART3_TX | I2S1_TX_FS | FB_AD18 | FTM0_FLT2 | | |
| 93 | H7 | VSS | VSS | VSS | | | | | | | | |
| 94 | F5 | VDD | VDD | VDD | | | | | | | | |
| 95 | E10 | PTB16 | TSI0_CH9 | TSI0_CH9 | PTB16 | SPI1_SOUT | UART0_RX | I2S1_TXD0 | FB_AD17 | EWM_IN | | |
| 96 | E9 | PTB17 | TSI0_CH10 | TSI0_CH10 | PTB17 | SPI1_SIN | UART0_TX | I2S1_TXD1 | FB_AD16 | EWM_OUT_b | | |
| 97 | D12 | PTB18 | TSI0_CH11 | TSI0_CH11 | PTB18 | CAN0_TX | FTM2_CH0 | I2S0_TX_ BCLK | FB_AD15 | FTM2_QD_ PHA | | |
| 98 | D11 | PTB19 | TSI0_CH12 | TSI0_CH12 | PTB19 | CAN0_RX | FTM2_CH1 | I2S0_TX_FS | FB_OE_b | FTM2_QD_ PHB | | |
| 99 | D10 | PTB20 | ADC2_SE4a | ADC2_SE4a | PTB20 | SPI2_PCS0 | | | FB_AD31/ NFC_ DATA15 | CMP0_OUT | | |
| 100 | D9 | PTB21 | ADC2_SE5a | ADC2_SE5a | PTB21 | SPI2_SCK | | | FB_AD30/ NFC_ DATA14 | CMP1_OUT | | |
| 101 | C12 | PTB22 | DISABLED | | PTB22 | SPI2_SOUT | | | FB_AD29/ NFC_ DATA13 | CMP2_OUT | | |
| 102 | C11 | PTB23 | DISABLED | | PTB23 | SPI2_SIN | SPI0_PCS5 | | FB_AD28/ NFC_ DATA12 | CMP3_OUT | | |
| 103 | B12 | PTC0 | ADC0_SE14/ TSI0_CH13 | ADC0_SE14/ TSI0_CH13 | PTC0 | SPI0_PCS4 | PDB0_ EXTRG | | FB_AD14/ NFC_ DATA11 | I2S0_TXD1 | | |
| 104 | B11 | PTC1/ LLWU_P6 | ADC0_SE15/ TSI0_CH14 | ADC0_SE15/ TSI0_CH14 | PTC1/ LLWU_P6 | SPI0_PCS3 | UART1_ RTS_b | FTM0_CH0 | FB_AD13/ NFC_ DATA10 | I2S0_TXD0 | | |
| 105 | A12 | PTC2 | ADC0_SE4b/ CMP1_IN0/ TSI0_CH15 | ADC0_SE4b/ CMP1_IN0/ TSI0_CH15 | PTC2 | SPI0_PCS2 | UART1_ CTS_b | FTM0_CH1 | FB_AD12/ NFC_DATA9 | I2S0_TX_FS | | |

| 144 LQFP | 144 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 106 | A11 | PTC3/ LLWU_P7 | CMP1_IN1 | CMP1_IN1 | PTC3/ LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | CLKOUT | I2S0_TX_ BCLK | | |
| 107 | H8 | VSS | VSS | VSS | | | | | | | | |
| 108 | — | VDD | VDD | VDD | | | | | | | | |
| 109 | A9 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | FB_AD11/ NFC_DATA8 | CMP1_OUT | I2S1_TX_ BCLK | |
| 110 | D8 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ ALT2 | I2S0_RXD0 | FB_AD10/ NFC_DATA7 | CMP0_OUT | I2S1_TX_FS | |
| 111 | C8 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_SOUT | PDB0_ EXTRG | I2S0_RX_ BCLK | FB_AD9/ NFC_DATA6 | I2S0_MCLK | | |
| 112 | B8 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | USB_SOF_ OUT | I2S0_RX_FS | FB_AD8/ NFC_DATA5 | | | |
| 113 | A8 | PTC8 | ADC1_SE4b/ CMP0_IN2 | ADC1_SE4b/ CMP0_IN2 | PTC8 | | FTM3_CH4 | I2S0_MCLK | FB_AD7/ NFC_DATA4 | | | |
| 114 | D7 | PTC9 | ADC1_SE5b/ CMP0_IN3 | ADC1_SE5b/ CMP0_IN3 | PTC9 | | FTM3_CH5 | I2S0_RX_ BCLK | FB_AD6/ NFC_DATA3 | FTM2_FLT0 | | |
| 115 | C7 | PTC10 | ADC1_SE6b | ADC1_SE6b | PTC10 | I2C1_SCL | FTM3_CH6 | I2S0_RX_FS | FB_AD5/ NFC_DATA2 | I2S1_MCLK | | |
| 116 | B7 | PTC11/ LLWU_P11 | ADC1_SE7b | ADC1_SE7b | PTC11/ LLWU_P11 | I2C1_SDA | FTM3_CH7 | I2S0_RXD1 | FB_RW_b/ NFC_WE | | | |
| 117 | A7 | PTC12 | DISABLED | | PTC12 | | UART4_ RTS_b | | FB_AD27 | FTM3_FLT0 | | |
| 118 | D6 | PTC13 | DISABLED | | PTC13 | | UART4_ CTS_b | | FB_AD26 | | | |
| 119 | C6 | PTC14 | DISABLED | | PTC14 | | UART4_RX | | FB_AD25 | | | |
| 120 | B6 | PTC15 | DISABLED | | PTC15 | | UART4_TX | | FB_AD24 | | | |
| 121 | — | VSS | VSS | VSS | | | | | | | | |
| 122 | — | VDD | VDD | VDD | | | | | | | | |
| 123 | A6 | PTC16 | DISABLED | | PTC16 | CAN1_RX | UART3_RX | ENET0_ 1588_TMR0 | FB_CS5_b/ FB_TSIZ1/ FB_BE23_ 16_b | NFC_RB | | |
| 124 | D5 | PTC17 | DISABLED | | PTC17 | CAN1_TX | UART3_TX | ENET0_ 1588_TMR1 | FB_CS4_b/ FB_TSIZ0/ FB_BE31_ 24_b | NFC_CE0_b | | |
| 125 | C5 | PTC18 | DISABLED | | PTC18 | | UART3_ RTS_b | ENET0_ 1588_TMR2 | FB_TBST_b/ FB_CS2_b/ FB_BE15_8_ b | NFC_CE1_b | | |
| 126 | B5 | PTC19 | DISABLED | | PTC19 | | UART3_ CTS_b | ENET0_ 1588_TMR3 | FB_CS3_b/ FB_BE7_0_b | FB_TA_b | | |
| 127 | A5 | PTD0/ LLWU_P12 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_ RTS_b | FTM3_CH0 | FB_ALE/ FB_CS1_b/ FB_TS_b | I2S1_RXD1 | | |
| 128 | D4 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_ CTS_b | FTM3_CH1 | FB_CS0_b | I2S1_RXD0 | | |


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